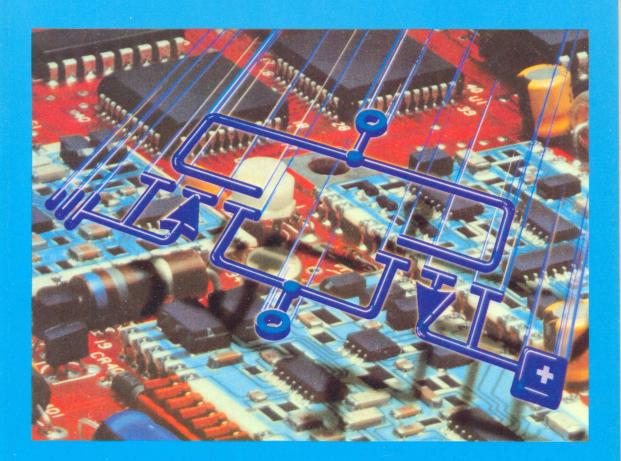


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# HIGH-SPEED CMOS LOGIC DATA

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The "Better" Program 3

Design Considerations 4

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Reliability 6

Package Dimensions

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## HIGH-SPEED CMOS LOGIC DATA

Prepared by Technical Information Center

This book presents technical data for the broad line of High-Speed Logic integrated circuits. Complete specifications are provided in the form of data sheets. In addition, a comprehensive Function Selector Guide and a Design Considerations chapter have been included to familiarize the user with these logic circuits.

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MOTOROLA HIGH-SPEED CMOS LOGIC DATA

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Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC04 HCT04 HCU04 HC05 HCT05	Hex Inverter Hex Inverter with LSTTL-Compatible Inputs Hex Unbuffered Inverter Hex Inverter with Open-Drain Outputs Hex Inverter with Open-Drain Outputs and LSTTL-Compatible Inputs	LS04 LS04 LS04 LS05 LS05	*4069 *4069 4069	LS/CMOS LS/CMOS LS/CMOS LS LS	14 14 14 14 14
HC14 HC34 HCT34 HC35 HCT35	Hex Schmitt-Trigger Inverter Hex Noninverting Buffer Hex Noninverting Buffer with LSTTL-Compatible Inputs Hex Noninverting Buffer with Open-Drain Outputs Hex Noninverting Buffer with Open-Drain Outputs and LSTTL-Compatible Inputs	LS14 LS34 LS34 LS35 LS35	4584	LS/CMOS LS LS LS LS	14 14 14, 14 14
HC125 HC126 HC240 HCT240	Quad 3-State Noninverting Buffer Quad 3-State Noninverting Buffer Octal 3-State Inverting Buffer/Line Driver/Line Receiver Octal 3-State Inverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs Octal 3-State Noninverting Buffer/Line Driver/Line Receiver	LS125,LS125A LS126,LS126A LS240 LS240		LS LS LS LS	14 14 20 20 20
HCT241 HC242 HC243 HC244 HCT244	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs Quad 3-State Inverting Bus Transceiver Quad 3-State Noninverting Bus Transceiver Octal 3-State Noninverting Buffer/Line Driver/Line Receiver Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	LS241 LS242 LS243 LS244 LS244	stevie	LS LS LS LS	20 14 14 20 20
HC245 HCT245 HC365 HC366 HC367	Octal 3-State Noninverting Bus Transceiver Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs Hex 3-State Noninverting Buffer with Common Enables Hex 3-State Inverting Buffer with Common Enables Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections	LS245 LS245 LS365,LS365A LS366,LS366A LS367,LS367A	4503	LS LS LS LS LS/CMOS	20 20 16 16 16
HC368 HC540 HCT540 HC541 HCT541	Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections Octal 3-State Inverting Buffer/Line Driver/Line Receiver Octal 3-State Inverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs Octal 3-State Noninverting Buffer/Line Driver/Line Receiver Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	LS368,LS368A LS540 LS540 LS541 LS541	ous Devices	LS LS LS LS	16 20 20 20 20 20
HC620 HCT620 HC623 HCT623 HC640	Octal 3-State Inverting Bus Transceiver Octal 3-State Inverting Bus Transceiver with LSTTL-Compatible Inputs Octal 3-State Noninverting Bus Transceiver Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs Octal 3-State Inverting Bus Transceiver	LS620 LS620 LS623 LS623 LS640		LS LS LS LS	20 20 20 20 20
HCT640 HC643 HCT643 HC4049 HC4050	Octal 3-State Inverting Bus Transceiver with LSTTL-Compatible Inputs Octal 3-State Inverting and Noninverting Bus Transceiver Octal 3-State Inverting and Noninverting Bus Transceiver with LSTTL-Compatible Inputs Hex Inverting Buffer/Logic-Level Down Converter Hex Noninverting Buffer/Logic-Level Down Converter	LS640 LS643 LS643	4049 4050	LS LS LS CMOS CMOS	20 20 20 16 16

#### **BUFFERS/INVERTERS (Continued)**

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
★HC9014	Nine-Wide Schmitt-Trigger Inverter	CT Devices Hay	angel elite	ave CMOS-Com	20
★HC9015	Nine-Wide Schmitt-Trigger Noninverting Buffer		No.		20
★ HC9034	Nine-Wide Inverter		TON .	Device	20
<b>★</b> HCT9034	Nine-Wide Inverter with LSTTL-Compatible Inputs			Spinera	20
★ HC9035	Nine-Wide Noninverting Buffer	E 636	505		20
<b>★</b> HCT9035	Nine-Wide Noninverting Buffer with LSTTL-Compatible		26		20
	Inputs				Olygid-Daylid
<b>★</b> HC9114	Nine-Wide Schmitt-Trigger Inverter with Open-Drain Outputs				20
★ HC9115	Nine-Wide Schmitt-Trigger Noninverting Buffer with Open-Drain Outputs				20
★HC9134	Nine-Wide Inverter with Open-Drain Outputs			ap val	20
★HC9135	Nine-Wide Noninverting Buffer with Open-Drain Outputs			g Outputs	20

HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

Device	HCT 04	HCU 04	HCT O5	HC 14	HCT 34	HCT 35	HC 125	HC 126	HC HCT 240	HCT 241	HC 242	HC 243	HCT 244
# Pins	14	14	14	14	14	14	14	14	20	20	14	14	20
Quad Device Hex Device Octal Device Nine-Wide Device		1.	•	•	•	•	•	•		es juis	• tract	ncj•noi G lovel	onio de vi
Noninverting Outputs Inverting Outputs			lugal-sk		LITE.	autil a	Divid 1	OH stu	ent pidte	gmb0-i	ONO =	eH beni	ad b
Single Stage (unbuffered)			371				in the	Mark 1			. would		
Schmitt Trigger	2 8	108	acon	•	120	1 81	106	03.03					
3-State Outputs Open-Drain Output Common Output Enables Active-Low Output Enables Active-High Output Enables Separate 4-Bit Sections Separate 2-Bit and 4-Bit Sections		20	98.	00	20	•		91*		•	Salve	ay solo	
Transceiver Direction Control								*		ible	• 1710 efficience	Stage	lavert Sinck
Logic-Level Down Converter												nonT n	Solve

<sup>\*</sup>Suggested alternative ★ Exclusive High-Speed CMOS design

Device Sumber Caphellest Caphelle

**BUFFERS/INVERTERS (Continued)** 

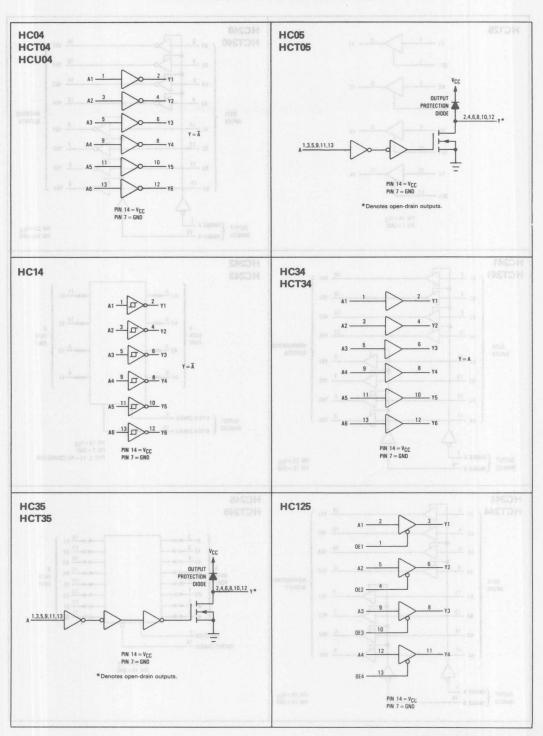
HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

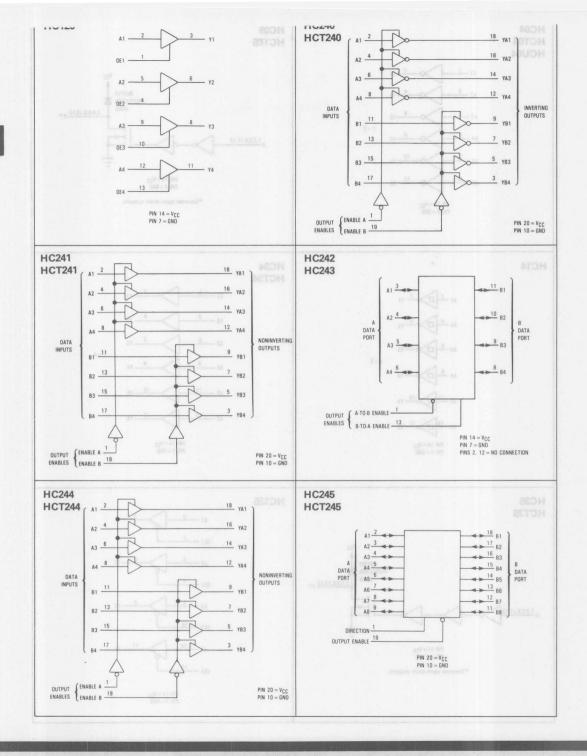
Device	HC HCT 245	HC 365	HC 366	HC 367	HC 368	HC HCT 540	HC HCT 541	HC HCT 620	HC HCT 623	HC HCT 640	HC HCT 643
# Pins	20	16	16	16	16	20	20	20	20	20	20
Quad Device Hex Device Octal Device Nine-Wide Device		•	. 29			diw sasion		-110	mpuks re-Vikla re-Vander Open-Din		DHA DHA
Noninverting Outputs Inverting Outputs	•	•		edvigtuO	niesd-na	QD ranker	shub pri	havring/	ola 🖭 ar	M SEV	DH W
Single Stage (unbuffered)								ukrab 20	AO beed	tripus unit	organization
Schmitt Trigger		- 18 IS									
3-State Outputs Open-Drain Outputs Common Output Enables	•	. briggins .	e ditagnic	D-JTT3.	eval-t asc	ved Tox	freque.	dekragme	0-8010	ovelij sec	weO.Or
Active-Low Output Enables		•	3H*	DEI •	• 31		• 11				
Active-High Output Enables	D\$4	OH	TOH !	DH D	8 10	t une	TOR		600	Det Det	
Separate 4-Bit Sections Separate 2-Bit and 4-Bit Sections	4328	801	36	NE . 1	1 8	7.0	10				
Transceiver Direction Control	:	4						•	•	•sive	i bre D
Logic-Level Down Converter			-							SOIL	PO 887

HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

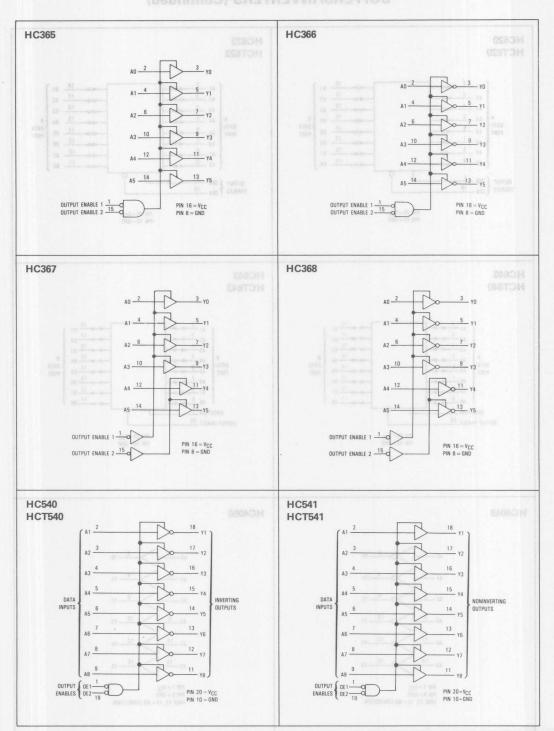
Device	HC 4049	HC 4050	HC 9014	HC 9015	HC HCT 9034	HC HCT 9035	HC 9114	HC 9115	HC 9134	HC 9135
# Pins	16	16	20	20	20	20	20	20	20	20
Quad Device Hex Device Octal Device Nine-Wide Device								asidani asidenii r asidenii r aroiti		omma Levita Levita f
Noninverting Outputs Inverting Outputs		•				•	•	1962 (\$4.1)	Z-Bit and	spansi l
Single Stage (unbuffered)									Control	ortagriC
Schmitt Trigger								Converte	peroG tav	ul-pigo.
3-State Outputs Open-Drain Outputs Common Output Enables Active-Low Output Enables Active-High Output Enables Separate 4-Bit Sections Separate 2-Bit and 4-Bit Sections							•	•	•	•
Transceiver Direction Control										N Ed E
Logic-Level Down Converter										

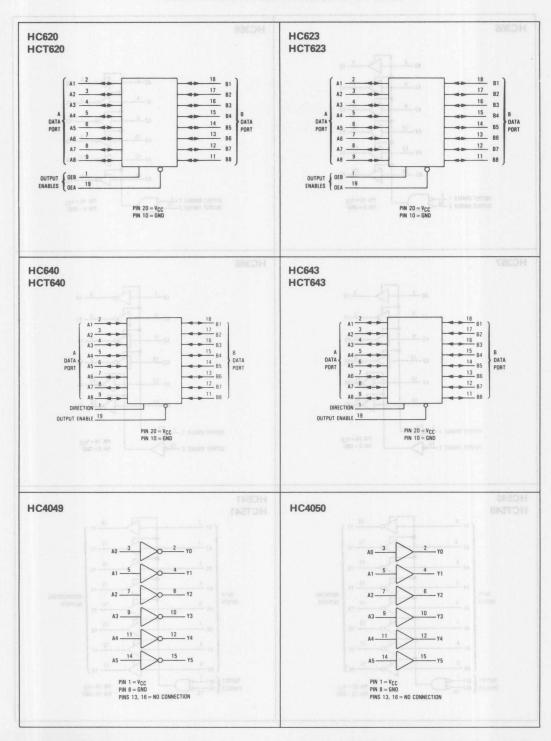
#### **BUFFERS/INVERTERS (Continued)**

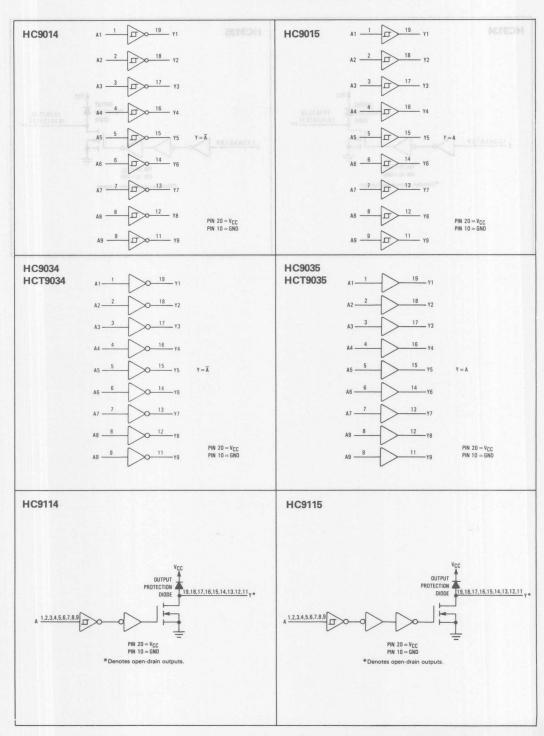


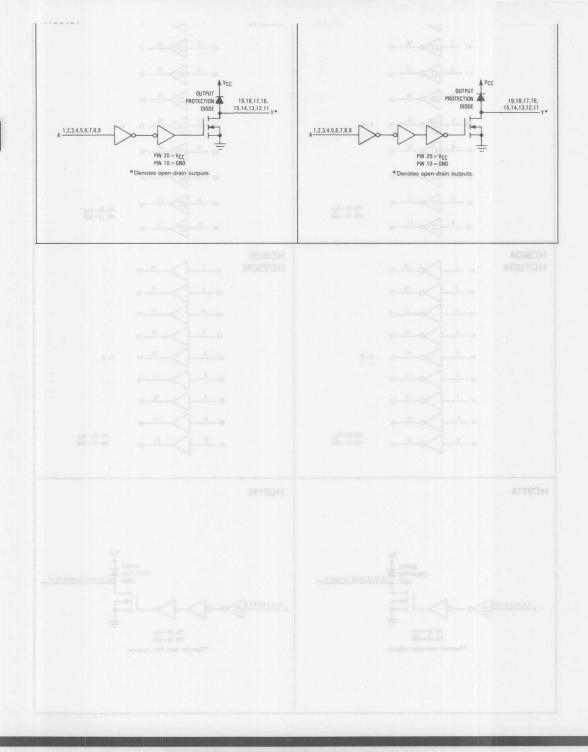


#### **BUFFERS/INVERTERS (Continued)**









Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC00 HC02 HC03 HC08 HC10	Quad 2-Input NAND Gate Quad 2-Input NAND Gate Quad 2-Input NAND Gate with Open-Drain Outputs Quad 2-Input AND Gate Triple 3-Input NAND Gate	LS00 LS02 LS03 LS08 LS10	4011 4001 *4011 4081 4023	LS LS LS LS	14 14 14 14 14
HC11 HC20 HC27 HC30 HC32	Triple 3-Input AND Gate Dual 4-Input NAND Gate Triple 3-Input NOR Gate 8-Input NAND Gate Quad 2-Input OR Gate	LS11 LS20 LS27 LS30 LS32	4073 4012 4025 4068 4071	LS LS LS LS	14 14 14 14 14
HC51 * HC58 HC86 HC132 HC133	2-Wide, 2-Input/2-Wide, 3-Input AND-NOR Gates 2-Wide, 2-Input/2-Wide, 3-Input AND-OR Gates Quad 2-Input Exclusive OR Gate Quad 2-Input NAND Gate with Schmitt-Trigger Inputs 13-Input NAND Gate	LS51 LS86 LS132 LS133	*4506 *4506 4070 4093	LS LS LS LS	14 14 14 14 14
HC266 HC386 HC4002 HC4075 HC4078	Quad 2-Input Exclusive NOR Gate with Open-Drain Outputs Quad 2-Input Exclusive OR Gate Dual 4-Input NOR Gate Triple 3-Input OR Gate 8-Input NOR/OR Gate	LS266 LS386 *LS25	*4077 4070 4002 4075 4078	LS/CMOS LS/CMOS CMOS CMOS CMOS	14 14 14 14 14
★HC7266	Quad 2-Input Exclusive NOR Gate	*LS266	4077	LS/CMOS	14

\*Suggested alternative ★Exclusive High-Speed CMOS design

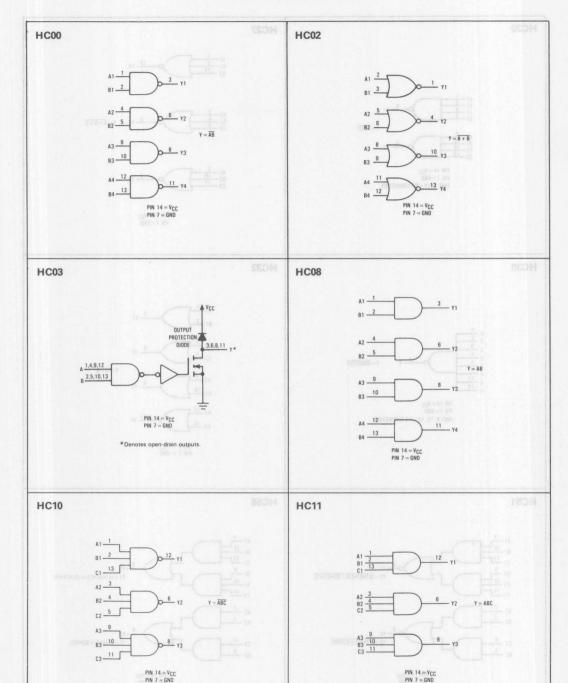
HC Devices Have CMOS-Compatible Inputs.

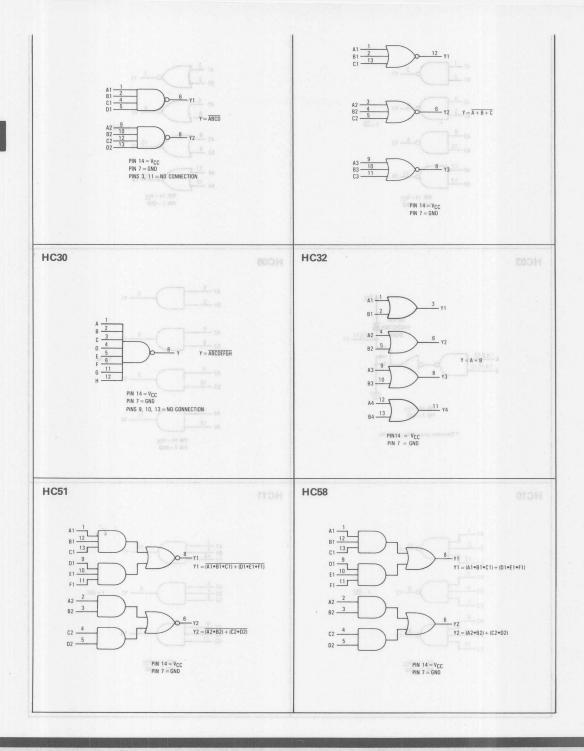
Device		HC 00	HC 02	HC 03	HC 08	HC 10	HC 11	HC 20	HC 27	HC 30	HC 32
# Pins		14	14	14	14	14	14	14	14	14	14
Single Device											
Dual Device Triple Device Quad Device	Equivolent Equivalent Otace	ionobami mnterius				٠			•	-65	Evera
NAND NOR AND OR	Davios WCNACOKX or CDXXXXX	Davice Sazza		•		nou.		71343777		avo,	MCSA/I
Exclusive OR Exclusive NOR AND-NOR AND-OR	4001 7.003.9 4005 4000	1.808 1.808 1.808		183	gsuO nis	Open-D		K NOR G	ad 2-Ingi ad 2-Ingi ad 2-Ingi ala 3-Ingi	10 1	DOH _
2-Input 3-Input 4-Input 8-Input 13-Input	8075 8005 8006 1007	LS71 LS27 LS27 LS32 LS32	i	•	•	•	616 • 976 078	KAND I H NOR G ID Gate	opio 3-ingo logni Mango ed 3-ingo ed 3-ingo	17 1	HC3 HC3 HC3 NC3 HC3
Schmitt-Trigger Inputs	bysis# 1	rea.			etaD ROI	- GWA B	grr-E ,et	W-Cline	Wide, 2-le	2-2	HCS
Open-Drain Outputs	3082.4				eates 98	DOMA 7	dal-E jab	W-EVID	Yide, 2-13	5 8	CHA

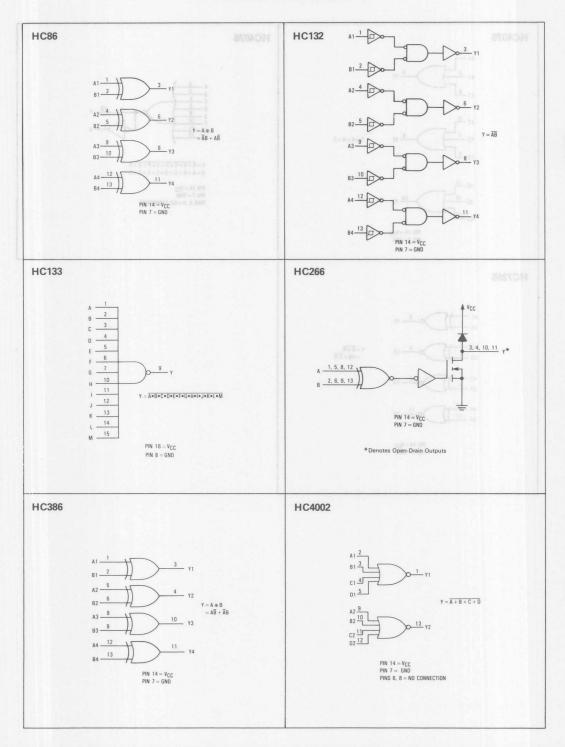
HC Devices Have CMOS-Compatible Inputs.

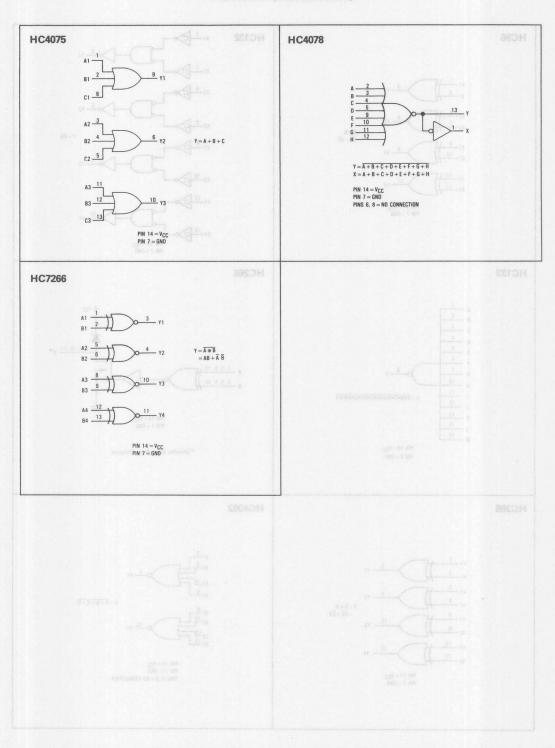
	Device		HC 51	HC 58	HC 86	HC 132	HC 133	HC 266	HC 386	HC 4002	HC 4075	HC 4078	HC 7266
# Pins	SUMO	HODA	14	14	14	14	16	14	14	14	14	14	14
Single Device	CMOS	4078			144		•		2005	ROYAL	ist purpose	8 . 20	HCal
Dual Device								ets© R	Old svist	ioid na	nES beu	208	COPH
Triple Device Quad Device						•					eviser	notta bat	Medians
NAND NOR AND OR						•	•			•			
Exclusive OR Exclusive NOR AND-NOR AND-OR					•				•				•
2-Input 3-Input 4-Input 8-Input 13-Input			:	:	•	•		•	•	•	•		•
Schmitt-Trigger	Inputs											2111	
Open-Drain Outp	outs				12910								

These devices are identical in function and are different in pinout only: HC86 and HC386

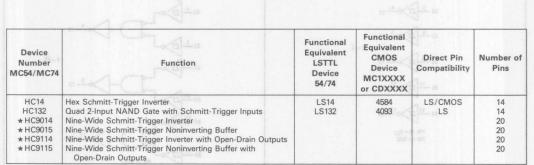




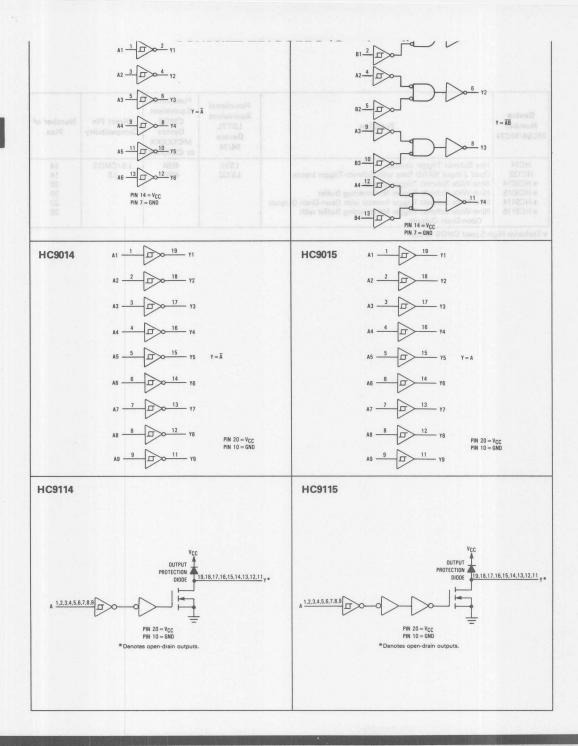




#### SCHMITT TRIGGERS



\* Exclusive High-Speed CMOS design

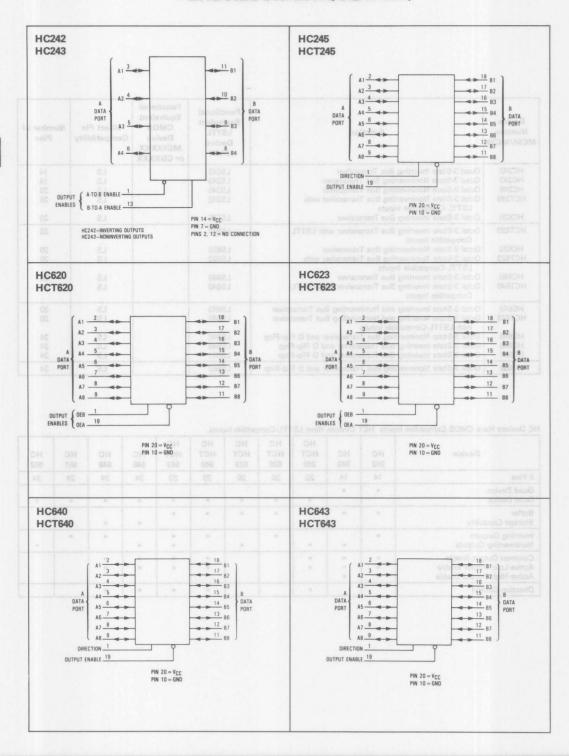


#### BUS TRANSCEIVERS

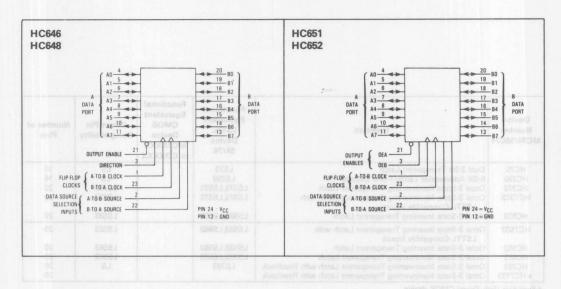
Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC242	Quad 3-State Inverting Bus Transceiver	LS242		LS	14
HC243	Quad 3-State Noninverting Bus Transceiver	LS243	-	LS	14
HC245	Octal 3-State Noninverting Bus Transceiver	LS245	lancara.	LS	20
HCT245	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS245		LS	20
HC620	Octal 3-State Inverting Bus Transceiver	LS620		LS	20
HCT620	Octal 3-State Inverting Bus Transceiver with LSTTL- Compatible Inputs	LS620	BROW OTWESTED	LS	20
HC623	Octal 3-State Noninverting Bus Transceiver	LS623		LS	20
HCT623	Octal 3-State Noninverting Bus Transceiver with	LS623		LS	20
HC640 HCT640	LSTTL-Compatible Inputs Octal 3-State Inverting Bus Transceiver Octal 3-State Inverting Bus Transceiver with LSTTL- Compatible Inputs	LS640 LS640		LS LS	20 20
HC643	Octal 3-State Inverting and Noninverting Bus Transceiver	LS643		LS	20
HCT643	Octal 3-State Inverting and Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS643		LS	20
HC646	Octal 3-State Noninverting Bus Transceiver and D Flip-Flop	LS646		LS	24
HC648	Octal 3-State Inverting Bus Transceiver and D Flip-Flop	LS648		LS	24
HC651	Octal 3-State Inverting Bus Transceiver and D Flip-Flop	LS651		LS	24
HC652	Octal 3-State Noninverting Bus Transceiver and D Flip-Flop	LS652		LS	24

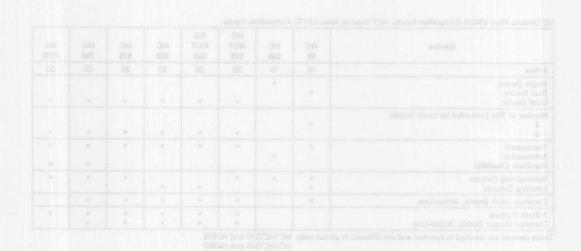
HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

Device	HC 242	HC 243	HC HCT 245	HC HCT 620	HC HCT 623	HC HCT 640	HC HCT 643	HC 646	HC 648	HC 651	HC 652
# Pins	14	14	20	20	20	20	20	24	24	24	24
Quad Device Octal Device	•	•									
Buffer Storage Capability	•	•	HC\$8	•	•	•	•			(\$44) •546	DI+
Inverting Outputs Noninverting Outputs	•			•		•	:		•	•	
Common Output Enable Active-Low Output Enable Active-High Output Enable	•	:	:						* · · · · · · · · · · · · · · · · · · ·		
Direction Control	-				111		•				



#### **BUS TRANSCEIVERS (Continued)**





Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC75	Dual 2-Bit Transparent Latch	LS75		LS	16
HC259	8-Bit Addressable Latch/1-of-8 Decoder	LS259		LS	16
HC373	Octal 3-State Noninverting Transparent Latch	LS373,LS573		LS373	20
НСТ373	Octal 3-State Noninverting Transparent Latch with LSTTL-Compatible Inputs	LS373,LS573		LS373	20
HC533	Octal 3-State Inverting Transparent Latch	LS533,LS563		LS533	20
HCT533	Octal 3-State Inverting Transparent Latch with LSTTL-Compatible Inputs	LS533,LS563		LS533	20
HC563	Octal 3-State Inverting Transparent Latch	LS533,LS563		LS563	20
HC573	Octal 3-State Noninverting Transparent Latch	LS373,LS573		LS573	20
HC793	Octal 3-State Noninverting Transparent Latch with Readback	LS793		LS	20
<b>★</b> HC7793	Octal 3-State Noninverting Transparent Latch with Readback				20

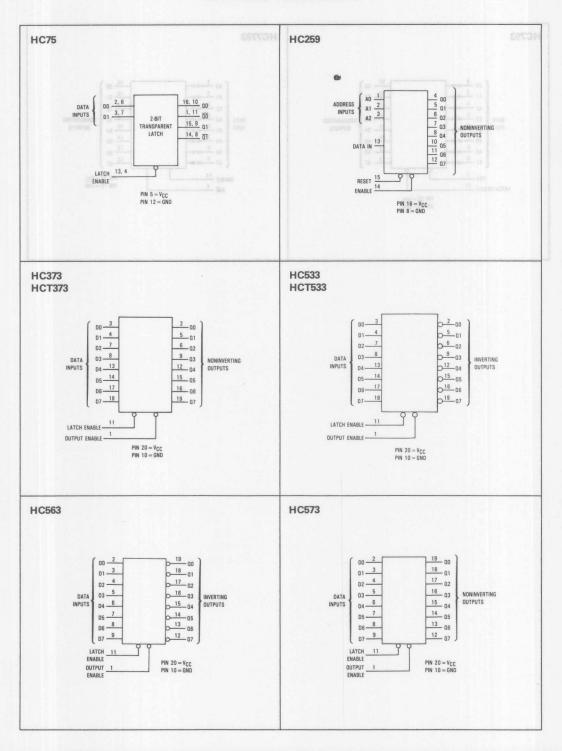
<sup>★</sup> Exclusive High-Speed CMOS design

HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

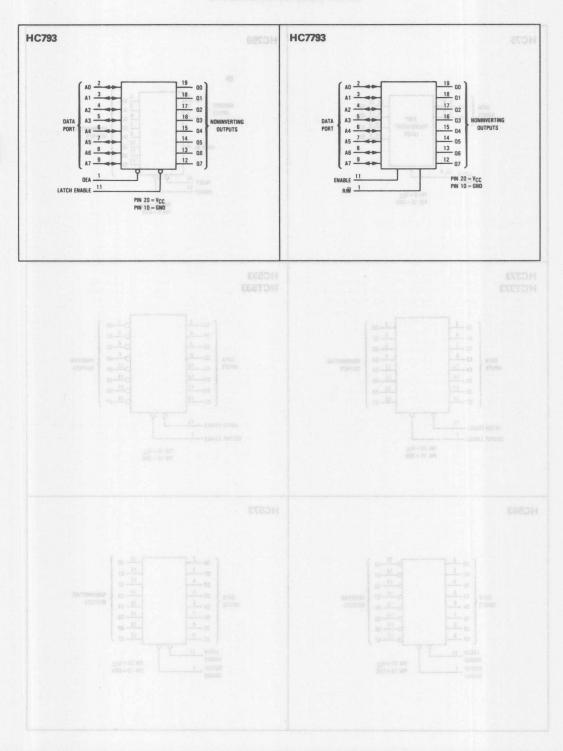
Device	HC 75	HC 259	HC HCT 373	HC HCT 533	HC 563	HC 573	HC 793	HC 7793
# Pins	16	16	20	20	20	20	20	20
Single Device Dual Device Octal Device	•	•						
Number of Bits Controlled by Latch Enable: 2 8								
Transparent Addressable Readback Capability	•		•	•	•	٠		:
Noninverting Outputs Inverting Outputs	:		•			•	•	٠
Common Latch Enable, Active-Low			•		•	•	•	
3-State Outputs Common Output Enable, Active-Low			:	:	:	:		•

These devices are identical in function and are different in pinout only: HC/HCT373 and HC573 HC/HCT533 and HC563

#### **LATCHES** (Continued)



2



#### FLIP-FLOPS

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX	Direct Pin Compatibility	Number o
4 1 4		34/74	or CDXXXX	Dinapole atomor	
HC73	Dual J-K Flip-Flop with Reset	LS73,LS73A,	*4027	LS73,	14
0 0		LS107,LS107A		LS73A	Noninvertin
HC74	Dual D Flip-Flop with Set and Reset	LS74,LS74A	*4013	LS	14
HC76	Dual J-K Flip-Flop with Set and Reset	LS76,LS76A,	*4027	LS76,	16
		LS112,LS112A	Englished 1	LS76A	Cummon.
HC107	Dual J-K Flip-Flop with Reset	LS73,LS73A,	*4027	LS107,	14
0 0		LS107,LS107A		LS107A	H normmout
HC109	Dual J-K Flip-Flop with Set and Reset	LS109,LS109A	*4027	LS	16
HC112	Dual J-K Flip-Flop with Set and Reset	LS76,LS76A,	*4027	LS112,	16
		LS112,LS112A		LS112A	wod-entra
HC113	Dual J-K Flip-Flop with Set	LS113,LS113A	*4027	LS	14
HC173	Quad 3-State D Flip-Flop with Common Clock and Reset	LS173,LS173A	4076	LS/CMOS	16
HC174	Hex D Flip-Flop with Common Clock and Reset	LS174	4174	LS/CMOS	16
HC175	Quad D Flip-Flop with Common Clock and Reset	LS175	4175	LS/CMOS	16
HC273	Octal D Flip-Flop with Common Clock and Reset	LS273	neticie lapute.	LS	20
HC374	Octal 3-State Noninverting D Flip-Flop	LS374,LS574		LS374	20
HCT374	Octal 3-State Noninverting D Flip-Flop with LSTTL- Compatible Inputs	LS374,LS574	99	LS374	20
HC534	Octal 3-State Inverting D Flip-Flop	LS534,LS564		LS534	20
HCT534	Octal 3-State Inverting D Flip-Flop with LSTTL-Compatible Inputs	LS534,LS564		LS534	20
HC564	Octal 3-State Inverting D Flip-Flop	LS534,LS564		LS564	20
HC574	Octal 3-State Noninverting D Flip-Flop	LS374,LS574		LS574	20
HC646	Octal 3-State Noninverting Bus Transceiver and D Flip-Flop	LS646		LS	24
HC648	Octal 3-State Inverting Bus Transceiver and D Flip-Flop	LS648		LS	24
HC651	Octal 3-State Inverting Bus Transceiver and D Flip-Flop	LS651	and the state of the second	LS	24
HC652	Octal 3-State Noninverting Bus Transceiver and D Flip-Flop	LS652		LS	24

<sup>\*</sup>Suggested alternative

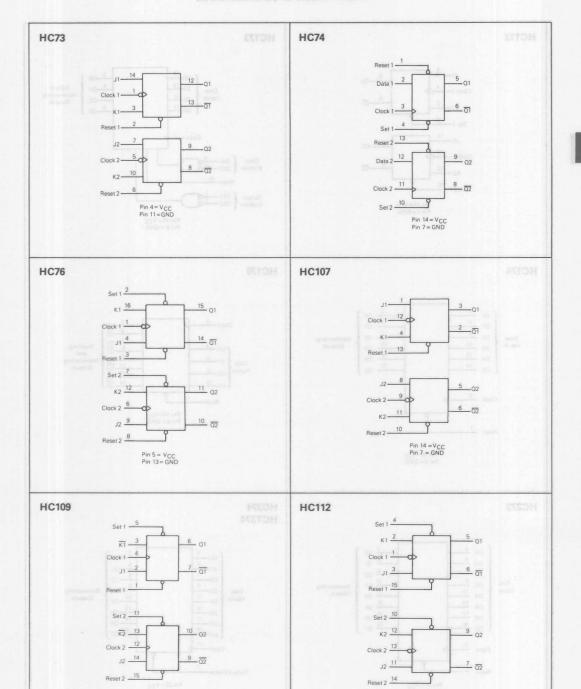
Device	HC 73	HC 74	HC 76	HC 107	HC 109	HC 112	HC 113	HC 173	HC 174	HC 175
# Pins	14	1 14	16	14	16	16	14	16	16 D	16
Туре	J-K	D	J-K	J-K	J-K	J-K	J-K	D		D
TION DOVIGO	Fuperic	•	•	٠	•	•	•	•	ero	re (i
Negative-Transition Clocking	rived .				puspeners *	•			MCZE	
Common, Active-Low Data Enables	arelali				3580	EL NEW	political R	Note Tour	E)	DH
Noninverting Outputs Inverting Outputs	* 12 M/TS		:	• 19	up/Natura	red • this	qu#-qi	B O IsuC	74.	3H .
3-State Outputs Common, Active-Low Output Enables				150	21 000 s	G dilas		to a land	50	OH.
Common Reset Active-Low Reset Active-High Reset				•189	A to a a	2 ren	Pip Pa	Si-L hard	180	SH:
Active-Low Set	eus reu	•				•	•			
Transceiver Direction Control	L\$113,L\$	Stages S	tions also	13 nom	and relative	40P-0	R Q otal	Art lead See head	13	OH OH

HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

	Device		HC 273	HCT 374	HC HCT 534	HC 564	HC 574	HC 646	HC 648	HC 651	HC 652
# Pins	1632.)	534,1,558d	20	20	20	20	20	24	24	24	24
Туре			D.	D	D	D	D	D	D	D	D
Dual Device Quad Device Hex Device Octal Device	e	\$74,1.5674 1.5646 1.5848	2	Pip-Flob	bea 190 Ind D Fil		G getha ual getha grapa grapa	e Nonins o Vonins u Insura	eral 3-Stea steal 3-Stea steal 3-Stea	0 8	HOB HOB
Common C		19057		- GDFI-	R G bri	19/10/990	H 888 B	attended a	28 J. 185		12.025
Negative-Tr	ransition Clocking			on-ga a	bing you		e and a	·	pret a Stra prive	mulis be	Lating anta
Common, A	Active-Low Data Enables										
Noninvertin Inverting O			•				•	•			
3-State Out Common, A	tputs Active-Low Output Enables			:	:	:	:	:		•	
Common R Active-Low Active-High	Reset										
Active-Low	Set										
Transceiver Direction C								:	:	•	•

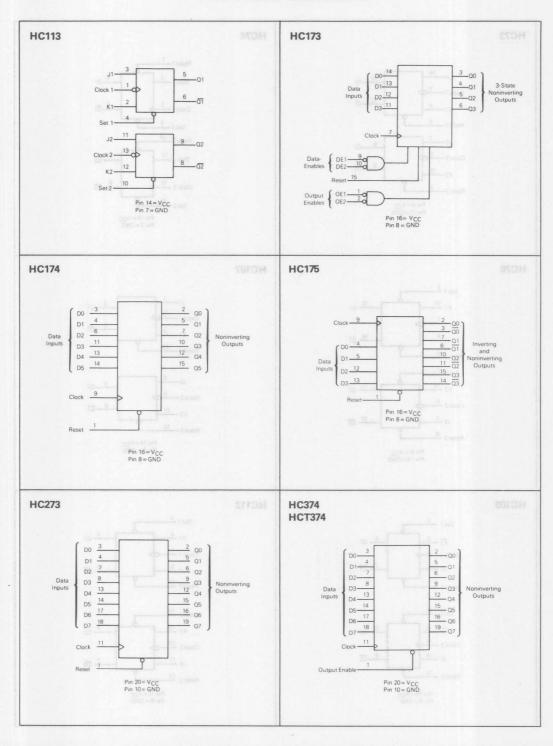
These devices are identical in function and are different in pinout only: HC73 and HC107
HC76 and HC112
HC374 and HC574
HC534 and HC564

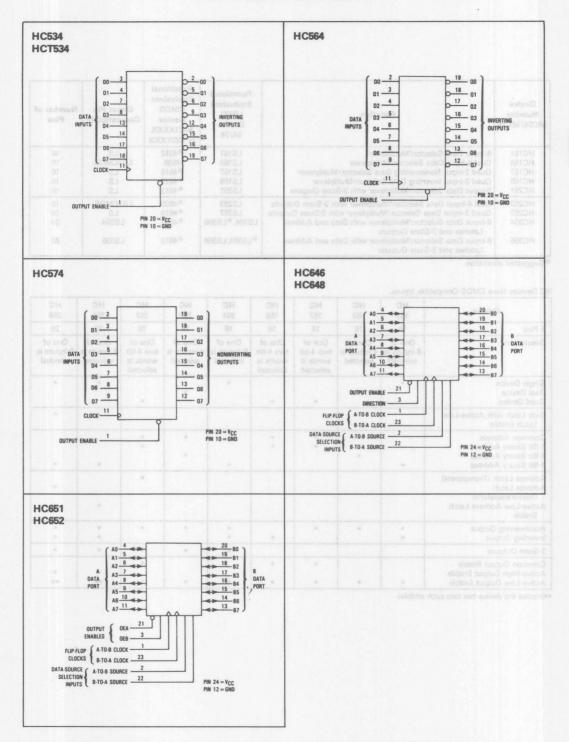
# FLIP-FLOPS (Continued)



Pin 16 = VCC Pin 8 = GND

Pin 16 = VCC Pin 8 = GND





Device Number MC54/MC74	Function    10   11   12   13   13   14   15   15   15   15   15   15   15	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC151	8-Input Data Selector/Multiplexer	LS151	*4512	LS	16
HC153	Dual 4-Input Data Selector/Multiplexer	LS153	4539	LS/CMOS	16
HC157	Quad 2-Input Noninverting Data Selector/Multiplexer	LS157	*4519	LS	16
HC158	Quad 2-Input Inverting Data Selector/Multiplexer	LS158	*4519	LS	16
HC251	8-Input Data Selector/Multiplexer with 3-State Outputs	LS251	*4512	LS	16
HC253	Dual 4-Input Data Selector/Multiplexer with 3-State Outputs	LS253	*4539	LS/CMOS	16
HC257	Quad 2-Input Data Selector/Multiplexer with 3-State Outputs	LS257	*4519	LS	16
HC354	8-Input Data Selector/Multiplexer with Data and Address Latches and 3-State Outputs	LS354,*LS356	*4512	LS354	20
HC356	8-Input Data Selector/Multiplexer with Data and Address Latches and 3-State Outputs	*LS354,LS356	*4512	LS356	20

<sup>\*</sup>Suggested alternative

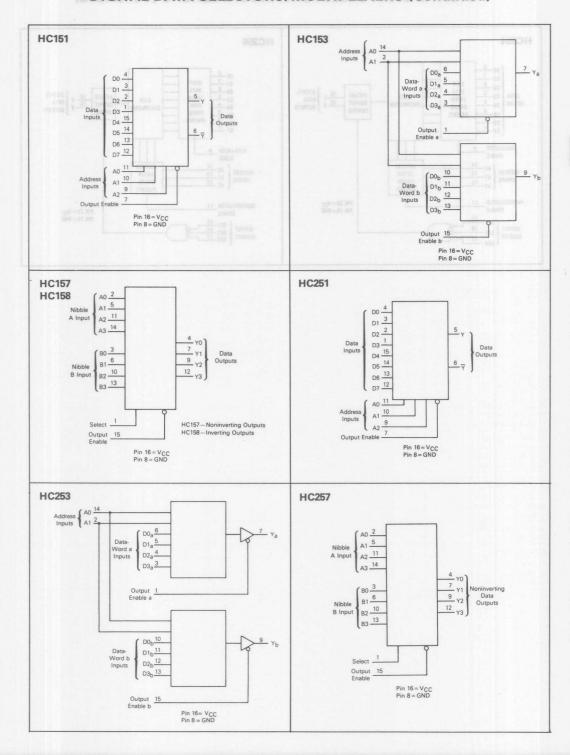
### HC Devices Have CMOS-Compatible Inputs.

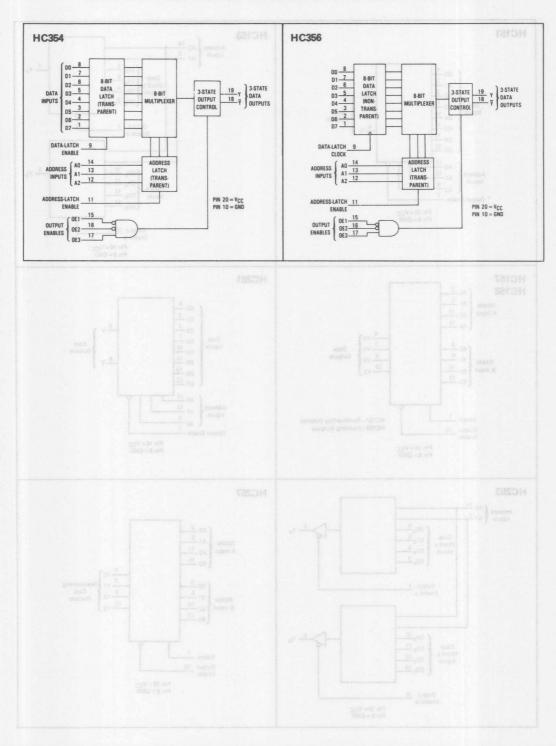
ı	Device	HC 151	HC 153	HC 157	HC 158	HC 251	HC 253	HC 257	HC 354	HC 356
# Pins	CH . M	16	16	16	16	16	16	16	20	20
Description	50 - 41 00 - 12 00 00 00 00 00 00 00 00 00 00 00 00 00	One of 8 inputs is selected	One of 4 inputs is selected	One of two 4-bit words is selected	One of two 4-bit words is selected	One of 8 inputs is selected	One of 4 inputs is selected	One of two 4-bit words is selected	One of 8 inputs is selected	One of 8 inputs is selected
Single Device Dual Device Quad Device		Lis-s	SUA TO BE			•	10 ET		1	•
Data Latch w Latch Enab	vith Active-Low ble		S (A DES GLOS SE (B TERA CLOS	50.4515 50.15				9	- Trespins	•
Common Add 1-Bit Binary A 2-Bit Binary A 3-Bit Binary A	Address Address	15 3	NUCE AST B 3	DAT THE LASE (LASSON	:	- 080 - 51 M	•	•	518663	869700
Address Late (Non-transp								•	•	10851
Noninverting Inverting Out		:	•	•		:	•	•	:	:
3-State Outpu	uts					7 (0 <b>-</b> 0 - 0 - 0 - 0 - 0 - 0 - 0 - 0 - 0 - 0		•	day.	•
	tput Enable Output Enable Output Enable	•			AT ME	23 - 82 - 43 22 - 23 - 43 23 - 31 - 43		•		

<sup>••</sup>implies the device has two such enables

# 2

# DIGITAL DATA SELECTORS/MULTIPLEXERS (Continued)





# DECODERS/DEMULTIPLEXERS/DISPLAY DRIVERS

Device	BCD Address of Highest Input	Functional Equivalent		Functional Equivalent CMOS	Direct Pin	Number of	
Number MC54/MC74	9	Function		LSTTL Device 54/74	Device MC1XXXX or CDXXXX	Compatibility	Pins
HC42 HC137 HC138 HC139 HC147	1-of-10 Decoder 1-of-8 Decoder/Demul- 1-of-8 Decoder/Demul- Dual 1-of-4 Decoder/D Decimal-to-BCD Encoder	tiplexer emultiplexer	dress Latch	LS42 LS137 LS138 LS139 LS147	*4028 *4028 *4028 4556	LS LS LS/CMOS LS	16 16 16 16 16
HC154 * HC237 HC259 HC4511	1-of-16 Decoder/Demul 1-of-8 Decoder/Demul 8-Bit Addressable Late BCD-to-Seven-Segmer 1-of-16 Decoder/Demu	tiplexer with Add h/1-of-8 Decode nt Latch/Decode	r/Display Driver	LS154,*LS159 *LS137 LS259 *LS47,*LS48, *LS49 *LS154,*LS159	*4515 *4028 4511 4514.	LS LS CMOS	24 16 16 16
HC4514 HC4543	BCD-to-Seven-Segmer for LCDs			*LS47,*LS48, *LS49	*4515 4543	CMOS	16

<sup>\*</sup>Suggested alternative

Prince Prescription Control Co

<sup>★</sup> Exclusive High-Speed CMOS design

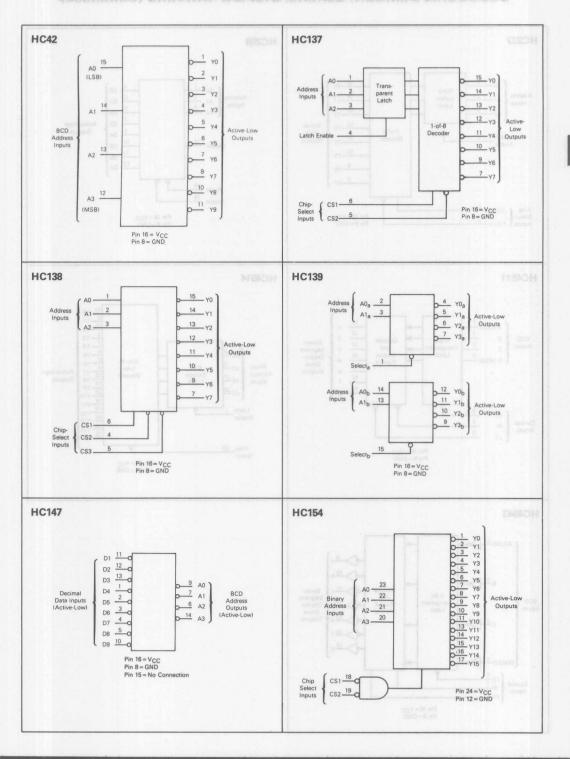
Device	HC 42	HC 137	HC 138	HC 139	HC 147	HC 154
# Pins	16	16	16	16	16	24
Input Description	BCD Address	3-Bit Binary Address	3-Bit Binary Address	2-Bit Binary Address	Any Combination of 9 Inputs	4-Bit Binary Address
Output Description	One of 10	One of 8	One of 8	One of 4	BCD Address of Highest Input	One of 16
Single Device Dual Device	Sevice Vincerous	terred .	•	roitsnut	•	SELMOTE
Address Input Latch Active-High Latch Enable Active-Low Latch Enable	MXXXXGG vo	2987	dotte I acce		-10 December	HQ42 1-0
Active-Low Inputs	8500.00	LETER		reseals	dumed\neocotic	1C138 1=0
Active-Low Outputs Active-High Outputs	4558	CALETT .	•	Jak • Galukin	Depart of Brook	C147
Active-Low Output Enable Active-High Output Enable	8184 8818 8556#	plena.	right, June	Disk of Purers	- 16 Decoder/Dampt - B Decoder/Dampt	0-1 **SOH
Active-Low Reset	1178 200	14.7897.4	Saylor Driver	nboseG\rists.l	J-m-Savin-Segmen	58 -H&O
Active-Low Blanking Input Active-High Blanking Input	,ar89 4514,	12 YELS 1.8 PS 1.5	riore. Lessi	bA dilw revolgit	18 Decader/Densit	04574 1-0
Active-Low Lamp-Test Input	53 BP					00 600
Phase Input (for LCD's)	200	01019	State Angles		#00.1 v	

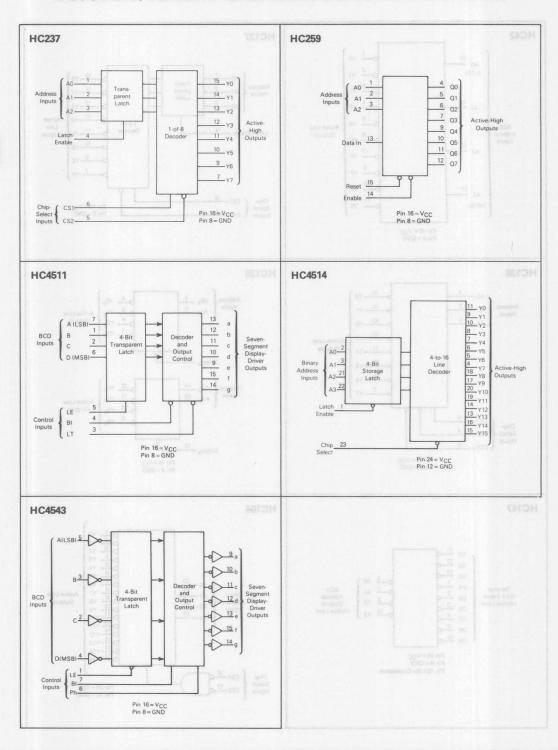
### HC Devices Have CMOS-Compatible Inputs

Device	HC 237	HC 259	HC 4511	HC 4514	HC 4543
# Pins	16	16	16	24	16
Input Description	3-Bit Binary Address	3-Bit Binary Address	BCD Data	4-Bit Binary Address	BCD Data
Output Description	One of 8	One of 8	7-Segment Display	One of 16	7-Segment Display
Single Device Dual Device	•	•	•	•	•
Address Input Latch Active-High Latch Enable Active-Low Latch Enable	:		:		:
Active-Low Inputs					
Active-Low Outputs Active-High Outputs					
Active-Low Output Enable Active-High Output Enable	•	•		•	
Active-Low Reset					
Active-Low Blanking Input Active-High Blanking Input			•		
Active-Low Lamp Test Input					
Phase Input (for LCD's)					•

# 2

# DECODERS/DEMULTIPLEXERS/DISPLAY DRIVERS (Continued)





# ANALOG SWITCHES/MULTIPLEXERS/DEMULTIPLEXERS

Device Number MC54/MC74	8	Function		Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC4016 HC4051 HC4052 HC4053 HC4066	C4051 8-Channel Analog Multiplexer/Demultiplexer C4052 Dual 4-Channel Analog Multiplexer/Demultiplexer C4063 Triple 2-Channel Analog Multiplexer/Demultiplexer C4066 Quad Analog Switch/Multiplexer/Demultiplexer				4016,4066 4051 4052 4053 4066,4016	CMOS CMOS CMOS CMOS CMOS	14 16 16 16 16
*HC4316 *HC4351	Separate Analog a	Quad Analog Switch/Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies B-Channel Analog Multiplexer/Demultiplexer with			*4016 *4051	ry Address pry Address tub with Active- witch Engble	16 20
★ HC4352 ★ HC4353	Dual 4-Channel Anal Address Latch Triple 2-Channel Ana Address Latch				*4052 *4053	nte English Igh English colog and Conte	20

<sup>\*</sup>Suggested alternative ★ High-Speed CMOS design only

ASSE  4 Independently Connolled Switching China a Soperste Analog Lover Power Supply  **  **  **  **  **  **  **  **  **	ASTE 4281  ASTE ACIDITATE Committed Subsection of 8 Switteries Subsection Place a Separate Power Subsyly Power Subsyly  **The an Address **The analysis and address an	ASTR Address A 2-Bit Address Commoded Selecte One of 6 Se

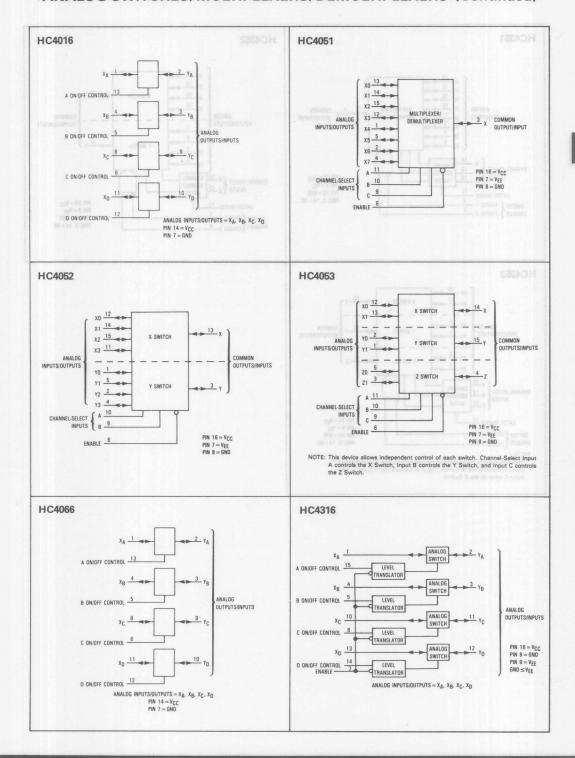
Device		HC 4016	HC 4051	HC 4052	HC 4053	HC 4066
# Pins		14	16	16	16	14
Description		4 Independently Controlled Switches	A 3-Bit Address Selects One of 8 Switches	A 2-Bit Address Selects One of 4 Switches	A 3-Bit Address Selects Varying Combinations of the 6 Switches	4 Independently Controlled Switches
Single Device Dual Device Triple Device Quad Device		Functions Equivalent LSTIL Devices	•	Function	•	Davice Number MCS4*4G78
1-to-1 Multiplexing 2-to-1 Multiplexing	2000003-16	9E/38 •				•
4-to-1 Multiplexing 8-to-1 Multiplexing				s/Muldpl∙ser/Dem hiltiplener/Demulto		
Active-High ON/OFF Contro	ol School	•	ABREIGHTEN Verwalei ift von	CA vaccional field to la	est 4 Champion Aug	нофия т
Common Address Inputs	8104,8804		texelostu	V/Mudipreser/Dere	ood Anseig Switch	HC4085
2-Bit Binary Address 3-Bit Binary Address Address Latch with Active-I	ow Latch Enable		selfqual	V Muhipheser / Dani ind Digital Power I Wholever / December	ead Analog Switch Separate Analog to Channel Analog to	# HC4316 C
Common Switch Enable Active-Low Enable Active-High Enable	28055		•	aCI\vancale,statA go	rium le caretob A.	# HC4352 E
Separate Analog and Contro Power Supplies	ol Reference		•	EL VIOLUNI SININ EIN	dotal corpus	ALCOHA I
Switched Tubs (for RON an Improvement)	d Prop. Delay				PUS design only	a High Losed CN

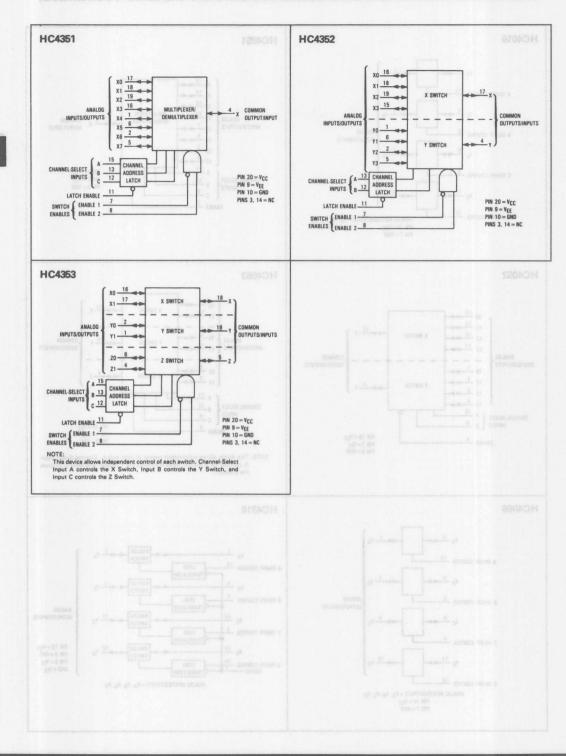
### HC Devices Have CMOS-Compatible Inputs.

Device	HC 4316	HC 4351	HC 4352	HC 4353
# Pins	16	20	20	20
Description	4 Independently Controlled Switches (Has a Separate Analog Lower Power Supply)	A 3-Bit Address Selects One of 8 Switches (Has an Address Latch)	A 2-Bit Address Selects One of 4 Switches (Has an Address Latch)	A 3-Bit Address Selects Varying Combinations of the 6 Switches (Has an Address Latch)
Single Device Dual Device Triple Device Quad Device		•	•	•
1-to-1 Multiplexing 2-to-1 Multiplexing 4-to-1 Multiplexing 8-to-1 Multiplexing	•	•	•	٠
Active-High ON/OFF Control	•			
Common Address Inputs 2-Bit Binary Address 3-Bit Binary Address Address Latch with Active-Low Latch Enable		:	•	•
Common Switch Enable Active-Low Enable Active-High Enable	•	•	•	•
Separate Analog and Control Reference Power Supplies	•	•	•	•
Switched Tubs (for R <sub>ON</sub> and Prop. Delay Improvement)				

<sup>••</sup>implies the device has two such enables

## ANALOG SWITCHES/MULTIPLEXERS/DEMULTIPLEXERS (Continued)





# SHIFT REGISTERS

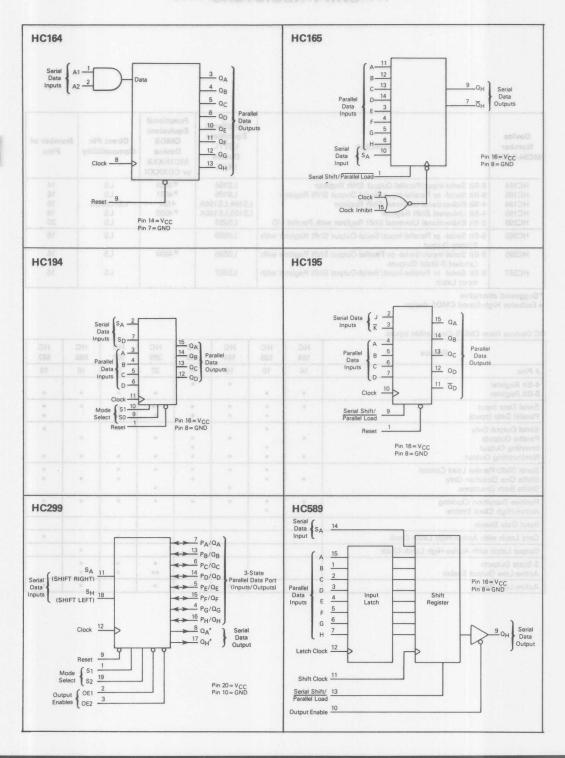
Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC164 HC165 HC194 HC195 HC299	8-Bit Serial-Input/Parallel-Output Shift Register 8-Bit Serial- or Parallel-Input/Serial-Output Shift Register 4-Bit Bidirectional Universal Shift Register 4-Bit Universal Shift Register 8-Bit Bidirectional Universal Shift Register with Parallel I/O	LS164 LS165 LS194,LS194A LS195,LS195A LS299	*4034 *4021 4194 *4035	LS LS LS/CMOS LS LS	14 16 16 16 20
HC589	8-Bit Serial- or Parallel-Input/Serial-Output Shift Register with 3-State Output	LS589		LS	16
HC595 HC597	8-Bit Serial-Input/Serial- or Parallel-Output Shift Register with Latched 3-State Outputs 8-Bit Serial- or Parallel-Input/Serial-Output Shift Register with Input Latch	LS595 LS597	*4034	LS LS	16 16

HC Devices Have CMOS-Compatible In

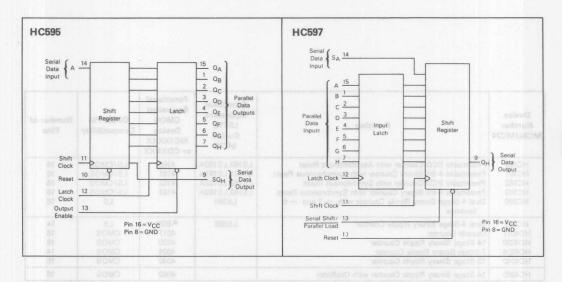
Device	HC	HC	HC	HC	HC	HC	нс	HC
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	164	165	194	195	299	589	595	597
# Pins	14	16	16	16	20	. 16	16	16
4-Bit Register 8-Bit Register			•	•		9		
Serial Data Input Parallel Data Inputs		:			•			:
Serial Output Only Parallel Outputs Inverting Output Noninverting Output				Sied vid vid				
Serial Shift/Parallel Load Control Shifts One Direction Only Shifts Both Directions		:		:		:		:
Positive-Transition Clocking Active-High Clock Enable	HC688	:	•	•	•	•	•	czas
Input Data Enable	1.0							
Data Latch with Active-High Latch Clock	J. topol:		10	1	-			
Output Latch with Active-High Latch Clock	1.5			a Land			•	
3-State Outputs Active-Low Output Enable		etes2	12	nga Lunga Lunga Lunga		:	0.	
Active-Low Reset	10000	SetVanda CTV					•	

<sup>\*</sup>Suggested alternative

\*Exclusive High-Speed CMOS design



# SHIFT REGISTERS (Continued)





Device Number MC54/MC74	Function Section Secti	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC160	Presettable BCD Counter with Asynchronous Reset	LS160,LS160A	4160	LS/CMOS	16
HC161	Presettable 4-Bit Binary Counter with Asynchronous Reset	LS161,LS161A	4161	LS/CMOS	16
HC162	Presettable BCD Counter with Synchronous Reset	LS162,LS162A	4162	LS/CMOS	16
HC163	Presettable 4-Bit Binary Counter with Synchronous Reset	LS163,LS163A	4163	LS/CMOS	16
HC390	Dual 4-Stage Binary Ripple Counter with ÷ 2 and ÷ 5 Sections	LS390		LS	16
HC393	Dual 4-Stage Binary Ripple Counter	LS393	*4520	LS	14
HC4017	Decade Counter		4017	CMOS	16
HC4020	14-Stage Binary Ripple Counter		4020	CMOS	16
HC4024	7-Stage Binary Ripple Counter		4024	CMOS	14
HC4040	12-Stage Binary Ripple Counter		4040	CMOS	16
HC4060	14-Stage Binary Ripple Counter with Oscillator		4060	CMOS	16

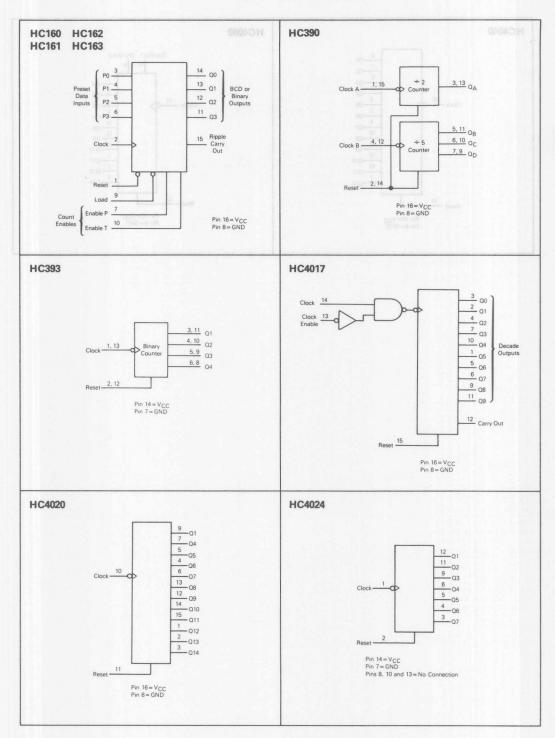
<sup>\*</sup>Suggested alternative

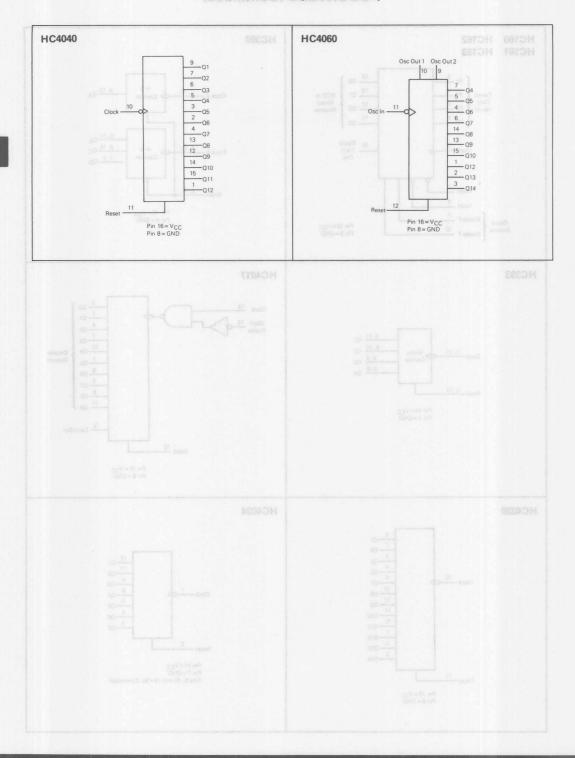
### HC Devices Have CMOS-Compatible Inputs

Device	HC 160	HC 161	HC 162	HC 163	HC 390	HC 393	HC 4017	HC 4020	HC 4024	HC 4040	HC 4060
# Pins	16	16	16	16	16	14	16	16	14	16	16
Single Device Dual Device		•	•	•			•	•	•	•	•
Ripple Counter Number of Ripple Counter Internal Stages Number of Stages with Available Outputs					• 4 4	• 4 4		• 14 12	• 7 7	• 12 12	• 14 10
Count Up	•	•	•	•	•	•	•	•	•	•	•
4-Bit Binary Counter BCD Counter Decimal Counter		•	•	•		•					
Separate ÷ 2 Section Separate ÷ 5 Section											
On-Chip Oscillator Capability											•
Positive-Transition Clocking Negative-Transition Clocking Active-High Clock Enable Active-Low Clock Enable	•	•		•	•	•	:	•	•	•	
Active-High Count Enable	••	••	••	••							
Active-High Reset	•	•	•	•	•	•	•		•	•	•
4-Bit Binary Preset Data Inputs BCD Preset Data Inputs Active-Low Load Preset	:	:		:							
Carry Output											

<sup>••</sup>implies the device has two such enables

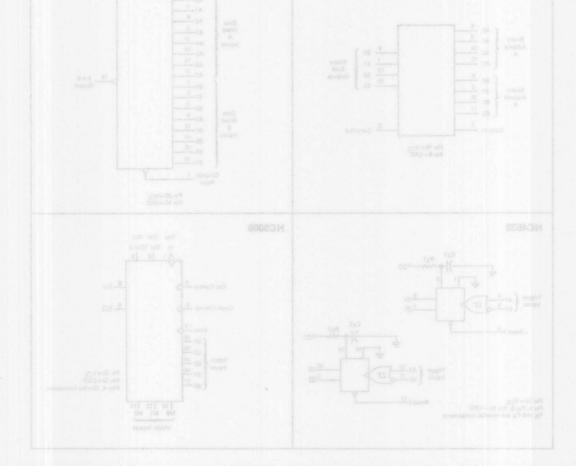
# **COUNTERS** (Continued)

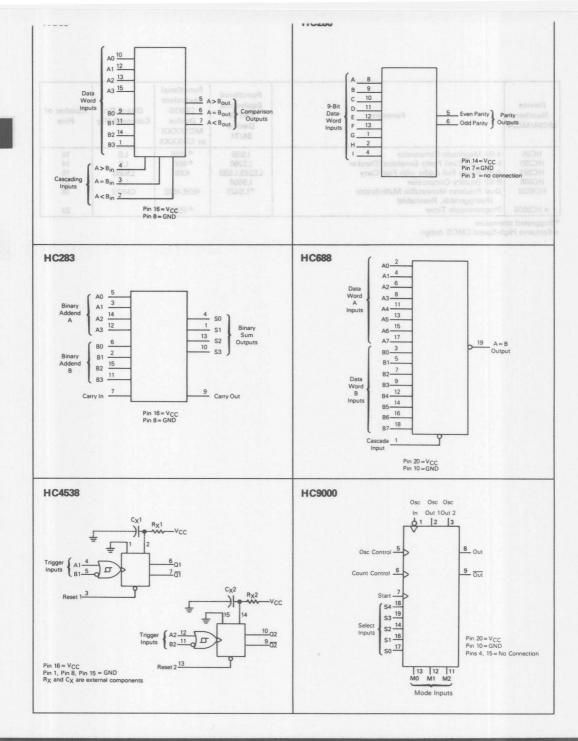




Device Number MC54/MC74	Function Stands	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC85	4-Bit Magnitude Comparator	LS85	*4585	LS	16
HC280	9-Bit Odd/Even Parity Generator/Checker	LS280	*4531	LS	14
HC283	4-Bit Binary Full Adder with Fast Carry	LS283,LS83	4008	LS283	16
HC688	8-Bit Equality Comparator	LS688		LS	20
HC4538	Dual Precision Monostable Multivibrator (Retriggerable, Resettable)	*LS423	4538,4528	CMOS	16
★HC9000	Programmable Timer		*4536	69	20

<sup>\*</sup>Suggested alternative
\*Exclusive High-Speed CMOS design





The "Better" Program 3

The "Better" Program E

# The "BETTER" Program

Motorola's "BETTER" program was developed to provide improved levels of reliability for standard commercial products.

The "BETTER" program is offered on High-Speed CMOS in dual-in-line ceramic and plastic packages, as well as in SOIC packages.

Motorola standard commercial integrated circuits are manufactured under stringent in-process controls and quality inspections combined with the industry's finest outgoing quality inspections. The "BETTER" program offers three levels of extra processing, each tailored to meet different user needs at nominal costs.

### LEVEL I - SUFFIX "S"

In addition to standard processing, "BETTER" Level I product is 100% subjected to temperature cycling (10 cycles,  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ) and also receives a high temperature functional and D.C. parametric test at the maximum rated temperature.

### LEVEL II - SUFFIX "D"

"BETTER" Level II product is standard product which receives static burn-in performed according to MIL-STD-883B. A 2% P.D.A. (Percent Defective Allowed) fallout is permissible; if a greater fallout occurs, the lot is sent through another burn-in cycle. The second P.D.A. is 0.5%; parts failing this criteria are considered unmarketable.

### LEVEL III - SUFFIX "DS"

Level III is a combination of "BETTER" Levels I and II. Although Motorola offers temperature cycling in its "BETTER" Level I and III product, reliability studies indicate that High-Speed CMOS routinely passes stresses of 1000 cycles ( $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ) due to improvements in wafer fabrication and assembly operations. For more information the reader is referred to Chapter 6 "Reliability", the section entitled "Thermal Cycling".

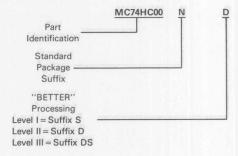
High temperature testing can also be considered unnecessary, for the 25°C test limits for all parametric tests are guard-banded to insure that device performance at the maximum recommended temperature conforms to the guaranteed limits.

High-Speed CMOS devices screened to "BETTER" Level II are recommended for highly complex circuit boards where board rework is difficult and costly. Burn-in eliminates the majority of infant mortalities, thus increasing the degree of board confidence. See Chapter 6, "Reliability" for more information on the overall reliability of High-Speed CMOS. Specifically, refer to the section entitled "Life Test" for information on the effects of burn-in on High-Speed CMOS.

### PART ORDERING

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

### **HOW TO ORDER**



Mosorola's "BETTER" program was developed to proving mproved levels of reliability for standard conversely products.

The "BETTER program is offered on reign-speed union in dual-in-line occurric and plastic packages, as well as in SOIC and testing.

Motorola standard commercial integrated circuits are man unactured under stringent in process controls and quality inspections combined with the industry's linear outgoing number inspections. The "BETTER" program offers those levels of extra processing, each tailored to meet different user partial coasts.

### LEVEL I - SUFFIX "S"

In addition to standard processing, "BETTER" Level product is 100% subjected to temperature cycling 110 cycles, —85°C to +150°C and also species a high temperature temperature that and D.C. parametric test at the maximum rated discoverature.

### "O" XERUS - IL JAVA

"SETTER" Leval if product is franded product which receives static furn-in performed according to Mit. STD 88390.

A 2% P.D.A. (Percent Datective Allervied) fellout is permissible; if a greater failout occurs, the let is sent through another burner; cycle. The second P.D.A. is 0.5%; parts failing this cheers are considered unreakteable.

### TEVEL III - SUFFIX "DS"

Level III is a combination of "SEFTER" Levels I and it. Although Motorcia offers remperature cycling in its "SEFTER" Level I and fit product, reliability studies indicate that High Speed CMOS toutinely passes stresses of 1000 cycles I – 65°C to + 150°C) due to improvements in water fabrication and satematicy operations. For more information the reader is referred to Chapter 6 "Reliability", the section entitled "Thermal Content."

High temperature tasting can also be considered unnease sary, for the 25°C test limits for all parametric tests are guardbinded to fraum that device performance at the maximum accommended temperature conforms to the guaranteed limits.

trigh Speed CMOS devices screened to "RETTER" Level II are monumended for highly complex circuit beards where board rework is difficult and costly. Burn-in similares the majority of infant mertalities, thus increasing the degree of board confidence. See Chapter 6, "ReSebility" for more intermition on the overall reliability of High-Speed CMOS. Special set to the section entitled "Life Test" for information on the actions entitled "Life Test" for information on the affaces of burn-in or High-Speed CMOS.

### DIMERSORO TRAF

The Standard Motorcia pair number with the corresponding SETTER" settix can be ordered from your local authorized Motorcia distributor or Motorcia sales of local. "SETTER" proing will be quoted as an adder to associate commercial product

### SOW TO ORDER

Part
Identification
Rendard
Standard
Suffix
Package
Suffix
Peckage
Peccasing
Retreet I = Suffix S
Level II = Suffix S
Level III = Suffix S
Level III = Suffix S

# Introduction Handling Presentions Power Supply Slaing Striery Systems Cpp Power Calculation Apples State Outputs Open Drain Outputs Hoput Outputs Supply Voltage Effects on Drive Current and Propagation Delay Supply Voltage Effects on Drive Current and Propagation Delay Typical Parametric Values Descripting Capacitors Apples Apples Descripting Capacitors Apples Ap

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CMOS devices have been used for many years in applications where the primary concerns were low power consumption, wide power-supply range, and high noise immunity. However, metal-gate CMOS (MC14000 series) is too slow for many applications. Applications requiring high-speed devices, such as microprocessor memory decoding, had to go to the faster families such as LSTTL. This meant sacrificing the best qualities of CMOS. The next step in the logic evolution was to introduce a family of devices that were fast enough for such applications, while retaining the advantages of CMOS. The results of this change can be seen in Table 1 where HSCMOS devices are compared to standard (metal-gate) CMOS, LSTTL, and ALS.

The Motorola CMOS evolutionary process shown in Figure 1 indicates that one advantage of the silicon-gate process is device size. The High-Speed CMOS (HSCMOS) device is about half the size of the metal-gate predecessor, yielding significant chip area savings. The silicon-gate process allows smaller gate or channel lengths due to the self-aligning gate feature. This process uses the gate to define the channel during processing, eliminating registration errors and, therefore, the need for gate overlaps. The elimination of the gate overlap significantly lowers the gate capacitance, resulting in higher speed capability. The smaller gate length also results in higher drive capability per unit gate width, ensuring more efficient use of chip area. Immunity enhancements to electrostatic discharge (ESD) damage and latch up are ongoing. Precautions should still be taken, however, to guard against electrostatic discharge and latch up.

Motorola's High-Speed CMOS family has a broad range of functions from basic gates, flip-flops, and counters to buscompatible devices. The family is made up of devices that are identical in pinout and are functionally equivalent to LSTTL devices, as well as the most popular metal-gate devices not available in TTL. Thus, the designer has an excellent alternative to existing families without having to become familiar with a new set of device numbers.

### INTRODUCTION HANDLING PRECAUTIONS

High-Speed CMOS devices, like all MOS devices, have an insulated gate that is subject to voltage breakdown. The gate oxide for HSCMOS devices breaks down at a gate-source potential of about 100 volts. All device inputs are protected by a resistor-diode network (Figure 2). Using the test setup shown in Figure 3, the inputs typically withstand a >2 kV discharge.

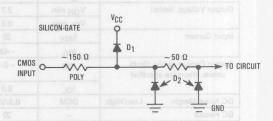


Figure 2. Input Protection Network

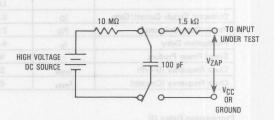
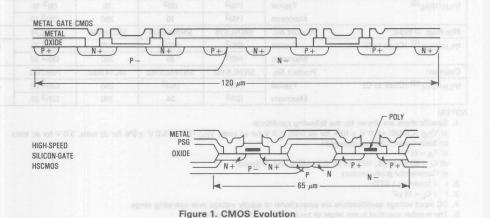


Figure 3. Electrostatic Discharge Test Circuit



MOTOROLA HIGH-SPEED CMOS LOGIC DATA

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		4		

Characteristic	Symbol	uspi -on	TL SU MINOS VI	CM	ortw.	
		bloo LS	ALS	MC14000	Hi-Speed	Unit
Operating Voltage Range	VCC/EE/DD	5±5%	5±5%	3.0 to 18	2.0 to 6.0	V
Operating Temperature Range	TA	0 to +70	0 to +70	-40 to +85	-55 to +125	°C
Input Voltage (limits)	V <sub>IH</sub> min	2.0	2.0	3.54	3.54	V
	V <sub>IL</sub> max	0.8	0.8	1.54	1.04	V
Output Voltage (limits)	V <sub>OH</sub> min	2.7	2.7	V <sub>DD</sub> -0.05	V <sub>CC</sub> -0.1	V
	V <sub>OL</sub> max	0.5	0.5	0.05	0.1	V
Input Current	INH	20	20	+0.3	± 1.0	μΑ
月亭	INL	-400	-200	10.5	±1.0	210
Output Current @ VO (limit) unless otherwise specified	OH	-0.4 <sub>2019</sub>	-0.4	-2.1 @ 2.5 V	-4.0 @ V <sub>CC</sub> -0.8 V	mA
	loL	8.0	8.0	0.44 @ 0.4 V	4.0 @ 0.4 V	mA
DC Noise Margin Low/High	DCM	0.3/0.7	0.3/0.7	1.454	0.90/1.354	V
DC Fanout		20	20	>50(1)2	50(10)2	nsari

Speed/Power Characteristics (1) (All Typical Ratings)

Characteristic	Combat.	П	L swintered	CN		
Characteristic	Symbol	LS	ALS	MC14000	Hi-Speed	Unit
Quiescent Supply Current/Gate	IG	0.4	0.2	0.0001	0.0005	mA
Power/Gate (Quiescent)	PG	2.0	1.0	0.0006	0.001	mW
Propagation Delay	tp	9.0	7.0	125	8.0	ns
Speed Power Product	-HOAT JON	18	7.0	0.075	0.01	pJ
Clock Frequency (D-F/F)	f <sub>max</sub>	33	35	4.0	40	MHz
Clock Frequency (Counter)	f <sub>max</sub>	40	45	5.0	150 - 40 mai	MHz

### Propagation Dolay (1)

Characteristic		BVI	TL <sup>ISHE INTERSOXS</sup>	CN	M BICINI	
		LS	ALS	MC14000	Hi-Speed	Unit
Gate, NOR or NAND:	Product No.	SN74LS00	SN74ALS00	MC14001B	74HC00	-
tPLH/tPHL <sup>(5)</sup>	Typical	(10)3	(5)3	25	(8)3 10	ns
	Maximum	(15)3	10	250	(15)3 20	1
Flip-Flop, D-type:	Product No.	SN74LS74	SN74ALS74	MC14013B	74HC74	-
tPLH/tPHL(5) (Clock to Q)	Typical	(25)3	(12)3	175	(23)2 25	ns
	Maximum	(40)3	20	350	(30)3 32	
Counter:	Product No.	SN74LS163	SN74ALS163	MC14163B	74HC163	_
tPLH/tPHL <sup>(5)</sup> (Clock to Q)	Typical	(18)3	(10)3	350	(20)3 22	ns
	Maximum	(27)3	24	700	(27)3 29	

### NOTES:

- 1. Specifications are shown for the following conditions:
  - a)  $V_{DD}$  (CMOS) = 5.0 V  $\pm$  10% for dc tests, 5.0 V for ac tests;  $V_{CC}$  (TTL) = 5.0 V  $\pm$ 5% for dc tests, 5.0 V for ac tests
  - b) Basic Gates: LS00 or equivalent

  - c) T<sub>A</sub> = 25°C d) C<sub>L</sub> = 50 pF (ALS, HC), 15 pF (LS, 14000 and Hi-Speed)
  - e) Commercial grade product
- 2. ( ) fanout to LSTTL
- 3. ( ) C<sub>L</sub> = 15 pF
- 4. DC input voltage specifications are proportional to supply voltage over operating range.
- 5. The number specified is the larger of tpLH and tpHL for each device.

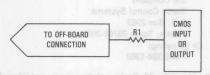
The input protection network uses a polysilicon resistor in series with the input and before the protection diodes. This series resistor slows down the slew rate of static discharge spikes to allow the protection diodes time to turn on. Outputs have a similar ESD protection network except for the series resistor. Although the on-chip protection circuitry guards against ESD damage, additional protection may be necessary once the chip is placed in circuit. Both an external series resistor and ground and VCC diodes, similar to the input protection structure, are recommended if there is a potential of ESD, voltage transients, etc. Several monolithic diode arrays are available from Motorola, such as the MAD130 (dual 10 diode array) or the MAD1104 (dual 8 diode array). These diodes, in chip form, not only provide the necessary protection, but also save board space as opposed to using discrete diodes.

Static damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged pins are the easiest to detect. An ESD-damaged pin that has been completely destroyed may exhibit a low-impedance path to VCC or GND. Another common failure mode is a fused or open circuit. The effect of both failure modes is that the device no longer properly responds to input signals. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performance. Generally, another effect of static damage is increased chip leakage currents (ICC).

Although the input network does offer significant protection, these devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4 to 15 kV range (depending

on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

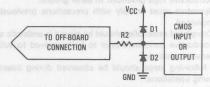
- Wrist straps and equipment logs should be maintained and audited on a regular basis. Wrist straps malfunction and may go unnoticed. Also, equipment gets moved from time to time and grounds may not be reconnected properly.
- Do not exceed the Maximum Ratings specified by the data sheet.
- All unused device inputs should be connected to V<sub>CC</sub> or GND.
- 4. All low impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the CMOS device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
- 5. Circuit boards containing CMOS devices are merely extensions of the devices, and the same handling precautions apply. Contacting edge connectors wired directly to device inputs can cause damage. Plastic wrapping should be avoided. When external connectors to a PC board are connected to an input or output of a CMOS device, a resistor should be used in series with the input or output. This resistor helps limit accidental damage if the PC board is removed and brought into contact with static generating materials. The limiting factor for the series resistor is the added delay. The delay is caused by the time constant formed by the series resistor and input capacitance. Note that the maximum input rise and fall times should not be exceeded. In Figure 4, two possible networks are shown using a series resistor to reduce ESD damage. For convenience, an equation is given for added propagation delay and rise time effects due to series resistance size.



Advantage: Requires minimal board area

Disadvantage: R1>R2 for the same level of protection; therefore, rise and fall times, propagation delays, and output drives are severely

affected.



Advantage: R2 < R1 for the same level of protection, Impact on ac and dc

characteristics is minimized.

Disadvantage: More board area, higher initial

cost.

NOTE: These networks are useful for protecting the following:

A digital inputs and outputs
B analog inputs and outputs

C 3-state outputs

outs and outputs D bidirectional (I/O) ports

Propagation Delay and Rise Time vs. Series Resistance

$$R \approx \frac{t}{C \cdot k}$$

where:

R = the maximum allowable series resistance in ohms

t = the maximum tolerable propagation delay or rise time in seconds

C = the board capacitance plus the driven device's input capacitance in farads

k=0.7 for propagation delay calculations

k = 2.3 for rise time calculations

Figure 4. Networks for Minimizing ESD and Reducing CMOS Latch Up Susceptibility

- 6. All CMOS devices should be stored or transported in materials that are antistatic or conductive. CMOS devices must not be inserted into conventional plastic "snow", styrofoam, or plastic trays, but should be left in their original container until ready for use.
- 7. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, because a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are essential and should be tested daily. See Figure 5 for an example of a typical work station.
- 8. Nylon or other static generating materials should not come in contact with CMOS devices.
- 9. If automatic handlers are being used, high levels of static electricity may be generated by the movement of the device, the belts, or the boards. Reduce static buildup by using ionized air blowers, anti-static sprays, and room humidifiers. All conductive parts of machines which come into contact with the top, bottom, or sides of IC packages must be grounded to earth ground.
- Cold chambers using CO<sub>2</sub> for cooling should be equipped with baffles, and the CMOS devices must be contained on or in conductive material.
- 11. When lead straightening or hand soldering is necessary, provide ground straps for the apparatus used and be sure that soldering iron tips are grounded.
- 12. The following steps should be observed during wave solder operations:
- a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to earth ground.
  - The loading and unloading work benches should have conductive tops grounded to earth ground.
  - c. Operators must comply with precautions previously explained.
  - d. Completed assemblies should be placed in antistatic or conductive containers prior to being moved to subsequent stations.
- 13. The following steps should be observed during boardcleaning operations:
  - Vapor degreasers and baskets must be grounded to earth ground.

- b. Brush or spray cleaning should not be used.
- c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic or conductive container.
- d. Cleaned assemblies should be placed in antistatic or conductive containers immediately after removal from the cleaning basket.
- High velocity air movement or application of solvents and coatings should be employed only when a static eliminator using ionized air is directed at the printed circuit board.
- The use of static detection meters for production line surveillance is highly recommended.
- 15. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
- 16. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
- 17. Double check test equipment setup for proper polarity of VCC and GND before conducting parametric or functional testing.
- 18. Do not recycle shipping rails. Repeated use causes deterioration of their antistatic coating. Exception: carbon rails (black color) may be recycled to some extent. This type of rail is conductive and antistatic.

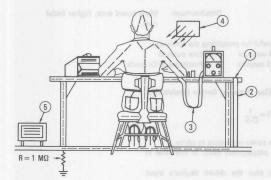
### RECOMMENDED READING

"Total Control of the Static in Your Business" Available by writing to:

Static Control Systems
P.O. Box 2963
Austin, Texas 78769-2963

Or by calling: 1-800-328-1368

S. Cherniak, "A Review of Transients and Their Means of Suppression", Application Note-843, Motorola Semiconductor Products Inc., 1982.



### NOTES

- 1. 1/16 inch conductive sheet stock covering bench-top work area.
- 2. Ground strap.
- 3. Wrist strap in contact with skin.
- Static neutralizer. (Ionized air blower directed at work.)
   Primarily for use in areas where direct grounding is impractical.
- Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside a building to be less than outside humidity.

Figure 5. Typical Manufacturing Work Station

### **POWER SUPPLY SIZING**

CMOS devices have low power requirements and the ability to operate over a wide range of supply voltages. These two characteristics allow CMOS designs to be implemented using inexpensive power supplies without cooling fans. In addition, batteries may be used as either a primary power source or as a backup.

The maximum recommended power supply voltage for HC devices is 6.0 V and 5.5 V for HCT devices. Figure 6 offers some insight as to how this specification was derived. In the figure, VS is the maximum power supply voltage and IS is the sustaining current for the latch-up mode. The value of VS was chosen so that the secondary breakdown effect may be avoided. The low-current junction avalanche region is between 10 and 14 volts at  $T_A\!=\!25^{\circ}C$ .

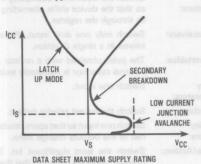


Figure 6. Secondary Breakdown Characteristics

In an ideal system design, the power supply should be designed to deliver only enough current to ensure proper operation of all devices. The obvious benefit of this type of design is cost savings.

### BATTERY SYSTEMS

HSCMOS devices can be used with battery or battery backup systems. A few precautions should be taken when designing battery-operated systems.

- The recommended power supply voltages should be observed. For battery backup systems such as the one in Figure 7, the battery voltage must be at least 2.7 volts (2 volts for the minimum power supply voltage and 0.7 volts to account for the voltage drop across the series diode).
- 2. Inputs that might go above the battery backup voltage should use the HC4049 or HC4050 buffers (Figure 8). If line power is interrupted, CMOS System A and Buffer A lose power. However, CMOS System B and Buffer B remain active due to the battery backup. Buffer A protects System A from System B by blocking active inputs while the circuit is not powered up. Also, if the power supply voltage drops below the battery voltage, Buffer A acts as a level translator for the outputs from System B. Buffer B acts to protect System B from any overvoltages which might exist. Both buffers may be replaced with current-limiting resistors, however power consumption is increased and propagation delays are lengthened.
- Outputs that are subject to voltage levels above V<sub>CC</sub> or below GND should be protected with a series resistor and/ or clamping diodes to limit the current to an acceptable level.

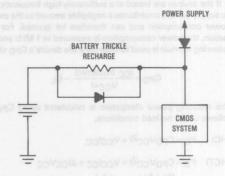


Figure 7. Battery Backup System

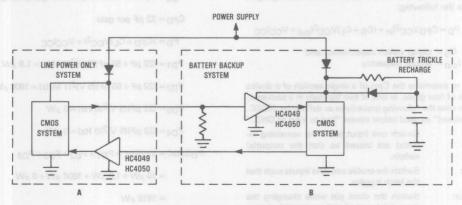


Figure 8. Battery Backup Interface

amphon for modivido is dependent on the power-supply voltage, frequency of operation, internal capacitance, and load. The power consumption may be calculated for each package by summing the quiescent power consumption, ICC. VCC, and the switching power required by each device within the package. For large systems, the most timely method is to bread-board the circuit and measure the current required under a variety of conditions.

The device dynamic power requirements can be calculated by the equation:

$$P_D = (C_L + C_{PD}) V_{CC}^2 f$$

where:  $P_D =$  power dissipated in  $\mu W$ 

CL = total load capacitance present at the output in

Cpn = a measure of internal capacitances, called power dissipation capacitance, given in pF

Vcc = supply voltage in volts f = frequency in MHz

If the devices are tested at a sufficiently high frequency, the dc supply current contributes a negligible amount to the overall power consumption and can therefore be ignored. For this reason, the power consumption is measured at 1 MHz and the following formula is used to determine the device's Cpn value:

$$C_{PD} = \frac{I_{CC} \text{ (dynamic)}}{V_{CC} \cdot f} - C_{L}$$

The resulting power dissipation is calculated using CpD as follows under no-load conditions.

(HC) 
$$P_D = C_{PD}V_{CC}^2f + V_{CC}I_{CC}$$

(HCT) 
$$P_D = C_{PD}V_{CC}^2f + V_{CC}I_{CC} + \Delta I_{CC}V_{CC}$$
  
 $(\delta_1 + \delta_2 + ... + \delta_n)$ 

where the previously undefined variable,  $\delta_{\Pi}$  is the duty cycle of each input applied at TTL/NMOS levels.

The power dissipation for analog switches switching digital signals is the following:

$$(HC) \qquad P_D = C_{PD}V_{CC}^2f_{in} + (C_S + C_L)V_{CC}^2f_{out} + V_{CC}I_{CC}$$

In order to determine the CPD of a single section of a device (i.e., one of four gates, or one of two flip-flops in a package), Motorola uses the following procedures as defined by JEDEC. Note: "biased" as used below means "tied to VCC or GND."

Gates: Switch one input while the remaining input(s) are biased so that the output(s)

switch.

Latches: Switch the enable and data inputs such that the latch toggles.

Flip-Flops: Switch the clock pin while changing the

data pin(s) such that the output(s) change with each clock cycle.

Data Selectors/ Multiplexers:

Switch one address input with the corresponding data inputs at opposite logic levels so that the output switches.

Analog Switches: Switch one address/select pin which changes two switches. The switch inputs/ outputs should be left open. For digital applications where the switch inputs/outputs change between VCC and GND, the respective switch capacitance should be added to the load capacitance.

Counters:

Switch the clock pin with the other inputs biased so that the device counts.

Shift Registers: Switch the clock while alternating the input so that the device shifts alternating 1s and

Os through the register.

Transceivers:

Switch only one data input. Place transceivers in a single direction.

Monostables: The pulse obtained with a resistor and no

external capacitor is repeatedly switched. Switch one input.

Parity

Generators: Encoders:

Switch the lowest priority output.

Display Drivers:

Switch one input so that approximately one-

half of the outputs change state.

ALUs/Adders:

Switch the least significant bit. The remaining inputs are biased so that the device is alternately adding 0000 (binary) or 0001

(binary) to 1111 (binary).

On HSCMOS data sheets, Cpp is a typical value and is given either for the package or for the individual device (i.e., gates, flip-flops, etc.) within the package. An example of calculating the package power requirement is given using the 74HC00, as shown in Figure 9.

From the data sheet:

 $I_{CC} = 2 \mu A$  at room temperature (per package)

CPD = 22 pF per gate

 $P_{D1} = (22 pF + 50 pF)(5 V)^{2}(1 kHz) = 1.8 \mu W$ 

 $PD2 = (22 pF + 50 pF)(5 V)^{2}(1 MHz) = 1800 \mu W$ 

 $P_{D3} = (22 pF)(5 V)^2(0 Hz) = 0 \mu W$ 

 $P_{D4} = (22 \text{ pF})(5 \text{ V})^2(0 \text{ Hz}) = 0 \mu \text{W}$ 

PD(total) = VCClCC+PD1+PD2+PD3+PD4

 $= 10 \mu W + 1.8 \mu W + 1800 \mu W + 0 \mu W$ 

 $= 1812 \mu W$ 

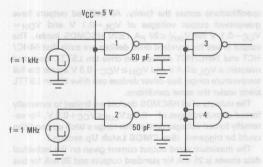


Figure 9. Power Consumption Calculation Example

As seen by this example, the power dissipated by CMOS devices is dependent on frequency. When operating at very high frequencies, HSCMOS devices can consume as much power as LSTTL devices, as shown in Figure 10. The power savings of HSCMOS is realized when used in a system where only a few of the devices are actually switching at the system frequency. The power consumption savings comes from the fact that for CMOS, only the devices that are switching consume significant power.

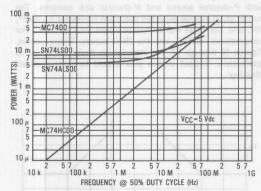


Figure 10. Power Consumption vs. Input Frequency for TTL, LSTTL, ALS, and HSCMOS

### **INPUTS**

A basic knowledge of input and output structures is essential to the HSCMOS designer. This section deals with the various input characteristics and application rules regarding their use. Output characteristics are discussed in the section titled Outputs.

All standard HC, HCU and HCT inputs, while in the recommended operating range (GND  $\leq$  V $_{in}$   $\leq$  VCC), can be modeled as shown in Figure 11. For input voltages in this range, diodes D1 and D2 are modeled as resistors representing the high-impedance of reverse biased diodes. The maximum input current is 1  $\mu$ A, worst case over temperature, when the inputs are at VCC or GND, and VCC = 6 V.

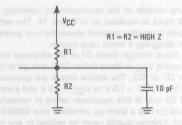


Figure 11. Input Model for GND ≤ Vin ≤ VCC

When CMOS inputs are left open-circuited, the inputs may be biased at or near the typical CMOS switchpoint of 0.45 V<sub>CC</sub> for HC devices or 1.3 V for HCT devices. At this switchpoint, both the P-channel and the N-channel transistors are conducting, causing excess current drain. Due to the high gain of the buffered devices (see Figure 12), the device can go into oscillation from any noise in the system, resulting in even higher current drain.

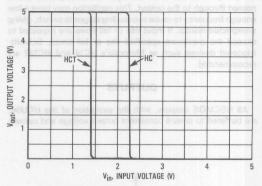


Figure 12. Typical Transfer Characteristics for Buffered Devices

For these reasons, all unused HC/HCT inputs should be connected either to  $V_{CC}$  or GND. For applications with inputs going to edge connectors, a 100 k $\Omega$  resistor to GND should be used, as well as a series resistor (Rg) for static protection and current limiting (see **Handling Precautions**, this chapter, for series resistor consideration). The resistors should be configured as in Figure 13.

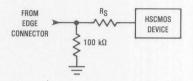


Figure 13. External Protection

Current flows through diode D1 or D2 whenever the input voltage exceeds V<sub>CC</sub> or drops below GND enough to forward bias either D1 or D2. The device inputs are guaranteed to withstand from GND - 1.5 V to V<sub>CC</sub> + 1.5 V and a maximum current of 20 mA. If this maximum rating is exceeded, the device could go into a latch-up condition (see CMOS Latch Up section). Voltage should never be applied to any input or output pin before power has been applied to the device's power pins. Bias on input or output pins should be removed before removing the power. However, if the input current is limited to less than 20 mA, and this current only lasts for a brief period of time (<100 ms), no damage to the device occurs.

Another specification that should be noted is the maximum input rise  $(t_{\Gamma})$  and fall  $(t_{\Gamma})$  times. Figure 15 shows the results of exceeding the maximum rise and fall times recommended by Motorola or contained in JEDEC Standard No. 7A. The reason for the oscillation on the output is that as the voltage passes through the switching threshold region with a slow rise time, any noise that is on the input line is amplified, and is passed through to the output. This oscillation may have a low enough frequency to cause succeeding stages to switch, giving unexpected results. If input rise or fall times are expected to exceed the maximum specified rise or fall times, Schmittriggered devices such as Motorola's HC14 and HC132 are recommended.

# **OUTPUTS**

All HSCMOS outputs, with the exception of the HCU04, are buffered to ensure consistent output voltage and current

Figure 14. Input Model for Vin>VCC or Vin<GND

specifications across the family. All buffered outputs have guaranteed output voltages of VOL=0.1 V and VOH= VCC-0.1 V for  $|I_{Out}| \leq 20~\mu A~(\leq 20~HSCMOS~loads)$ . The output drives for standard drive devices are such that 54HC/ HCT and 74HC/HCT devices can drive ten LSTTL loads and maintain a VOL $\leq 0.4$  V and VOH $\geq$ VCC-0.8 V across the full temperature range; bus-driver devices can drive fifteen LSTTL loads under the same conditions.

The outputs of all HSCMOS devices are limited to externally forced output voltages of  $-0.5 \le V_{Out} \le V_{CC} + 0.5 \text{ V}$ . For externally forced voltages outside this range a latch up condition could be triggered. (See **CMOS Latch Up** section.)

The maximum rated output current given on the individual data sheets is 25 mA for standard outputs and 35 mA for bus drivers. The output short circuit currents of these devices typically exceed these limits. The outputs can, however, be shorted for short periods of time for logic testing, if the maximum package power dissipation is not violated. (See individual data sheets for maximum power dissipation ratings.)

For applications that require driving high capacitive loads where fast propagation delays are needed (e.g., driving power MOSFETs), devices within the same package may be paralleled. Paralleling devices in different packages may result in devices switching at different points on the input voltage waveform, creating output short circuits and yielding undesirable output voltage waveforms.

As a design aid, output characteristic curves are given for both P-channel source and N-channel sink currents. The curves given include expected minimum curves for  $T_A = 25^\circ$ ,  $85^\circ$ , and  $125^\circ$ C, as well as typical values for  $T_A = 25^\circ$ C. For temperatures  $<25^\circ$ C, use the  $25^\circ$ C curves. These curves, Figures 16 through 27, are intended as design aids, not as guarantees. Unused output pins should be open-circuited (floating).

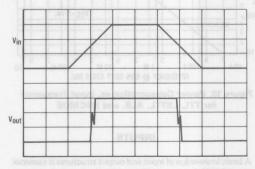


Figure 15. Maximum Rise Time Violation

# N-CHANNEL SINK CURRENT

STANDARD OUTPUT CHARACTERISTICS

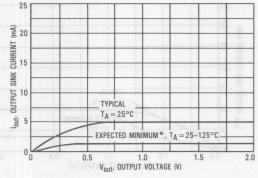


Figure 16. VGS=2.0 V

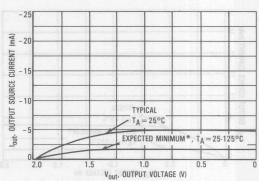


Figure 17. VGS = -2.0 V

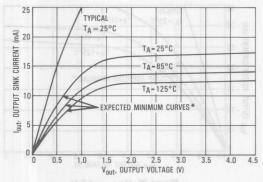


Figure 18. VGS = 4.5 V

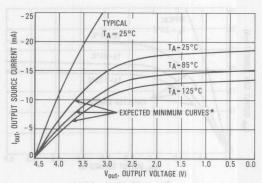


Figure 19. VGS = -4.5 V

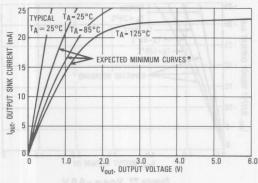


Figure 20. VGS = 6.0 V

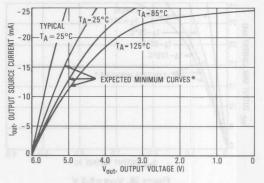


Figure 21.  $V_{GS} = -6.0 \text{ V}$ 

<sup>\*</sup>The expected minimum curves are not guarantees but are design aids.

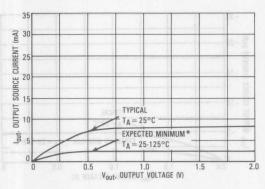


Figure 22. VGS = 2.0 V

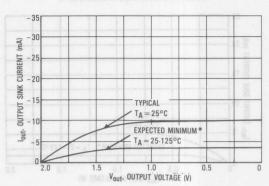


Figure 23. VGS = -2.0 V

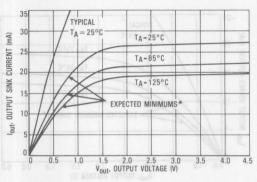


Figure 24. VGS = 4.5 V

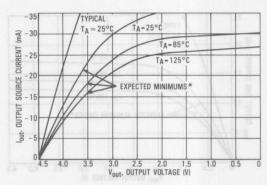


Figure 25. VGS = -4.5 V

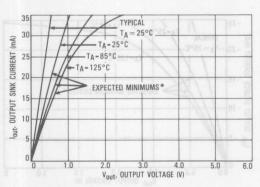


Figure 26. VGS = 6.0 V

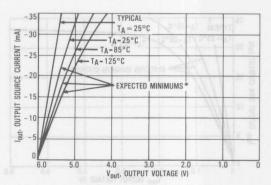


Figure 27. VGS = -6.0 V

<sup>\*</sup>The expected minimum curves are not guarantees, but are design aids.

# **3-STATE OUTPUTS**

Some HC/HCT devices have outputs that can be placed into a high-impedance state. These 3-state output devices are very useful for gang connecting to a common line or bus. When enabled, these output pins can be considered as ordinary output pins; as such, all specifications and precautions of standard output pins should be followed. When disabled (high-impedance state), these outputs can be modeled as in Figure 28. Output leakage current (10  $\mu$ A worst case over temperature) as well as 3-state output capacitance must be considered in any bus design.

When power is interrupted to a 3-state device, the bus voltage is forced to between GND and VCC  $\pm$  0.7 V regardless of the previous output state.

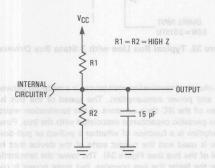


Figure 28. Model for Disabled Outputs

# **OPEN-DRAIN OUTPUTS**

Motorola provides several devices that are designed only to sink current to GND. These open-drain output devices are fabricated using only an N-channel transistor and a diode to  $V_{CC}$  (Figure 29). The purpose of the diode is to provide ESD protection. Open-drain outputs can be modeled as shown in Figure 30.

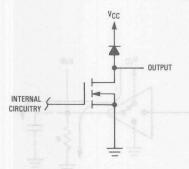


Figure 29. Open-Drain Output

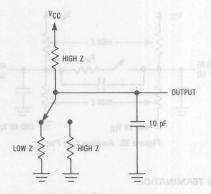


Figure 30. Model of Open-Drain Output

#### INPUT/OUTPUT PINS

Some HC/HCT devices contain pins that serve both as inputs and outputs of digital logic. These pins are referred to as digital I/O pins. The logic level applied to a control pin determines whether these I/O pins are selected as inputs or outputs.

When I/O pins are selected as outputs, these pins may be considered as standard CMOS outputs. When selected as inputs, except for an increase in input leakage current and input capacitance, these pins should be considered as standard CMOS inputs. These increases come from the fact that a digital I/O pin is actually a combination of an input and a 3-state output tied together (see Figure 31).

As stated earlier, all HC/HCT inputs must be connected to an appropriate logic level. This could pose a problem if an I/O pin is selected as an input while connected to an improperly terminated bus.

Motorola recommends terminating HC/HCT-type buses with resistors to V<sub>CC</sub> or GND of between 1 k $\Omega$  to 1 M $\Omega$  in value. The choice of resistor value is a trade-off between speed and power consumption (see **Bus Termination**, this chapter).

Some Motorola devices have analog I/O pins. These analog I/O pins should not be confused with digital I/O pins. Analog I/O pins may be modeled as in Figure 32. These devices can be used to pass analog signals, as well as digital signals, in the same manner as mechanical switches.

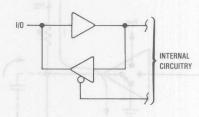


Figure 31. Typical Digital I/O Pin

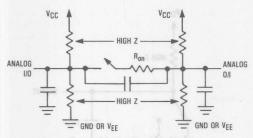


Figure 32. Analog I/O Pin

#### **BUS TERMINATION**

Because buses tend to operate in harsh, noisy environments, most bus lines are terminated via a resistor to VCC or ground. This low impedance to VCC or ground (depending on preference of a pull-up or pull-down logic level) reduces bus noise pickup. In certain cases a bus line may be released (put in a high-impedance state) by disabling all the 3-state bus drivers (see Figure 33). In this condition all HC/HCT inputs on the bus would be allowed to float. A CMOS input or I/O pin (when selected as an input) should never be allowed to float. (This is one reason why an HCT device may not be a drop-in replacement of an LSTTL device.) A floating CMOS input can put the device into the linear region of operation. In this region excessive current can flow and the possibility of logic errors due to oscillation may occur (see Inputs, this chapter). Note that when a bus is properly terminated with pull-up resistors, HC devices, instead of HCT devices, can be driven by an NMOS or LSTTL bus driver. HC devices are preferred over HCT devices in bus applications because of their higher lowlevel input noise margin. (With a 5 V supply the typical HC switch point is 2.3 V while the switch point of HCT is only 1.3 V.)

Some popular LSTTL bus termination designs may not work for HSCMOS devices. The outputs of HSCMOS may not be able to drive the low value of termination used by some buses. (This is another reason why an HCT device may not be a dropin replacement for an LSTTL device.) However, because low power operation is one of the main reasons for using CMOS, an optimized CMOS bus termination is usually advantageous.

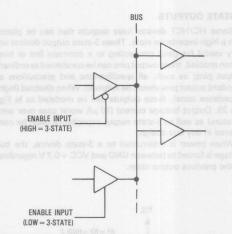
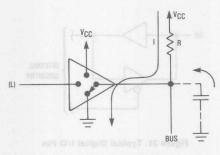
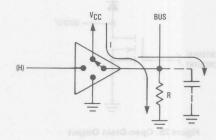


Figure 33. Typical Bus Line with 3-State Bus Drivers

The choice of termination resistances is a trade-off between speed and power consumption. The speed of the bus is a function of the RC time constant of the termination resistor and the parasitic capacitance associated with the bus. Power consumption is a function of whether a pull-up or pull-down resistor is used and the output state of the device that has control of the bus (see Figure 34). The lower the termination resistor the faster the bus operates, but more power is consumed. A large value resistor wastes less power, but slows the bus down. Motorola recommends a termination resistor value between 1 k $\Omega$  and 1 M $\Omega$ . An alternative to a passive resistor termination would be an active-type termination (see Figure 35). This type termination holds the last logic level on the bus until a driver can once again take control of the bus. An active termination has the advantage of consuming a minimal amount of power. Most HC/HCT bus drivers do not have built-in hysteresis. Therefore, heavily loaded buses can slow down rise and fall signals and exceed the input rise/fall time defined in JEDEC Standard No. 7A. In this event, devices with Schmitt-triggered inputs should be used to condition these slow signals.



(a) USING A PULL-UP RESISTOR



(b) USING A PULL-DOWN RESISTOR

Figure 34

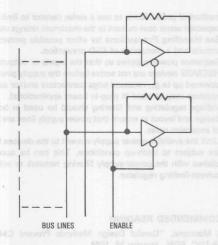


Figure 35. Using Active Termination (HC125)

# TRANSMISSION LINE TERMINATION

When data is transmitted over long distances, the line on which the data travels can be considered a transmission line. (Long distance is relative to the data rate being transmitted.) Examples of transmission lines include high-speed buses, long PCB lines, coaxial and ribbon cables. All transmission lines should be properly terminated into a low-impedance termination. A low-impedance termination helps eliminate noise, ringing, overshoot, and crosstalk problems. Also a low-impedance termination reduces signal degradation because the small values of parasitic line capacitance and inductance have lesser effect on a low-impedance line.

The value of the termination resistor becomes a trade-off between power consumption, data rate speeds, and transmission line distance. The lower the resistor value, the faster data can be presented to the receiving device, but the more power the resistor consumes. The higher the resistor value, the longer it will take to charge and discharge the transmission line through the termination resistor ( $T = R \cdot C$ ).

Transmission line distance becomes more critical as data rates increase. As data rates increase, incident (and reflective) waves begin to resemble that of RF transmission line theory. However, due to the nonlinearity of CMOS digital logic, conventional RF transmission theory is not applicable.

HC devices are preferred over HCT devices due to the fact that HC devices have higher switch points than HCT devices. This higher switch point allows HC devices to achieve better incident wave switching on lower impedance lines.

HC/HCT may not have enough drive capability to interface with some of the more popular LSTTL transmission lines. (Possible reason why an HCT device may not be a drop-in replacement of an equivalent TTL device.) This does not pose a major problem since having larger value termination resistors is desirable for CMOS type transmission lines.

By increasing the termination resistance value, the CMOS advantage of low power consumption can be realized. Motorola recommends a minimum termination resistor value as shown in Figure 36. The termination resistor should be as close to the receiving unit as possible. Another method of

terminating the line driver, as well as the receiving unit, is shown in Figure 37. Note that the resistor values in Figure 37 are twice the resistor value of Figure 36; this gives a net equivalent termination value of Figure 36. Even higher values of resistors may be used for either termination method. This reduces power consumption, but at the expense of speed and possible signal degradation.

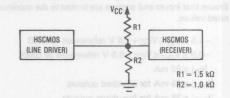


Figure 36. Termination Resistors at the Receiver

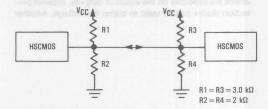


Figure 37. Termination Resistors at Both the Line Driver and Receiver

# **CMOS LATCH UP**

Typically, HSCMOS devices do not latch up with currents of 75 mA forced into or out of the inputs or 300 mA for the outputs under worst case conditions ( $T_A = 125^{\circ}C$  and  $V_{CC} = 6$  V). Under dc conditions for the inputs, the input protection network typically fails, due to grossly exceeding the maximum input voltage rating of -1.5 to  $V_{CC} + 1.5$  V before latch-up currents are reached. For most designs, latch up will not be a problem, but the designer should be aware of it, what causes it, and how it can be prevented.

Figure 38 shows the layout of a typical CMOS inverter and Figure 39 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the device on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the SAM evice, the output voltage must be greater than VCC+0.5 V or less than -0.5 V and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device can be destroyed or its reliability can be degraded. Ways to prevent such an occurrence are listed below.

- Ensure that inputs and outputs are limited to the maximum rated values.
  - -1.5 ≤ V<sub>in</sub> ≤ V<sub>CC</sub>+1.5 V referenced to GND
  - -0.5 ≤ V<sub>out</sub> ≤ V<sub>CC</sub> + 0.5 V referenced to GND

|lin| ≤20 mA

|lout | ≤25 mA for standard outputs

|Iout| ≤35 mA for bus-driver outputs

If voltage transients of sufficient energy to latch up the device are expected on the inputs or outputs, external protection diodes can be used to clamp the voltage. Another

- expected worst case current to the maximum ratings value. See **Handling Precautions** for other possible protection circuits and a discussion of ESD prevention.
- Sequence power supplies so that the inputs or outputs of HSCMOS devices are not active before the supply pins are powered up (e.g., recessed edge connectors and/or series resistors may be used in plug-in board applications).
- Voltage regulating and filtering should be used in board design and layout to ensure that power supply lines are free of excessive noise.
- Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power-supply filtering network or with a current-limiting regulator.

# RECOMMENDED READING

Paul Mannone, "Careful Design Methods Prevent CMOS Latch-Up", EDN, January 26, 1984.

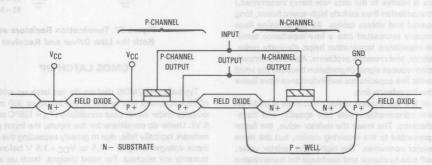


Figure 38. CMOS Wafer Cross Section

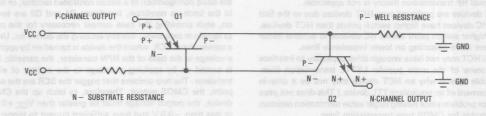


Figure 39. Latch-Up Circuit Schematic

# MAXIMUM POWER DISSIPATION

The maximum power dissipation for Motorola HSCMOS packages is 750 mW for both ceramic and plastic DIPs and 500 mW for SOIC packages. The deratings are -10 mW/°C from 65°C for plastic DIPs, -10 mW/°C from 100°C for ceramic packages, and -7 mW/°C from 65°C for SOIC packages. This is illustrated in Figure 40.

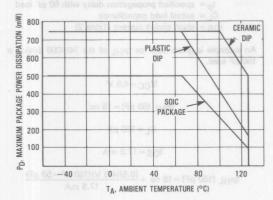


Figure 40. Maximum Package Power Dissipation versus Temperature

Internal heat generation in HSCMOS devices comes from two sources, namely, the quiescent power and dynamic power consumption.

In the quiescent state, either the P-channel or N-channel transistor in each complementary pair is off except for small source-to-drain leakage due to the inputs being either at V<sub>CC</sub> or ground. Also, there are the small leakage currents flowing in the reverse-biased input protection diodes and the parasitic diodes on the chip. The specification which takes all leakage into account is called Maximum Quiescent Supply Current (per package), or I<sub>CC</sub>, and is shown on all data sheets.

The three factors which directly affect the value of quiescent power dissipation are supply voltage, device complexity, and temperature. On the data sheets, I<sub>CC</sub> is specified only at V<sub>CC</sub>=6.0 V because this is the worst-case supply voltage condition. Also, larger or more complex devices consume more quiescent power because these devices contain a proportionally greater reverse-biased diode junction area and more off (leaky) FFTs.

Finally, as can be seen from the data sheets, temperature increases cause I<sub>CC</sub> increases. This is because at higher temperatures, leakage currents increase.

# HC QUIESCENT POWER DISSIPATION

When HC device inputs are virtually at  $V_{CC}$  or GND potential (as in a totally CMOS system), quiescent power dissipation is minimized. The equation for HC quiescent power dissipation is given by:

PD=Vcclcc

Worst-case  $I_{CC}$  occurs at  $V_{CC}$ =6.0 V. The value of  $I_{CC}$  at  $V_{CC}$ =6.0 V, as specified in the data sheets, is used for all power supply voltages from 2 to 6 V.

# HCT QUIESCENT POWER DISSIPATION

Although HCT devices belong to the CMOS family, their input voltage specifications are identical to those of LSTTL. HCT parts can therefore be either judiciously substituted for or mixed with LS devices in a system.

TTL output voltages are V<sub>OL</sub> = 0.4 V (max) and V<sub>OH</sub> = 2.4 to 2.7 V (min).

Slightly higher I $_{CC}$  current exists when an HCT device is driven with  $V_{OL}$ =0.4 V (max) because this voltage is high enough to partially turn on the N-channel transistor. However, when being driven with a TTL  $V_{OH}$ , HCT devices exhibit large additional current flow ( $\Delta I_{CC}$ ) as specified on HCT device data sheets.  $\Delta I_{CC}$  current is caused by the off-rail input voltage turning on both the P and N channels of the input buffer. This condition offers a relatively low impedance path from  $V_{CC}$  to GND. Therefore, the HCT quiescent power dissipation is dependent on the number of inputs applied at the TTL  $V_{IH}$  logic voltage level.

The equation for HCT quiescent power dissipation is given by:

$$P_D = I_{CC}V_{CC} + \eta \Delta I_{CC}V_{CC}$$

where  $\eta$  = the number of inputs at the TTL VIH level.

# HC AND HCT DYNAMIC POWER DISSIPATION

Dynamic power dissipation is calculated in the same way for both HC and HCT devices. The three major factors which directly affect the magnitude of dynamic power dissipation are load capacitance, internal capacitance, and switching transient currents.

The dynamic power dissipation due to capacitive loads is given by the following equation:

where  $P_D = power$  in  $\mu W$ ,  $C_L = capacitive$  load in pF,  $V_{CC} = supply voltage$  in volts, and f = output frequency driving the load capacitor in MHz.

All CMOS devices have internal parasitic capacitances that have the same effect as external load capacitors. The magnitude of this internal no-load power dissipation capacitance, CPD, is specified as a typical value.

Finally, switching transient currents affect the dynamic power dissipation. As each gate switches, there is a short period of time in which both N- and P-channel transistors are partially on, creating a low-impedance path from V<sub>CC</sub> to ground. As switching frequency increases, the power dissipation due to this effect also increases.

The dynamic power dissipation due to CPD and switching transient currents is given by the following equation:

Therefore, the total dynamic power dissipation is given by:

$$P_D = V_{CC} I_{CC} + (C_L + C_{PD}) V_{CC} I_{CC} I_{CC}$$

When being driven by LSTTL logic voltage levels, the total power dissipation for HCT devices is given by the equation:

$$P_{D} = V_{CC} C_{CC} + V_{CC} \Delta I_{CC} (\delta, + \delta_{2} + \dots + \delta_{n})$$
$$+ (C_{L} + C_{PD}) V_{CC}^{2} f$$

where  $\delta_{\Pi}\!=\!$  duty cycle of LSTTL output applied to each input of an HCT device.

# CAPACITIVE LOADING EFFECTS ON PROPAGATION DELAY

In addition to temperature and power-supply effects, capacitive loading effects should be taken into account. The additional propagation delay may be calculated if the short circuit current for the device is known. Expected minimum numbers may be determined from Table 2.

From the equation

$$i = \frac{Cdv_C}{dt}$$

this approximation follows:

$$I = \frac{C\Delta V}{\Delta t}$$
 so 
$$\Delta t = \frac{C\Delta V}{I}$$
 or 
$$\Delta t = \frac{C(0.5 \text{ V}_{CC})}{I}$$

because the propagation delay is measured to the 50% point of the output waveform (typically 0.5 VCC).

This equation gives the general form of the additional propagation delay. To calculate the propagation delay of a device for a particular load capacitance, C<sub>L</sub>, the following equation may be used.

$$t_{PT} = t_{P} + 0.5 \text{ VCC } (C_{L} - 50 \text{ pF})/los$$

where tpT= total propagation delay

tp = specified propagation delay with 50 pF load

C<sub>L</sub> = actual load capacitance

IOS = short circuit current (Table 2)

An example is given here for tpHL of the 74HC00 driving a 150 pF load.

$$V_{CC} = 4.5 \text{ V}$$
 $t_{PHL} (50 \text{ pF}) = 18 \text{ ns}$ 
 $C_{L} = 150 \text{ pF}$ 
 $I_{OS} = 17.3 \text{ mA}$ 

$$t_{PHL}$$
 (150 pF) = 18 ns +  $\frac{(0.5)(4.5 \text{ V})(150 \text{ pF} - 50 \text{ pF})}{17.3 \text{ mA}}$ 

Another example for  $C_L = 0$  pF and all other parameters the same.

$$t_{PHL}$$
 (0 pF) = 18 ns +  $\frac{(0.5)(4.5 \text{ V})(0 \text{ pF} - 50 \text{ pF})}{17.3 \text{ mA}}$   
= 18 ns + ( - 6.5 ns)  
 $t_{PHL}$  = 11.5 ns

This method gives the expected propagation delay and is intended as a design aid, not as a guarantee.

Table 2. Expected Minimum Short Circuit Currents\*

lockes a typical value.	finequal-	Sta	ndard Dri	vers	E	Bus Drive	rs	11-14
Parameter	VCC	25°C	85°C	125°C	25°C	85°C	125°C	Unit
Output Short Circuit Source Current	2.0	1.89	1.83	1.80	3.75	3.64	3.60	mA
	4.5	18.5	15.0	13.4	37.0	30.0	26.6	
	6.0	35.2	28.0	24.6	70.6	56.1	49.2	
Output Short Circuit Sink Current	2.0	1.55	1.55	1.55	2.45	2.45	2.43	mA
	4.5	17.3	14.0	12.5	27.2	22.1	19.6	
	6.0	33.4	26.5	23.2	52.6	41.7	36.5	

<sup>\*</sup>These values are intended as design aids, not as guarantees.

# TEMPERATURE EFFECTS ON DC AND AC PARAMETERS

One of the inherent advantages of CMOS devices is that characteristics of the N- and P-channel transistors, such as drive current, channel resistance, propagation delay, and output transition time, track each other over a wide temperature range. Figure 41 shows the temperature relationships for these parameters. To illustrate the effects of temperature on noise margin, Figure 42 shows the typical transfer characteristics for devices with buffered inputs and outputs. Note that the typical switch point is at 45% of the supply voltage and is minimally affected by temperature.

The graphs in this section are intended to be design aids, not guarantees.

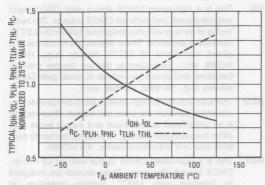


Figure 41. Characteristics of Drive Current, Channel Resistance, and AC Parameters Over Temperature

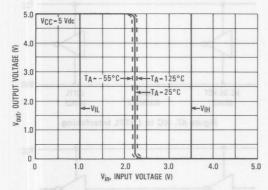


Figure 42. Temperature Effects on the HC Transfer Characteristics

# SUPPLY VOLTAGE EFFECTS ON DRIVE CURRENT AND PROPAGATION DELAY

The transconductive gain,  $I_{Out}/V_{in}$ , of MOSFETs is proportional to the gate voltage minus the threshold voltage,  $V_G-V_T$ . The gate voltage at the input of the final stage of buffered devices is approximately the power supply voltage,  $V_{CC}$  or GND. Because  $V_G=V_{CC}$  or GND, the output drive current is proportional to the supply voltage. Propagation delays for CMOS devices are also affected by the power supply voltage, because most of the delay is due to charging and discharging internal capacitances. Figures 43 and 44 show the typical variation of current drive and propagation delay, normalized to  $V_{CC}=4.5$  V for  $2.0 \le V_{CC} \le 6.0$  V. These curves may be used with the tables on each data sheet to arrive at parametric values over the voltage range.

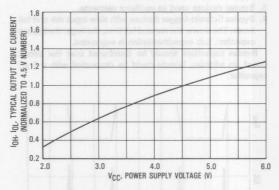


Figure 43. Drive Current versus VCC

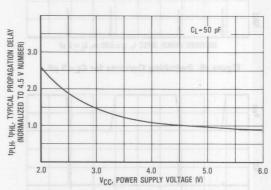


Figure 44. Propagation Delay versus VCC

The switching waveforms shown in Figures 45 and 46 show the current spikes introduced to the power supply and ground lines. This effect is shown for a load capacitance of less than 5 pF and for 50 pF. For ideal power supply lines with no series impedance, the spikes would pose no problem. However, actual power supply and ground lines do possess series impedance, giving rise to noise problems. For this reason, care should be taken in board layouts, ensuring low impedance paths to and from logic devices.

To absorb switching spikes, the following HSCMOS devices should be bypassed with good quality 0.022  $\mu$ F to 0.1  $\mu$ F decoupling capacitors:

- Bypass every device driving a bus with all outputs switching simultaneously.
- 2. Bypass all synchronous counters.
- 3. Bypass devices used as oscillator elements.
- Bypass Schmitt-trigger devices with slow input rise and fall times. The slower the rise and fall time, the larger the bypass capacitor. Lab experimentation is suggested.

Bypass capacitors should be distributed over the circuit board. In addition, boards could be decoupled with a 1  $\mu F$  capacitor.

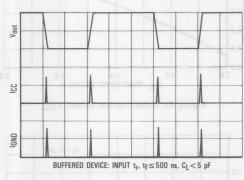


Figure 45. Switching Currents for C<sub>I</sub> <5 pF

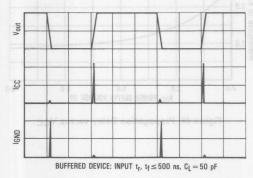


Figure 46. Switching Currents for CL = 50 pF

HSCMOS devices have a wide operating voltage range (V<sub>CC</sub> = 2 to 6 V) and sufficient current drive to interface with most other logic families available today. In this section, various interface schemes are given to aid the designer (see Figures 47 through 52). The various types of CMOS devices with their input/output levels and comments are given in Table 3.

Motorola presently has available several CMOS memories and microprocessors (see Table 4) which are designed to directly interface with High-Speed CMOS. With these devices now available, the designer has an attractive alternative to LSTTL/NMOS, and a total HSCMOS system is now possible. (See SG102, CMOS System IC Selection Guide, for more information.)

Device designators are as follows:

- HC This is a high-speed CMOS device with CMOS input switching levels and buffered CMOS outputs. The numbering of devices with this designator follows the LSTTL numbering sequence. These devices are functional and pinout equivalents of LSTTL devices (e.g., HC00, HC688, etc.). Exceptions to this are devices that are functional and pinout equivalents to metal-gate CMOS devices (e.g., HC4002, HC4538, etc.).
- HCU This is an unbuffered high-speed CMOS device with only one stage between the input and output. Because this is an unbuffered device, input and output levels may differ from buffered devices. At present, the family contains only one unbuffered device, the HCU04.
- HCT This is a high-speed CMOS device with an LSTTL-to-CMOS input buffer stage. These devices are designed to interface with LSTTL outputs operating at VCC=5 V ±10%. HCT devices have fully buffered CMOS outputs that directly drive HSCMOS or LSTTL devices.

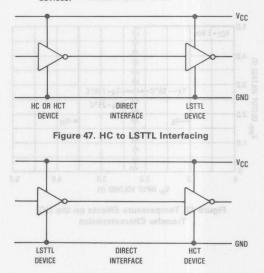


Figure 48. LSTTL to HCT Interfacing

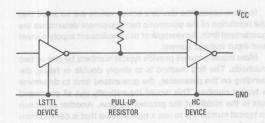


Figure 49. LSTTL to HC Interfacing

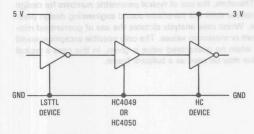
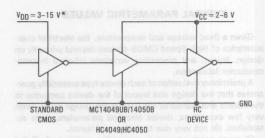


Figure 50. LSTTL to Low-Voltage HSCMOS



 $^*V_{OH}$  must be greater than V<sub>IH</sub> of low voltage Device; V<sub>DD</sub>=3-18 V may be used if interfacing to 14049UB/14050B.

Figure 51. High Voltage CMOS to HSCMOS

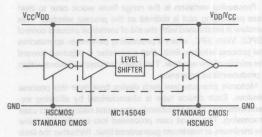


Figure 52. Up/Down Level Shifting Using the MC14504B

Table 3. Interfacing Guide

Device	Input Level	Output Level	Comments Comments
HCXXX	CMOS	CMOS	LSTTL Functional and Pinout Equivalent Devices
HC4XXX	CMOS	CMOS	CMOS Functional and Pinout Equivalent Devices
HCUXX	CMOS	CMOS	Used in Linear Applications
HCTXXX	TTL	CMOS	HSCMOS Device with TTL-to-CMOS Input Buffering
HC4049, HC4050	$-0.5 \le V_{in} \le 15 \text{ V}$	CMOS	High-to-Low Level Translators, CMOS Switching Levels
MC14049UB MC14050B	-0.5≤V <sub>in</sub> ≤18 V	CMOS	Metal-Gate CMOS High-to-Low Level Translators, CMOS Switching Levels
MC14504B	CMOS or TTL	CMOS	Metal-Gate CMOS High-to-Low or Low-to-High Level Translator

Table 4. CMOS Memories and Microprocessors

CMOS Memories	CMOS Mic	roprocessors
MCM6147	MC68HC01	MC146805G2
MCM61L47	MC68HC03	MC146805H2
MCM68HC34	MC68HC11A8	MC1468705F2
	MC68HC11D4	MC1468705G2
	MC68HC811A2	MC68HC05C4
	MC68HC811D4	MC68HSC05C4
	MC68HC04P3	MC68HC05C8
	MC146805E2	MC68HC805C4
	MC146805F2	MC68HC000

# RECOMMENDED READING

S. Craig, "Using High-Speed CMOS Logic for Microprocessor Interfacing", Application Note-868, Motorola Semiconductor Products Inc., 1982.

Given a fixed voltage and temperature, the electrical characteristics of High-Speed CMOS devices depend primarily on design, layout, and processing variations inherent in semi-conductor fabrication.

A preliminary evaluation of each device type essentially guarantees that the design and layout of the device conforms to the criteria and standards set forth in the design goals. With very few exceptions, device electrical parameters, once established, do not vary due to design and layout.

Of much more concern is processing variation. A digital processing line is allowed to deviate over a fairly broad processing range. This allows the manufacturer to incur reduced processing costs. These reduced processing costs are passed on to the consumer in the form of lower device prices.

Processing variation is the range from worst case to best case processing and is defined as the process window. This window is established with the aid of statistical process control (SPC). With SPC, when a processing parameter approaches the process window limit, that parameter is adjusted toward the middle of the window. This keeps process variations within a predetermined tolerance.

Motorola characterizes each device type over this process window. Each device type is characterized by allowing experimental lots to be processed using worst case and best case processing. The worst case processed lots usually determine the minimum or maximum guaranteed limit. (Whether the limit is a guaranteed minimum or maximum depends on the particular parameter being measured.)

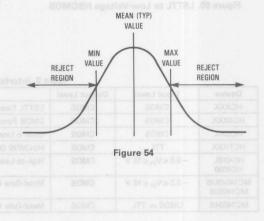
In production, these limits are guaranteed by probe and final test and therefore appear independent of process variation to the end user. However, this does not hold true for the mean value of the total devices processed. The mean value, commonly referred to as a typical value, shifts over processing and therefore varies from lot to lot or even wafer to wafer within a lot.

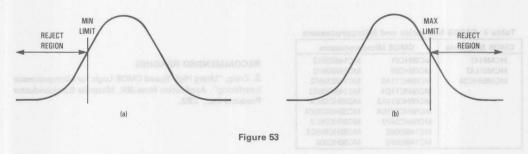
As with all processing or manufacturing, the total devices being produced fit the normal distribution or bell curve of Figure 53. In order to guarantee a valid typical value, a typical number plus a tolerance, would have to be specified and tested (see Figure 54). However, this would greatly increase processing costs which would have to be absorbed by the consumer.

In some cases, the device's actual values are so small that the resolution of the automatic test equipment determines the guaranteed limit. An example of this is quiescent supply current and input leakage current.

Most manufacturers provide typical numbers by one of two methods. The first method is to simply double or halve, depending on the parameter, the guaranteed limit to determine a typical number. This would theoretically put all processed lots in the middle of the process window. Another approach to typical numbers is to use a typical value that is derived from the aforementioned experimental lots. However, neither method accurately reflects the mean value of devices any one consumer can expect to receive.

Therefore, the use of typical parametric numbers for design purposes does not constitute sound engineering design practice. Worst case analysis dictates the use of guaranteed minimum or maximum values. The only possible exception would be when no guaranteed value is given. In this case a typical value may be used as a ballpark figure.





# REDUCTION OF ELECTROMAGNETIC INTERFERENCE (EMI)

Electromagnetic interference (EMI) and radio frequency interference (RFI) are phenomena inherent in all electrical systems covering the entire frequency spectrum. Although the characteristics have been well documented, EMI remains difficult to deal with due to numerous variables. EMI should be considered at the beginning of a design, and taken into account during all stages, including production and beyond.

These entities must be present for EMI to be a factor: (1) a source of EMI, (2) a transmission medium for EMI, and (3) a receiver of EMI. Several sources include relays, FM transmitters, local oscillators in receivers, power lines, engine ignitions, arc welders, and lighting. EMI transmission paths include ground connections, cables, and the space between conductors. Some receivers of EMI are radar receivers, computers, and television receivers.

For microprocessor based equipment, the source of emissions is usually a current loop on a PC board. The chips and their associated loop areas also function as receivers of EMI. The fact is that PC boards which radiate high levels of EMI are also more likely to act as receivers of EMI.

All logic gates are potential transmitters and receivers of emissions. Noise immunity and noise margin are two criterion which measure a gate's immunity to noise which could be caused by EMI. CMOS technology, as opposed to the other commonly used logic families, offers the best value for noise margin, and is therefore an excellent choice when considering EMI.

The electric and magnetic fields associated with ICs are porportional to the current used, the current loop area, and the switching transition times. CMOS technology is preferred due to smaller currents. Also, the current loop area can be reduced by the use of surface mount packages.

In a system where several pieces of equipment are connected by cables, at least five coupling paths should be taken into account to reduce EMI. They are: (1) common ground impedance coupling (a common impedance is shared between an EMI source and receiver), (2) common-mode, field-to-cable coupling (electromagnetic fields enter the loop found by two pieces of equipment, the cable connecting them, and the ground plane), (3) differential-mode, field-to-cable coupling (electromagnetic fields enter the loop formed by two pieces of equipment and the cable connecting them), (4) crosstalk coupling (signals in one transmission line are coupled into another transmission line), and (5) a conductive path through power lines.

Shielding is a means of reducing EMI. Some of the more commonly used shields against EMI and RFI contain stainless steel fiber-filled polycarbonate, aluminum flake-filled polycarbonate/ABS coated with nickel and copper electrolysis plating or cathode sputtering, nickel coated graphite fiber, and polyester SMC with carbon-fiber veil. Several manufacturers who make conductive compounds and additives are listed below.

# SHIELDING MANUFACTURERS

General Electric Co., Plastics Group, Pittsfield, MA
Mobay Chemical Corp., Pittsburg, PA
Wilson-Fiberfil International, Evansville, IN
American Cyanamid Co., Wayne, NJ
Fillite U.S.A., Inc., Huntington, WV
Transnet Corp., Columbus, OH

Motorola does not recommend, or in any way warrant the manufacturers listed here. Additionally, no claim is made that this list is by any means complete.

# RECOMMENDED READING

- D. White, K. Atkinson, and J. Osburn, "Taming EMI in Microprocessor Systems", *IEEE Spectrum*, Vol. 22, Number 12, Dec. 1985.
- D. White and M. Mardiguian, *EMI Control Methodology and Procedures*, 1985.
- H. Denny, Grounding for the Control of EMI.
- M. Mardiguian, How to Control Electrical Noise.
- D. White, Shielding Design Methodology and Procedures.

For more information on this subject, contact:

Interference Control Technologies
Don White Consultants, Inc., Subsidiary
State Route 625
P.O. Box D
Gainesville, VA 22065

# HYBRID CIRCUIT GUIDELINES

High-Speed CMOS devices, when purchased in chip (die) form, are useful in hybrid circuits. Most high-speed devices are fabricated with P wells and N substrates. Therefore, the substrates should be tied to  $V_{CC}$  (+ supply).

Several devices however, are fabricated with N wells and P substrates. In this case, the substrates should be tied to GND. The best solution to alleviate confusion about the substrate is the use of nonconductive or insulative substrates. This averts the necessity of tying the substrate off to either VCC or GND.

For more information on hybrid technology, contact:

International Society for Hybrid Microelectronics
P.O. Box 3255
Montgomery, AL 36109

Schmitt-trigger devices exhibit the effect of hysteresis. Hysteresis is characterized by two different switching threshold levels, one for positive-going input transitions and the other for negative-going input transitions.

Schmitt triggers offer superior noise immunity when compared to standard gates and inverters. Applications for Schmitt triggers include line receivers, sine to square wave converters, noise filters, and oscillators. Motorola offers six versatile Schmitt-trigger devices in the High-Speed CMOS logic family (see Table 5).

The typical voltage transfer characteristics of a standard CMOS inverter and a CMOS Schmitt-trigger inverter are compared in Figures 55 and 56. The singular transfer threshold of the standard inverter is replaced by two distinct thresholds in a Schmitt-trigger inverter. During a positive-going transition of  $V_{\rm in}$ , the output begins to go low after the  $V_{\rm T}+$  threshold is reached. During a negative-going  $V_{\rm in}$  transition,  $V_{\rm out}$  begins to go high after the  $V_{\rm T}-$  threshold is reached. The difference between  $V_{\rm T}+$  and  $V_{\rm T}-$  is defined as  $V_{\rm H},$  the hysteresis voltage.

As a direct result of hysteresis, Schmitt-trigger circuits provide excellent noise immunity and the ability to square up signals with long rise and fall times. Positive-going input noise excursions must rise above the V $_{T+}$  threshold before they affect the output. Similarly, negative-going input noise excursions must drop below the V $_{T-}$  threshold before they affect the output.

The HC132 can be used as a direct replacement for the HC00 NAND gate, which does not have Schmitt-trigger capability. The HC132 has the same pin assignment as the HC00. Schmitt-trigger logic elements act as standard logic elements in the absence of noise or slow rise and fall times, making direct substitution possible.

Versatility and low cost are attractive features of CMOS Schmitt triggers. With six Schmitt triggers per HC14 package, one trigger can be used for a noise elimination application while the other five function as standard inverters. Similarly, each of the four triggers in the HC132 can be used as either Schmitt triggers or NAND gates or some combination of both.

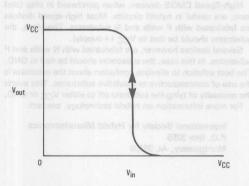


Figure 55. Standard Inverter Transfer Characteristic

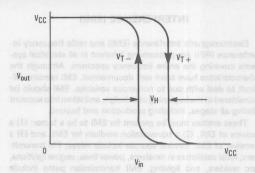


Figure 56. Schmitt-Trigger
Inverter Transfer Characteristic

Table 5. Schmitt-Trigger Devices

HC14	Hex Schmitt-Trigger Inverter
HC132	Quad 2-Input NAND Gate with Schmitt-Trigger Inputs
HC9014	Nine-Wide Schmitt-Trigger Inverter
HC9015	Nine-Wide Schmitt-Trigger Noninverting Buffer
HC9114	Nine-Wide Schmitt-Trigger Inverter with Open- Drain Outputs
HC9115	Nine-Wide Schmitt-Trigger Noninverting Buffer with Open-Drain Outputs

#### HC vs. HCT

Motorola's High-Speed CMOS is intended to give the designer an alternative to LSTTL. HSCMOS, with the faster speed advantage over metal-gate CMOS (MC14000 series) and the lower power consumption advantage over LSTTL, is an optimum choice for new midrange designs. With the advent of high-speed CMOS microprocessors and memories, the ability to design a 100% CMOS system is now possible.

HCT devices offer a short-term solution to the TTL/NMOSto-CMOS interface problem. To achieve this interface capability, some CMOS advantages had to be compromised. These compromises include power consumption, operating voltage range, and noise immunity.

In most cases HCT devices are drop-in replacements of TTL devices with significant advantages over the TTL devices. However, in some cases, an equivalent HCT device may not replace a TTL device without some form of circuit modification.

The wise designer uses HCT devices to perform logic level conversions only. In new designs, the designer wants all the advantages of a true CMOS system and designs using only HC devices.

# OSCILLATOR DESIGN WITH HIGH-SPEED CMOS

Oscillator design is a fundamental requirement of many systems and several types are discussed in this section. In general, an oscillator is comprised of two parts: an active network and a feedback network. The active network is usually in the form of an amplifier, or an unbuffered inverter, such as the HCU04. The feedback network is mainly comprised of resistors, capacitors, and depending upon the application, a quartz crystal or ceramic resonator.

Buffered inverters are never recommended in oscillator applications due to their high gain and added propagation delay. For this reason Motorola manufactures the HCU04, which is an unbuffered bex inverter.

Oscillators for use in digital systems fall into two general categories, RC oscillators and crystal or ceramic resonator oscillators. Crystal oscillators have the best performance, but are more costly, especially for nonstandard frequencies. RC oscillators are more useful in applications where stability and accuracy are not of prime importance. Where high performance at low frequencies is desired, ceramic resonators are sometimes used.

# RC OSCILLATORS

The circuit in Figure 57 shows a basic RC oscillator using the HCU04. When the input voltage of the first inverter reaches the threshold voltage, the outputs of the two inverters change state, and the charging current of the capacitor changes direction. The frequency at which this circuit oscillates depends upon R1 and C. The equation to calculate these component values is given in Figure 57.

Certain constraints must be met while designing this type of oscillator. Stray capacitance and inductance must be kept to a minimum by placing the passive components as close to the chip as possible. Also, at higher frequencies, the HCU04's

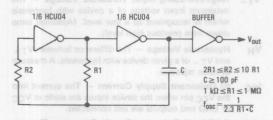


Figure 57. RC Oscillator

propagation delay becomes a dominant effect and affects the cycle time. A polystyrene capacitor is recommended for optimum performance.

#### CRYSTAL OSCILLATORS

Crystal oscillators provide the required stability and accuracy which is necessary in many applications. The crystal can be modeled as shown in Figure 58.

The power dissipated in a crystal is referred to as the drive level and is specified in mW. At low drive levels, the resonant resistance of the crystal can be so large as to cause start-up problems. To overcome this problem, the amplifier (inverter) should provide enough amplification, but not too much as to overdrive the crystal.

Figure 59 shows a Pierce crystal oscillator circuit, which is a popular configuration with CMOS.

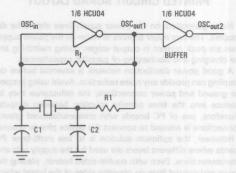
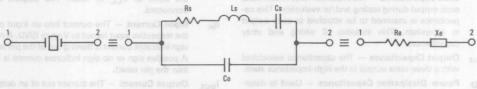


Figure 59. Pierce Crystal Oscillator Circuit

## Choosing R1

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 limits the drive level.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency at Osc Out 2. The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.



Values are supplied by the crystal manufacturer (parallel resonant crystal)

Figure 58. Equivalent Crystal Networks

# Selecting Re

The feedback resistor ( $R_f$ ) typically ranges up to 20 M $\Omega$ .  $R_f$  determines the gain and bandwidth of the amplifier. Proper bandwidth ensures oscillation at the correct frequency plus roll-off to minimize gain at undesirable frequencies, such as the first overtone.  $R_f$  must be large enough so as not to affect the phase of the feedback network in an appreciable manner.

# RECOMMENDED READING

D. Babin, "Designing Crystal Oscillators", Machine Design, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", Machine Design, April 25, 1985.

# PRINTED CIRCUIT BOARD LAYOUT

Noise generators on the power supply lines should be decoupled. The two major sources of noise on the power supply lines are peak current in output stages during switching and the charging and discharging of parasitic capacitances.

A good power distribution network is essential before decoupling can provide any noise reduction. Avoid using jumpers for ground and power connections; the inductance they introduce into the lines permits coupling between outputs. Therefore, use of PC boards with premanufactured ground connections is advised to connect the device pins to ground.

However, the optimum solution is to use multi-layer PC boards where different layers are used for the supply rails and interconnections. Even with double-sided boards, placing the power and ground lines on opposite sides of the board whenever possible is recommended. The multi-wire board is a less expensive approach than the multi-layer PC board, while retaining the same noise reduction characteristics. As a rule of thumb, there should be several ground pins per connector to give good ground distribution.

The precautions for ground lines also apply to V<sub>CC</sub> lines: 1) separate power stabilization for each board; 2) isolate noise sources; and 3) avoid the use of large, single voltage regulators.

After all of these precautions, decoupling is an added measure to reduce supply noise. See the **Decoupling Capacitors** section.

# GLOSSARY OF TERMS

- Cin Input Capacitance The parasitic capacitance associated with a given input pin.
- CL Load Capacitance The capacitor value which loads each output during testing and/or evaluation. This capacitance is assumed to be attached to each output in a system. This includes all wiring and stray capacitance.
- Cout Output Capacitance The capacitance associated with a three-state output in the high-impedance state.
- CPD Power Dissipation Capacitance Used to determine device dynamic power dissipation, i.e., PD = CPDVCC<sup>2</sup>f + VCCICC. See POWER SUPPLY SIZING for a discussion of CPD.

- fmax Maximum Clock Frequency The maximum clocking frequency attainable with the following input and output conditions being met:
  - Input Conditions (HC)  $t_r = t_f = 6$  ns, voltage swing from GND to  $V_{CC}$  with 50% duty cycle. (HCT)  $t_r = t_f = 6$  ns, voltage swing from GND to 3.0 V with 50% duty cycle.
  - Output Conditions (HC and HCT) waveform must swing from 10% of  $(V_{OH} V_{OL})$  to 90% of  $(V_{OH} V_{OL})$  and be functionally correct under the given load condition:  $C_{I} = 50$  pF, all outputs.
- V<sub>CC</sub> Positive Supply Voltage + dc supply voltage (referenced to GND). The voltage range over which ICs are functional.
- Vin Input Voltage DC input voltage (referenced to GND).
- Vout Output Voltage DC output voltage (referenced to GND).
- VIH Minimum High Level Input Voltage The worst case voltage that is recognized by a device as the HIGH state
- V<sub>IL</sub> Maximum Low Level Input Voltage The worst case voltage that is recognized by a device as the LOW
- WoH Minimum High Level Output Voltage The worst case high-level voltage at an output for a given output current (I<sub>Out</sub>) and supply voltage (V<sub>CC</sub>).
- Vol Maximum Low Level Output Voltage The worst case low-level voltage at an output for a given output current (I<sub>Out</sub>) and supply voltage (V<sub>CC</sub>).
- V<sub>T+</sub> Positive-Going Input Threshold Voltage The minimum input voltage of a device with hysteresis which is recognized as a high level. (Assumes ramp up from previous low level.)
- V<sub>T</sub> Negative-Going Input Threshold Voltage The maximum input voltage of a device with hysteresis which is recognized as a low level. (Assumes ramp down from previous high level).
- V<sub>H</sub> Hysteresis Voltage The difference between V<sub>T+</sub> and V<sub>T-</sub> of a given device with hysteresis. A measure of noise rejection.
- ICC IC Quiescent Supply Current The current into the V<sub>CC</sub> pin when the device inputs are static at V<sub>CC</sub> or GND and outputs are not connected.
- ΔICC Additional Quiescent Supply Current The current into the V<sub>CC</sub> pin when one of the device inputs is at 2.4 V with respect to GND and the other inputs are static at V<sub>CC</sub> or GND. The outputs are not connected.
- In Input Current The current into an input pin with the respective input forced to V<sub>CC</sub> or GND. A negative sign indicates current is flowing out of the pin (source). A positive sign or no sign indicates current is flowing into the pin (sink).
- Iout Output Current The current out of an output pin.
  A negative sign indicates current is flowing out of the
  pin (source). A positive sign or no sign indicates current
  is flowing into the pin (sink).

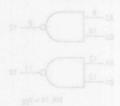
- I<sub>1H</sub> Input Current (High) The input current when the input voltage is forced to a high level.
- I<sub>|L</sub> Input Current (Low) The input current when the input voltage is forced to a low level.
- IOH Output Current (High) The output current when the output voltage is at a high level.
- IOL Output Current (Low) The output current when the output voltage is at a low level.
- Ioz Three-State Leakage Current The current into or out of a three-state output in the high-impedance state with that respective output forced to V<sub>CC</sub> or GND.
- tplh Low-to-High Propagation Delay (HC) The time interval between the 0.5 V<sub>CC</sub> level of the controlling input waveform and the 50% level of the output waveform, with the output changing from low level to high level. (HCT) The time interval between the 1.3 V level (with respect to GND) of the controlling input waveform and the 1.3 V level (with respect to GND) of the output waveform, with the output changing from low level to high level.
- tPHL High-to-Low Propagation Delay (HC) The time interval between the 0.5 V<sub>CC</sub> level of the controlling input waveform and the 50% level of the output waveform, with the output changing from high level to low level. (HCT) The time interval between the 1.3 V level (with respect to GND) of the controlling input waveform and the 1.3 V level (with respect to GND) of the output waveform, with the output changing from high level to low level.
- tpLz Low-Level to High-Impedance Propagation Delay (Disable Time) The time interval between the 0.5 V<sub>CC</sub> level for HC devices (1.3 V with respect to GND for HCT devices) of the controlling input waveform and the 10% level of the output waveform, with the output changing from the low level to high-impedance (off) state.
- tpHZ High-Level to High-Impedance Propagation Delay (Disable Time) The time interval between the 0.5 V<sub>CC</sub> level for HC devices (1.3 V with respect to GND for HCT devices) of the controlling input waveform and the 90% level of the output waveform, with the output changing from the high level to high-impedance (off) state.
- tpzL High-Impedance to Low-Level Propagation Delay (Enable Time) The time interval between 0.5 V<sub>CC</sub> level (HC) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% level (HC) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.
- tpzH High-Impedance to High-Level Propagation Delay (Enable Time) The time interval between the 0.5 V<sub>CC</sub> level (HC) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% level (HC) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a high level.
- **t**<sub>TLH</sub> Output Low-to-High Transition Time The time interval between the 10% and 90% voltage levels of the rising edge of a switching output.

- tTHL Output High-to-Low Transition Time The time interval between the 90% and 10% voltage levels of the falling edge of a switching output.
- tsu Setup Time The time interval immediately preceding the active transition of a clock or latch enable input, during which the data to be recognized must be maintained (valid) at the input to ensure proper recognition. A negative setup time indicates that the data at the input may be applied sometime after the active clock or latch transition and still be recognized. For HC devices, the setup time is measured from the 50% level of the clock or latch input waveform. For HCT devices, the setup time is measured from the 1.3 V level (with respect to GND) of the clock or latch input waveform to the 1.3 V level (with respect to GND) of the clock or latch input waveform.
- th Hold Time The time interval immediately following the active transition of a clock or latch enable input, during which the data to be recognized must be maintained (valid) at the input to ensure proper recognition. A negative hold time indicates that the data at the input may be changed prior to the active clock or latch transition and still be recognized. For HC devices, the hold time is measured from the 50% level of the clock or latch input waveform to the 50% level of the data waveform. For HCT devices, the hold time is measured from the 1.3 V level (with respect to GND) of the clock or latch input waveform to the 1.3 V level (with respect to GND) of the data waveform.
- trec Recovery Time (HC) The time interval between the 50% level of the transition from active to inactive state of an asynchronous control input and the 50% level of the active clock or latch enable edge required to guarantee proper operation of a device. (HCT) The time interval between the 1.3 V level (with respect to GND) of the transition from active to inactive state of an asynchronous control input and the 1.3 V level (with respect to GND) of the active clock or latch edge required to guarantee proper operation of a logic device.
- t<sub>w</sub> Pulse Width (HC) The time interval between 50% levels of an input pulse required to guarantee proper operation of a logic device. (HCT) The time interval between 1.3 V levels (with respect to GND) of an input pulse required to guarantee proper operation of a logic device.
- t<sub>r</sub> Input Rise Time (HC) The time interval between the 10% and 90% voltage levels on the rising edge of an input signal. (HCT) — The time interval between the 0.3 V level and 2.7 V level (with respect to GND) on the rising edge of an input signal.
- tf Input Fall Time (HC) The time interval between the 90% and 10% voltage levels on the falling edge of an input signal. (HCT) The time interval between the 2.7 V level and 0.3 V level (with respect to GND) on the falling edge of an input signal.





Data Sheets 5



# Quad 2-Input NAND Gate High-Performance Silicon-Gate CMOS

The MC54/74HC00 is identical in pinout to the LS00. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 32 FETs or 8 Equivalent Gates

# LOGIC DIAGRAM

A1 
$$\frac{1}{B1}$$
  $\frac{3}{2}$   $\frac{4}{B2}$   $\frac{4}{B2}$   $\frac{6}{B2}$   $\frac{6}{5}$   $\frac{7}{4}$   $\frac{10}{B4}$   $\frac{10}{13}$   $\frac{11}{A1}$   $\frac{11}{A2}$   $\frac{11}{A4}$   $\frac{12}{B4}$   $\frac{11}{B4}$   $\frac{11}{B4}$ 

# MC54/74HC00



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

# ORDERING INFORMATION

MC74HCXXN Plastic MC54HCXXJ Ceramic MC74HCXXD SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# PIN ASSIGNMENT

			1
A1 [	1 •	14	vcc
B1 [	2	13	] B4
Y1 [	3	12	] A4
A2 [	4	11	] Y4
B2 [	5	10	<b>B</b> 3
Y2 [	6	9	] A3
GND [	7	8	] Y3

# FUNCTION TABLE

Inp	uts	Output
Α	В	Y
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

# MAXIMUM BATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{In}$  and  $V_{Out}$  should be constrained to the range  $GND \leq (V_{In} \text{ or } V_{Out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	HADRO TEDS IN SILIGIN		Vcc	Guaranteed Limit			
Symbol	Parameter	Test Conditions		25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}} $ $ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=V <sub>CC</sub> or GND	6.0	±0.1	± 1.0	± 1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μΑ	6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

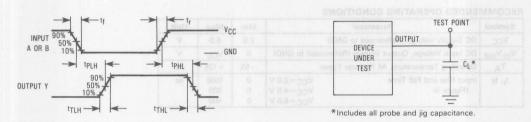
<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

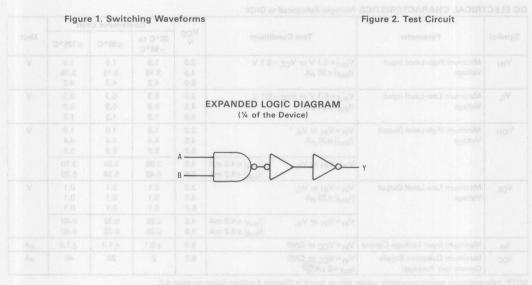
ites device contains protection		Birth Bulsy		1	Guaranteed Limit			bymaq.	
Symbol	deathy to guard again due to high static voltage	Parameter			V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Dela (Figures 1 and 2)	y, Input A or E	3 to Output Y		2.0 4.5 6.0	90 18 15	115 23 20	135 27 23	ns
tTLH, tTHL	Maximum Output Transition (Figures 1 and 2)	Time, Any Ou	itput	1982 Signific	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitano	е	1002	C Packaget	08-	10	10	10	pF

# NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	Europeign
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	more Of West Of .22	pF





# Quad 2-Input NOR Gate High-Performance Silicon-Gate CMOS

The MC54/74HC02 is identical in pinout to the LS02. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 40 FETs or 10 Equivalent Gates

# MC54/74HC02



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

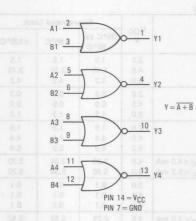
# ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# LOGIC DIAGRAM



# 

B1 0 3 12 0 B4 Y2 0 4 11 0 A4 A2 0 5 10 0 Y3 B2 0 6 9 0 B3 GND 0 7 8 0 A3

# FUNCTION TABLE

Inputs		Output
Α	В	Y
L	L	Н
L	Н	L
H	L	Da Lin
Н	Н	L

# MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
ICC	DC Supply Current, VCC and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65.to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \le |V_{in}$  or  $V_{out}| \le V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (R	eferenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0	1000 500 400	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	p a lity			V	Guaranteed Limit			
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Uni
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub>  I <sub>out</sub>   ≤20 μA	-0.1 V	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub>  I <sub>out</sub>  ≤20 μA	-0.1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	0	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	3 1	Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	± 1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA		6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

AC ELECTRICAL CHARACTERISTICS (C1 = 50 pF, Input tr = tf = 6 ns)

Symbol	Parameter	.,	Gua			
		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, Input A or B to Output Y	2.0	90	115	135	ns
tPHL	(Figures 1 and 2)	4.5	18	23	27	
101.162.0	CHOS (MAAN)	6.0	15	20	23	04-1
tTLH,	Maximum Output Transition Time, Any Output	2.0	75	95	110	ns
tTHL	(Figures 1 and 2)	4.5	15	19	22	MCSAL
MINISTER OF	tors, they are coronable with	6.0	13	16	19	in itiiw
Cin	Maximum Input Capacitance	-	10	10	10	pF

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

.0 V	Typical @ 25°C, V <sub>CC</sub> =5.0 V
pF	IGMM, 20MO 22 abetratel villous
	22 22 22 22 22 22 22 22 22 22 22 22 22

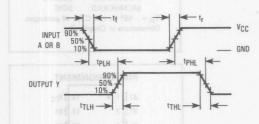
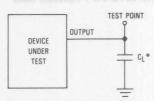


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM
(¼ of the Device)

# Quad 2-Input NAND Gate with Open-Drain Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC03 is identical in pinout to the LS03. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with

The HC03 NAND gate has, as its output, a high-performance MOS N-Channel transistor. This NAND gate can, therefore, with a suitable pullup resistor, be used in wired-AND applications. Having the output characteristic curves given in this data sheet, this device can be used as an LED driver or in any other application that only requires a sinking current.

- Output Drive Capability: 10 LSTTL Loads with Suitable Pullup Resistor
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 28 FETs or 7 Equivalent Gates



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

# ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD

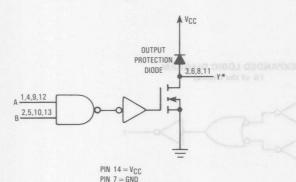
Plastic Ceramic SOIC

9 A3

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.



#### LOGIC DIAGRAM



<sup>\*</sup>Denotes open-drain outputs.

# 

Y2 [

GND [

#### 

Symbol	firms beginning Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\text{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions. †Derating — Plastic DIP:  $-10 \text{ mW/}^{\circ}\text{C}$  from 65° to 125°C

Ceramic DIP: - 10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Paramete	r	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced t	o GND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage	e (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Packa	age Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(rigule i)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	admentioned by the section in	shulant® 21	ntolenn	Guaranteed Limit			1414
Symbol	Parameter August Company	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V, I <sub>out</sub> =0 μA or V <sub>out</sub> =V <sub>CC</sub> -0.1 V, R <sub>pu</sub> per Figure 2	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	$V_{out}$ =0.1 V, $I_{out}$ =0 μA or $V_{out}$ = $V_{CC}$ -0.1 V, $R_{pu}$ per Figure 2	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
VOL Maximum Low-Level Output Voltage		V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40		
lin	Maximum Input Leakage Current	Vin=V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	2	20	40	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  Vin = VIL or VIH  Vout = VCC or GND	6.0	±0.5	±5.0	± 10.0	μА

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	This device contains object to great again the to High stelle voltage	Parameter	.,,	Gua	Symbia		
			VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLZ,	Maximum Propagation Del	ay, Input A or B to Output Y	2.0	125	155	190	ns
tPZL	(Figures 1 and 2)		4.5 6.0	25 21	31 26	38 32	off
tTHL	Maximum Output Transitio	n Time, Any Output	2.0	75	95	110	ns
et of ban	(Figures 1 and 2)		4.5	15	19	22	201
	eV to mittle GVD sprin		6.0	13	16	19	OS.
Cin	Maximum Input Capacitano	ce CCB I Tarrocks	3 087	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Out State)	put Capacitance (Output in High-Impedance	9 -	10	10	10	pF

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	SOUTH THE BUILDING TO SEE THE	
	PD = CPD VCC <sup>2</sup> f + ICC VCC	frequency of he 8 y local considerations; as	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

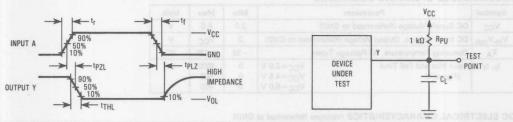
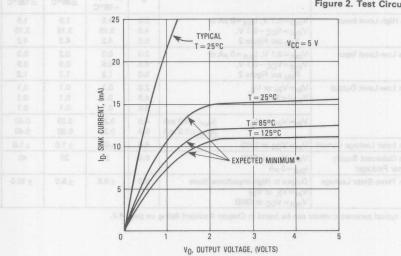


Figure 1. Switching Waveforms

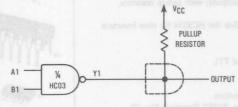
\*Includes all probe and jig capacitance.

# Figure 2. Test Circuit



\*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics



Output = Y1 • Y2 • ... • Yn

= A1B1•A2B2•...•AnBn

An -1/4 HC03

Y2

1/4

HC03

ИОСТАМИНОЯМ DE B2 -

LED 1 -

LED 2-

LED

ENABLE

LED Driver with Blanking

VCC A VCC A + V<sub>R</sub> ≥ Design Example 1/4 1/4 Conditions: I<sub>D</sub> ≅ 10 mA HC03 HC03 Using Figure 3 typical curve, @  $I_D = 10$  mA,  $V_{DS} \cong 0.4$  V

 $\therefore R = \frac{V_{CC} - V_F - V_O}{V_{CC} - V_F - V_O}$  $=\frac{5 V-1.7 V-0.4 V}{1}$ 10 mA

= 290  $\Omega$ 

Use R = 270  $\Omega$ 

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC04 is identical in pinout to the LS04 and the MC14069. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six three-stage inverters. See the HC9034 for nine inverters in one package.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 36 FETs or 9 Equivalent Gates

14

J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



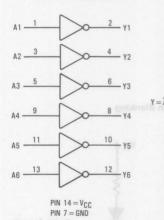
D SUFFIX SOIC CASE 751A

# ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# LOGIC DIAGRAM



# 

# **FUNCTION TABLE**

Inputs A	Outputs
L	Н
Н	L

# MAXIMUM BATINGS\*

IAAIIVIO	IVI RATINGS*	到 75年至一位,1997年,199	
Symbol	Mink I book Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	or V. Jug
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	o o°C an

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \le (V_{in} \text{ or } V_{out}) \le VCC$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Paramet	er		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)			2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)			0	Vcc	V
TA	Operating Temperature, All Pac	Operating Temperature, All Package Types			+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	30/V30 K20WU	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

			Vcc	Guaranteed Limit			
Symbol	Parameter	Test Conditions		25°C to -55°C	≤85°C	≤125°C	Uni
VIH	Minimum High-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	$V_{\text{out}} = V_{\text{CC}} - 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
VOH Minimum High-Level Ou Voltage	Minimum High-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
		$V_{in} = V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$		0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	6.0	±0.1	±1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 µA	6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Value Units This device contains p				Gua				
	teniena brave of yrituata o	Parameter	meter 6.7 - Ar 6.0 -		VCC	25°C to	<85°C	≤125°C	Unit
	Sharpest - suggested stated   W   Although the Although			(0)	-55°C	≥00 C	≥ 125 C		
tPLH,	Maximum Propagation Delay	, Input A to Outpu	t Y		2.0	95	120	145	ns
tPHL	(Figures 1 and 2)	Am			4.5	19	24	29	
sunsber	rol-daid sidt of augustov				6.0	16	20	25	
tTLH,	Maximum Output Transition	Time, Any Output	200		2.0	75	95	110	ns
THL	(Figures 1 and 2)				4.5	15	19	22	
3073	Arue V so niVia divid appar				6.0	13	16	19	
Cin	Maximum Input Capacitance		000	Tegalice*	3108	10	10	10	pF

# NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Inverter)	ne Recousmende	Typical @ 25°C, V <sub>CC</sub> =5.0 V	Isroitonu
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	1 to 125°C 100° to 125°C 15° to 125°C	20	pF

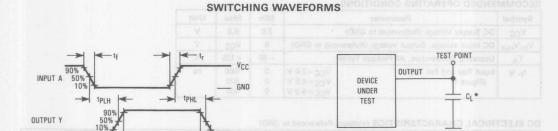


Figure 1

tTLH->

tTHL ->

\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

# (1/6 of Device Shown)

# Advance Information

# Hex Inverter with LSTTL-Compatible Inputs

**High-Performance Silicon-Gate CMOS** 

The MC54/74HCT04 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT04 is identical in pinout to the LS04.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 48 FETs or 12 Equivalent Gates

# MC54/74HCT04



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



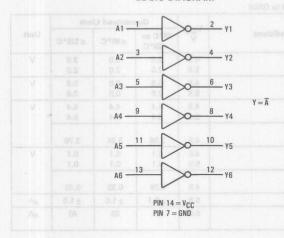
D SUFFIX SOIC CASE 751A

# ORDERING INFORMATION

MC74HCTXXN MC54HCTXXJ MC74HCTXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# LOGIC DIAGRAM



# PIN ASSIGNMENT A1 [ 1 • 14 ] V<sub>CC</sub> Y1 [ 2 13 ] A6 A2 [ 3 12 ] Y6 Y2 [ 4 11 ] A5 A3 [ 5 10 ] Y5 Y3 [ 6 9 ] A4 GND [ 7 8 ] Y4

# **FUNCTION TABLE**

Inputs	Outputs
L 9	Н
H	L

This document contains information on a new product. Specifications and information herein are subject to change without notice.

	m	
L	-	ч
г	w	л
	_	

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Not 3 7851 of 428 - TA Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
tr, tf	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

					Gua	imit		
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Uni
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V  l <sub>out</sub>  ≤20 μA	\$1	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	٧
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =V <sub>CC</sub> -0.1 V  I <sub>out</sub>  ≤20 μA	17-0	4.5 5.5	0.8	0.8	0.8	٧
Vон	Minimum High-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \le 20 \mu A$	14	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
	FUNCTION TA	V <sub>in</sub> =V <sub>IL</sub>  I <sub>out</sub>  ≤4.0 mA		4.5	3.98	3.84	3.70	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤20 μA		4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
	H	V <sub>in</sub> =V <sub>IH</sub>  I <sub>out</sub>  ≤4.0 mA	81,	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		5.5	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		5.5	2	20	40	μΑ

ΔICC	Additional Quiescent Supply	V <sub>in</sub> =2.4 V, Any One Input		≥ -55°C	25°C to 125°C	
	Current	Vin=VCC or GND, Other Inputs		Extra degrada in the contraction of		
		I <sub>out</sub> =0 μA	5.5	2.9	2.4	mA

# NOTES:

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5.0 V ± 10%, C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter 19319VII	Guaranteed Limit			
		25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	20	25	30	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 2)	15	19	22	ns
Cin	Maximum Input Capacitance	10	10	10	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Inverter)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	ugnt v
	Used to determine the no-load dynamic power consumption:	a Lamonity Characteristic of CIADS O	ensa n
	PD=CPD VCC2f+ICC VCC	22	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	was in the second of the second of the second	

# **SWITCHING WAVEFORMS**

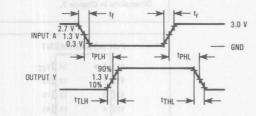
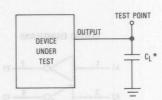


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM (1/6 of Device Shown)

# Hex Unbuffered Inverter High Performance Silicon-Gate CMOS

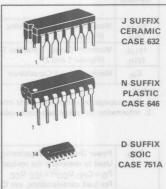
The MC54/74HCU04 is identical in pinout to the LSO4 and the MC14069UB. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six single-stage inverters. These inverters are well suited for use as oscillators, pulse shapers, and in many other applications requiring a high-input impedance amplifier. For digital applications, the HC04 is recommended.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V; 2.5 to 6 V in Oscillator Configurations
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 12 FETs or 3 Equivalent Gates

# A1 1 2 Y1 A2 3 4 Y2 A3 5 6 Y3 A4 9 8 Y4 A5 11 10 Y5 A6 13 12 Y6 PIN 14 = VCC PIN 7 = GND

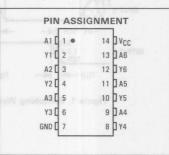
### MC54/74HCU04



### ORDERING INFORMATION

MC74HCUXXN Plastic MC54HCUXXJ Ceramic MC74HCUXXD SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.



# Inputs Outputs A Y L H

L

Н

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND  $\leq$  (Vin or Vour)  $\leq$  VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	-	No Limit	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	sent model, the contract in			V	Guaranteed Limit			
Symbol	Parameter 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit	
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.5 V*  I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	1.7 3.6 4.8	1.7 3.6 4.8	1.7 3.6 4.8	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =V <sub>CC</sub> −0.5 V*  I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	0.3 0.8 1.1	0.3 0.8 1.1	0.3 0.8 1.1	٧
VOH Minimum High-Level Output Voltage		$V_{in} = GND$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	1.8 4.0 5.5	1.8 4.0 5.5	1.8 4.0 5.5	V
		V <sub>in</sub> = GND	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.86 5.36	3.76 5.26	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{CC}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	0.2 0.5 0.5	0.2 0.5 0.5	0.2 0.5 0.5	V
		V <sub>in</sub> = V <sub>CC</sub>	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.32 0.32	0.37 0.37	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	± 0.1	±1.0	± 1.0	μΑ
ICC	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>OUt</sub> = 0 μA		6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

\*For  $V_{CC} = 2.0 \text{ V}$ ,  $V_{out} = 0.2 \text{ V}$  or  $V_{CC} - 0.2 \text{ V}$ .

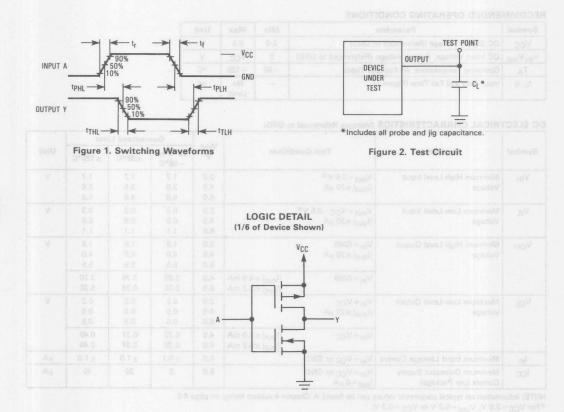
<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

Symbol	This downer contents	Value Unit		Gu	ipdentyl		
	anlage braug of visites of against out	Parameter A 4 m 1 d 1	V	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Dela (Figures 1 and 2)	y, Input A to Output Y	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
tTLH, tTHL	Maximum Output Transition (Figures 1 and 2)	Time, Any Output	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	100	1 Taylor 310 <u>8</u>	10	10	10	pF

### NOTES:

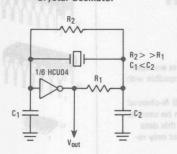
- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Inverter)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	innoitant
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	St of 980 ment 20 years 15 400 persons	pF

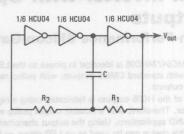


### TYPICAL APPLICATIONS

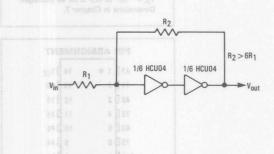
### **Crystal Oscillator**



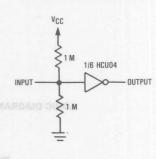
Stable RC Oscillator



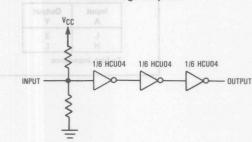
### Schmitt Trigger



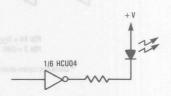
High Input Impedance Single-Stage Amplifier with a 2 to 6 V Supply Range



### Multi-Stage Amplifier



**LED Driver** 



For reduced power supply current, use high-efficiency LEDs such as the Hewlett-Packard HLMP series or equivalent.

### Product Preview

### **Hex Inverter with Open-Drain Outputs**

### **High-Performance Silicon-Gate CMOS**

The MC54/74HC05 is identical in pinout to the LS05. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each of the HC05 outputs is fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable output pullup resistor, this gate can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

- Output Drive Capability: 10 LSTTL Loads with Suitable Pullup Resistor
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 36 FETs or 9 Equivalent Gates

### MC54/74HC05



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

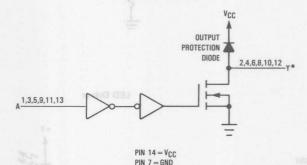
### ORDERING INFORMATION

MC74HCXXN Plastic MC54HCXXJ MC74HCXXD

Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM



\*Denotes open-drain outputs.

### PIN ASSIGNMENT 14 VCC 13 A6 12 1 Y6 A2 [ 11 DA5 Y2 [ 10 Y5 9 A4 Y3 [ 8 1 Y4 GND [

### **FUNCTION TABLE**

Input A	Output
L	Z
Н	L

Z=high impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	٧
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V	0	1000 500	ns
	The same of the sa	V <sub>CC</sub> =6.0 V	0	400	

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Figure 2. Test Circuit		amnot	Guaranteed Limit			
Symbol	Parameter	Test Conditions	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input $V_{out}$ = 0.1 V 2.0 Voltage $ I_{out} $ ≤ 20 μA 4.5	I <sub>out</sub>   ≤20 μA		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	$V_{\text{out}} = V_{\text{CC}} - 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu\text{A}$ $R_{\text{pu}}$ per Figure 2		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 µA	6.0	2	20	40	μΑ
loz	Maximum Output Leakage Current	A = V <sub>IL</sub> V <sub>out</sub> = V <sub>CC</sub> or GND		±0.5	±5.0	± 10.0	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

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Symbol	This device contains aircuity to dustd again due to high static voltage	Parameter CX + or 8.0-	1,,	Projected Limit			odmy8	
				VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tpLZ, Maximum Propagation Dela (Figures 1 and 2)	y, Input A to Output	Y/ co d.0 -	2.0	100	125	150	ns	
	(Figures 1 and 2)			4.5 6.0	20 17	25 21	30 26	m <sup>1</sup>
†THL	Maximum Output Transition Time, Any Output		2.0	75	95	110	ns	
	(Figures 1 and 2)			4.5	15	19	22	231
anVel-	agV 10 mV) ≥ GMD egnan			6.0	13	16	19	419
Cin	Maximum Input Capacitano	е	000 tegato	_501C P8	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Outp State)	out Capacitance (Out	put in High-Impedance	-	10	10	10	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Inverter)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	University of
	Used to determine the no-load dynamic power consumption:  PD = CPD VCc <sup>2</sup> f+I <sub>CC</sub> VCC	TBD	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	normission of the Copy to American	ngiiPio-i

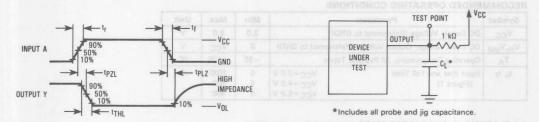
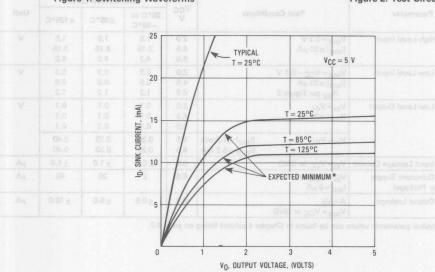


Figure 1. Switching Waveforms

Figure 2. Test Circuit



<sup>\*</sup>The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics

### MC54/74HCT05

Product Preview

### **Hex Inverter with Open-Drain Outputs and LSTTL-Compatible** Inputs

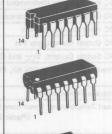
**High-Performance Silicon-Gate CMOS** 

The MC54/74HCT05 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT05 is identical in pinout to the LS05.

Each of the HCT05 outputs is fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable output pullup resistor, this gate can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

- Output Drive Capability: 10 LSTTL Loads with Suitable Pullup Resistor
- TTL/NMOS-Compatible Input Levels
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 48 FETs or 12 Equivalent Gates



J SUFFIX CERAMIC CASE 632

N SUFFIX PLASTIC **CASE 646** 



D SUFFIX SOIC CASE 751A

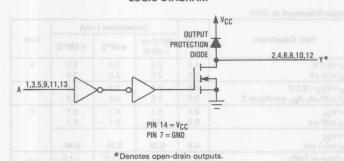
### **ORDERING INFORMATION**

MC74HCTXXN MC54HCTXXJ MC74HCTXXD

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM



PIN ASSIGNMENT 14 D VCC 13 A6 12 1Y6 A2 [ 11 A5 Y2 1 4 10 Y5 A3 [ Y3 [ 9 A4 8 1 Y4 GND [

### **FUNCTION TABLE**

Input	Output
m Oujean	Z
H	nemu L

Z = high impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice

### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit	
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V	
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V	
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V	
lin	DC Input Current, per Pin	±20	mA	
lout	DC Output Current, per Pin	±25	mA	
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA	
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW	
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C	
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
tr, tf	Input Rise and Fall Time (Figure 1)	0	500	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	A2 [] 3 [2]		.,	Gua	imit		
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$ , $R_{pu}$ per Figure 2	4.5 5.5	0.8	0.8	0.8	٧
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{iH}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
3.1	FUNCTION TAL	$V_{in} = V_{IH}$ $ I_{out}  \le 4.0 \text{ mA}$	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	5.5	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 µA	5.5	2	20	40	μΑ
loz	Maximum Output Leakage Current	A=V <sub>IL</sub> V <sub>out</sub> =V <sub>CC</sub> or GND	5.5	±0.5	±5.0	± 10.0	μΑ

ΔICC	Additional Quiescent Supply	Vin=2.4 V, Any One Input		≥ -55°C	25°C to 125°C	
	Current	Vin = VCC or GND, Other Inputs				
		I <sub>out</sub> =0 μA	5.5	2.9	2.4	mA

### NOTES

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

			Projected Limit				
Symbol	Parameter	25°C to -55°C	≤85°C	≤125°C	Unit		
tPLZ, tPZL	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	22	28	33	ns		
<sup>†</sup> THL	Maximum Output Transition Time, Any Output (Figures 1 and 2)	10	19	22	ns		
Cin	Maximum Input Capacitance	10	10	10	pF		
Cout	Maximum Three-State Output Capacitance (Output in High-Impedance State)	10	10	10	pF		

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Inverter)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC	TBD	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

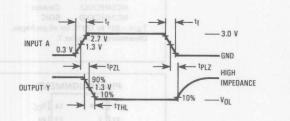
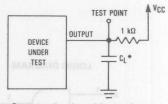
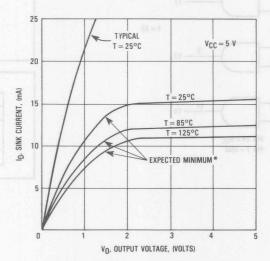


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit



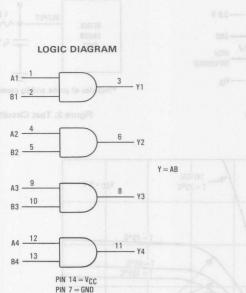
\*The expected minimum curves are not guarantees, but are design aids.

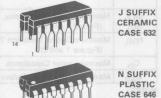
Figure 3. Open-Drain Output Characteristics

# Quad 2-Input AND Gate High-Performance Silicon-Gate CMOS

The MC54/74HC08 is identical in pinout to the LS08. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 24 FETs or 6 Equivalent Gates







D SUFFIX SOIC CASE 751A

### ORDERING INFORMATION

 $\begin{array}{ccc} \text{MC74HCXXN} & \text{Plastic} \\ \text{MC54HCXXJ} & \text{Ceramic} \\ \text{MC74HCXXD} & \text{SOIC} \\ T_A = -55^{\circ} \text{ to } 125^{\circ}\text{C} \text{ for all packages.} \\ \text{Dimensions in Chapter 7.} \end{array}$ 

### 

### **FUNCTION TABLE**

	Inp	uts	Output
	Α	В	Υ
Γ	L	L	L
	L	Н	L
1	Н	L	L
	Н	Н	Н

JAXIMU	M RATINGS*	the state of thought the lad	H JUST TOO
Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level

(e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter				Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)				6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)			0	Vcc	V
TA	Operating Temperature, All	Operating Temperature, All Package Types			+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	338V90 938V91	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

			No.		Guaranteed Limit			14
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	4	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	± 0.1	± 1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

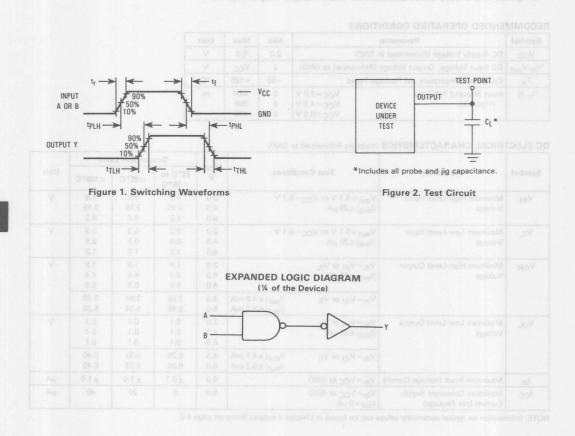
AC ELECTRICAL CHARACTERISTICS (C1 = 50 pF, Input tr = tf = 6 ns)

	This device contains		vialu sulleV			Gua	mit	Symbol	
Symbol	closuitor to guerd again due to high stade voltage	Parameter			VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay (Figures 1 and 2)	, Input A or B to O	utput Y		2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
tTLH, tTHL	Maximum Output Transition (Figures 1 and 2)	Time, Any Output	48.2	PSK) mentu	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance		000	Tegelos 1 O	08-	10	10	10	pF

### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	MATTER STATE
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	20 20 20 20	pF



# **Triple 3-Input NAND Gate**High-Performance Silicon-Gate CMOS

The MC54/74HC10 is identical in pinout to the LS10. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 36 FETs or 9 Equivalent Gates

### MC54/74HC10



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



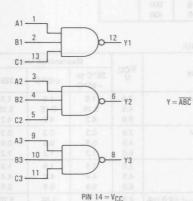
D SUFFIX SOIC CASE 751A

### ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM



PIN 7 = GND

### PIN ASSIGNMENT

PIN	ASSI	GNME	INI
A1 [	1 •	14	vcc
B1 [	2	13	] C1
A2 [	3	12	] Y1
B2 [	4	11	] C3
C2 [	5	10	] B3
Y2 [	6	9	] A3
GND [	7	8	] Y3

5

### FUNCTION TABLE

	Inputs	60,000	Output
Α	В	С	Y
L	X	X	Н
X	L	X	Н
X	X	L	H
Н	Н	Н	L

0	)	
-	-	20

-,	r arameter	value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	OMDS Define

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \subseteq (V_{in} \text{ or } V_{out}) \subseteq \mathsf{VCC}$ . Unused inputs must always be tied

to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	not Deast of and A Parameter		Min	Max	Unit
VCC	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	d to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	a hea			Gua	aranteed L	imit	Unit
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤ 20 μA		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤20 μA		1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	0 8 A	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$		3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ m}$ $ I_{out}  \le 5.2 \text{ m}$		0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

### AC ELECTRICAL CHARACTERISTICS (CL = 50 pF Input t<sub>r</sub> = t<sub>f</sub> = 6 ps)

Symbol			Gua	aranteed Li		
	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 1 and 2)	2.0 4.5 6.0	95 19 16	120 24 20	145 29 25	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	JYY bes	10	10	10	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	25	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

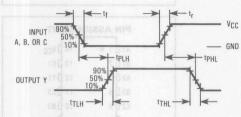
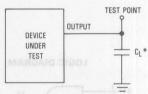


Figure 1. Switching Waveforms

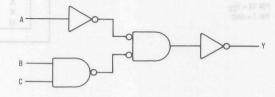


\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

5

### EXPANDED LOGIC DIAGRAM (1/3 of the Device)



# **Triple 3-Input AND Gate**High-Performance Silicon-Gate CMOS

The MC54/74HC11 is identical in pinout to the LS11. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 60 FETs or 15 Equivalent Gates

### MC54/74HC11



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

### ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD Plastic Ceramic SOIC

MC74HCXXD SOIC  $T_A = -55^{\circ}$  to 125°C for all packages.

Dimensions in Chapter 7.

### LOGIC DIAGRAM

$$\begin{array}{c|c}
A1 & \frac{1}{2} \\
B1 & \frac{1}{13}
\end{array}$$





PIN  $14 = V_{CC}$ PIN 7 = GND

### PIN ASSIGNMENT

1	71001		1
A1 [	1 •	14	Jvcc
B1 [	2	13	] C1
A2 [	3	12	] Y1
B2 [	4	11	] C3
C2 [	5	10	] B3
Y2 [	6	9	1 A3
GND [	7	8	] Y3

### **FUNCTION TABLE**

	Inputs		Output	
	Α	В	С	Υ
T	L	X	X	L
1	X	L	X	L
1	X	X	L	L
1	Н	Н	Н	Н

### MAXIMUM BATINGS\*

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	٧
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$   $(V_{in}$  or  $V_{out}) \leq$   $V_{CC}$ . Unused inputs must always be tied

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C Ceramic DIP: - 10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	/ <sub>CC</sub> =2.0 V / <sub>CC</sub> =4.5 V / <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

### DC FLECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				V	Guaranteed Limit			
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Uni
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤ 20 μA		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V	
			$I_{\text{out}} \le 4.0 \text{ mA}$ $I_{\text{out}} \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu A$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
	V <sub>in</sub> = V <sub>IH</sub> o		$I_{out}$ $\leq 4.0 \text{ mA}$ $I_{out}$ $\leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	± 1.0	± 1.0	μΑ
ICC	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

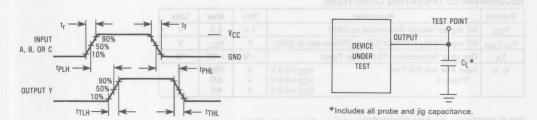
<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operation Conditions.

	This device contains				1,, 1	Gua	mit	Symbol	
Symbol	Paramete	Parameter	er 0.1+ crd.0-	VCC	25°C to -55°C	≤85°C	≤125°C	Unit	
tpLH, Maximum Propagation Delay, Input A, B, or C to Output Y				2.0	125	155	190	ns	
tpHL (Figures 1 and 2)					4.5 6.0	25 21	31 26	38 32	mi
tTLH,	Maximum Output Transition	Time, Any Output			2.0	75	95	110	ns
tTHL	(Figures 1 and 2)				4.5	15	19	22	30
DOVE I	Nov to niViz GVID egnisi Veni			6.0	13	16	19	-09	
Cin	Maximum Input Capacitance		000	Packinger	0.68	10	10	10	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	Function
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	on "O mont 3°\Wint 0127 - 910 quant + -	pF



# Hex Schmitt-Trigger Inverter High-Performance Silicon-Gate CMOS

The MC54/74HC14 is identical in pinout to the LS14, LS04, and HC04. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The MC54/74HC14 is useful to "square up" slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the HC14 finds applications in noisy environments.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 60 FETs or 15 Equivalent Gates

### MC54/74HC14

14

J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

### ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM

PIN 14 = V<sub>CC</sub> PIN 7 = GND

### PIN ASSIGNMENT

PIN	ASSI	GIVIVIE	IN I
A1 [	1 • /	14	J v <sub>CC</sub>
Y1 [	2	13	] A6
A2 [	3	12	] Y6
Y2 [	4	11	] A5
A3 [	5	10	] Y5
Y3 [	6	9	] A4
GND [	7	8	] Y4

### **FUNCTION TABLE**

Input	Output
A	Y
L	Н
H (8. se	L

### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	٧
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	2.0	6.0	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	-	No Limit*	ns

<sup>\*</sup>When Vin = 50% Vcc, Icc>1 mA.

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	re silvey		W	Gua	imit		
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
V <sub>T+</sub> max	Maximum Positive-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> =0.1 V  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	1.50 3.15 4.20	1.50 3.15 4.20	1.50 3.15 4.20	V
V <sub>T+</sub> min	Minimum Positive-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> =0.1 V  l <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.00 2.30 3.00	0.95 2.25 2.95	0.95 2.25 2.95	٧
V <sub>T</sub> _max	Maximum Negative-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> =V <sub>CC</sub> -0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.90 2.00 2.60	0.95 2.05 2.65	0.95 2.05 2.65	٧
V <sub>T</sub> _ min	Minimum Negative-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> =V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	0.30 0.90 1.20	0.30 0.90 1.20	0.30 0.90 1.20	٧
V <sub>H</sub> max Note 2	Maximum Hysteresis Voltage (Figure 3)	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	1.20 2.25 3.00	1.20 2.25 3.00	1.20 2.25 3.00	٧
V <sub>H</sub> min Note 2	Minimum Hysteresis Voltage (Figure 3)	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.20 0.40 0.50	0.20 0.40 0.50	0.20 0.40 0.50	٧

### NOTES

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2.  $V_H min > (V_T + min) (V_T max); V_H max = (V_T + max) (V_T min).$

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

### DC ELECTRICAL CHARACTERISTICS (Continued)

				V	Gua	ranteed Li	mit	
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
		V <sub>in</sub> ≤V <sub>T</sub> _min  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	Vin	$V_{in} \le V_{T-min}$	I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> ≥V <sub>T+</sub> max  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	0.9	V <sub>in</sub> ≥V <sub>T+</sub> max	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	W TATION ASSISTED AND A CONTRACT AND	6.0	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	100 + 310 = 0410A	6.0	2	20	40	μΑ

### NOTES

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2.  $V_H min > (V_T + min) (V_T max); V_H max = (V_T + max) (V_T min).$

### AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

Symbol			Gua			
	Parameter 38004 MUNICIPAL SHOOMY YTHROCE A 188	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	100-	10	10	10	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Inverter)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	22	pF

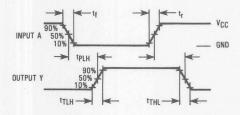
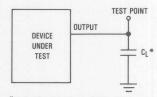


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

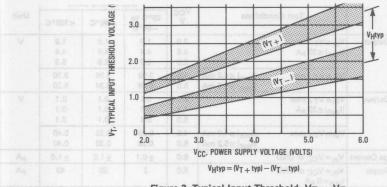
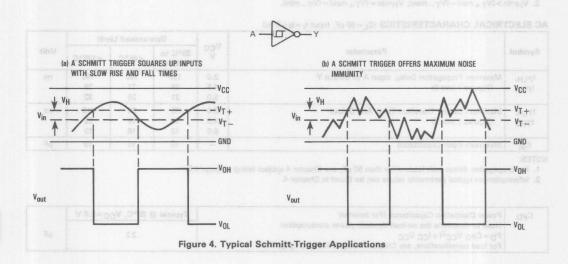


Figure 3. Typical Input Threshold, V<sub>T+</sub>, V<sub>T-</sub>
Versus Power Supply Voltage



### **Dual 4-Input NAND Gate High-Performance Silicon-Gate CMOS**

The MC54/74HC20 is identical in pinout to the LS20. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 28 FETs or 7 Equivalent Gates

### MC54/74HC20



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC **CASE 646** 



D SUFFIX SOIC CASE 751A

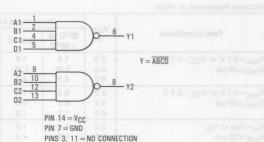
### ORDERING INFORMATION

MC74HCXXN Plastic MC54HCXX.J MC74HCXXD SOIC

Ceramic

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM



### PIN ASSIGNMENT 14 VCC B1 [ 13 D2 12 C2 NC 3 11 DNC C1 [ 10 B2 D1 0 5 9 A2 Y1 6 8 Y2 GND [

NC = NO CONNECTION

### **FUNCTION TABLE**

		Inp	Output		
	Α	В	С	D	Y H
	L	X	X	X	Н
10.	X	L	X	X	H V
	X	X	L	X	H
	X	X	X	L	Н
	Н	Н	Н	H	L

### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
VCC	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vourt) ≤ VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Re	ferenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package T	ypes	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0	1000 500 400	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	4.000				Guaranteed Limit			
Symbol	Parameter	Test Cor	nditions	VCC	25°C to -55°C	≤85°C	≤125°C	Uni
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $  I_{out}   \le 20 \mu\text{A}$		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	6 3 6 A	Vin=VIH or VIL	I <sub>out</sub>   ≤4.0 mA  I <sub>out</sub>   ≤5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{Out}}  \le 20 \ \mu\text{A}$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	A A A A	Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	± 0.1	± 1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA		6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

### AC ELECTRICAL CHARACTERISTICS ( $C_1 = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

		.,	Gua			
Symbol	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, Input A, B, C, or D to Output Y		90	115	135	ns
tPHL	(Figures 1 and 2)	4.5	18	23	27	
	527. The device inputs are com-	6.0	15	20	23	COM or
tTLH,	Maximum Output Transition Time, Any Output	2.0	75	95	110	ns
tTHL	(Figures 1 and 2)	4.5	15	19	22	
BASN		6.0	13	16	19	. mintral
Cin	Maximum Input Capacitance	us <del>d</del> ior	10	10	10	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	26	pF

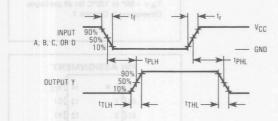
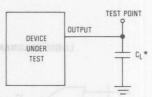


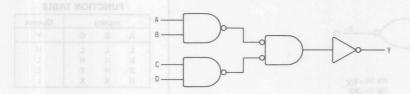
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

### EXPANDED LOGIC DIAGRAM (1/2 of the Device)



The MC54/74HC27 is identical in pinout to the LS27. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 42 FETs or 10.5 Equivalent Gates

14

J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



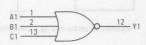
D SUFFIX SOIC CASE 751A

### ORDERING INFORMATION

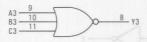
MC74HCXXN MC54HCXXJ MC74HCXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

LOGIC DIAGRAM







PIN 14 = V<sub>CC</sub> PIN 7 = GND PIN ASSIGNMENT

A1 [	1 •	14	VCC
B1 [	2	13	] C1
A2 [	3	12	Y1
B2 [	4	. 11	] C3
C2 [	5	10	] B3
Y2 [	6	9	] A3
GND [	7	8	] Y3

**FUNCTION TABLE** 

L		Inputs		Output
	Α	В	С	Y
	L	L	L	Н
	X	X	Н	L
	X	Н	X	L
	Н	X	X	L

IAAIIVIO	W NATINGS"	tilled and be also begins and	
Symbol	timid books Parameter	Value	Unit
VCC	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	N V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	dec man

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{\rm in}$  and  $V_{\rm out}$  should be constrained to the range GND  $\leq$  ( $V_{\rm in}$  or  $V_{\rm out}$ )  $\leq$   $V_{\rm CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{\rm CC}$ ). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	V <sub>CC</sub> DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	Vin, Vout DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	٧
TA	Operating Temperature, All Package Ty	pes	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	gure 2. Test Circuit	9			Guaranteed Limit			1 1 1 1
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} = 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
Vон	Minimum High-Level Output Voltage	I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	1-	Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$		4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	± 0.1	± 1.0	± 1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA		6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

### AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	This device contains p		Veltus Unit			Gua	-lodney2		
Symbol	due to bigh state voltages to	Parameter			V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay	, Input A, B, or C t	to Output Y		2.0	90	115	135	ns
tPHL	(Figures 1 and 2)				4.5 6.0	18 15	23 20	27 23	fire
tTLH,	Maximum Output Transition	Time, Any Output	50.3		2.0	75	95	110	ns
†THL	(Figures 1 and 2)				4.5	15	19	22	- 331
-paVz	(neg ChiD ≤ IVig or Vour)		1007	3910 ble	6.0	13	16	19	.03
Cin	Maximum Input Capacitance		906	Topakin	3108	10	10	10	pF

### NOTES:

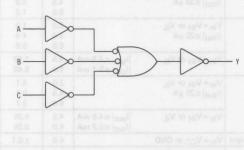
- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	Street Street Street Street Street Street	
	PD = CPD VCC2f + ICC VCC	27	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	to be the read from the constant field	



Figure 1. Switching Waveforms Figure 2. Test Circuit





### MC54/74HC30

# 8-Input NAND Gate High-Performance Silicon-Gate CMOS

The MC54/74HC30 is identical in pinout to the LS30. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 32 FETs or 8 Equivalent Gates



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

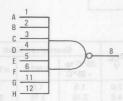
### ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM



 $Y = \overline{ABCDEFGH}$ 

PINS 9, 10, 13 = NO CONNECTION

PIN 14 = V<sub>CC</sub> PIN 7 = GND PIN ASSIGNMENT

A [ 1 • 14 ] VCC
B [ 2 13 ] NC
C [ 3 12 ] H
D [ 4 11 ] G
E [ 5 10 ] NC
F [ 6 9 ] NC
GND [ 7 8 ] Y

NC = NO CONNECTION

### **FUNCTION TABLE**

Inputs A through H	Output
All inputs H	L
One or more inputs L	Н

L	5
ζ	J

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq \mathsf{VCC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions. The Application of the Recommended Operating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	ed to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V	0	1000 500	ns
	A - Na	VCC = 6.0 V	0	400	

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Parameter Test Conditions		mentions	. 8	Guaranteed Limit			
Symbol			VCC	25°C to -55°C	≤85°C	≤125°C	Unit	
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub>  I <sub>out</sub>   ≤20 μA	-0.1 V	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub>  I <sub>out</sub>   ≤ 20 μA	-0.1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	Inputs A through H	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	± 0.1	± 1.0	± 1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$		6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

### AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

			Guaranteed Limit			
Symbol	Parameter	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	ww. 26	10	10	10	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	27	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

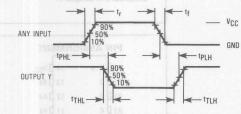
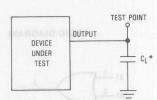


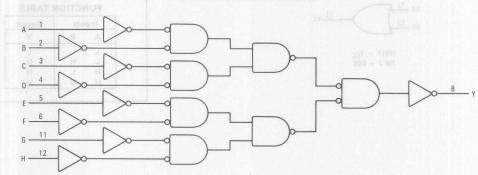
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

### EXPANDED LOGIC DIAGRAM



# Quad 2-Input OR Gate High-Performance Silicon-Gate CMOS

The MC54/74HC32 is identical in pinout to the LS32. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 48 FETs or 12 Equivalent Gates

### MC54/74HC32



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

### ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM

### PIN ASSIGNMENT

FIIV	ASSI	SIMINIE	IVI
A1 [	1 •	14	] v <sub>CC</sub>
B1 [	2	13	] B4
Y1 [	3	12	] A4
A2 [	4	11	] Y4
B2 [	5	10	] B3
Y2 [	6	9	] A3
GND [	7	8	] Y3

### **FUNCTION TABLE**

1	Inp	uts	Output
1	Α	В	Υ
F	L	X.	L
1	L	Н	Н.
1	Н	L	H
	Н	H	H

Y = A + B

### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused

outputs must be left open.

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Para	ameter		Min	Max	Unit
Vcc	DC Supply Voltage (Refere	nced to GNE	))	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output V	/oltage (Refe	erenced to GND)	0	Vcc	V
TA	Operating Temperature, All	Operating Temperature, All Package Types			+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	BONGE	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V	0	1000 500	ns
	19 ===		V <sub>CC</sub> = 6.0 V	0	400	

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	agneticement of box adors lie at	Guaranteed Lin	nit				
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out}$ = 0.1 V or $V_{CC}$ - 0.1 V $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	VOH Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

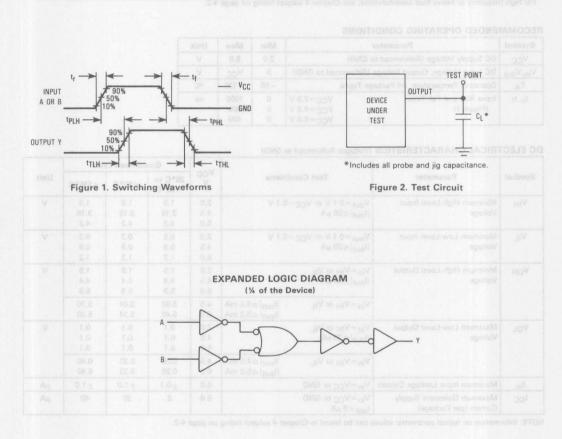
Functional operation should be restricted to the Recommended Operating Conditions.

<sup>†</sup>Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

	This device contains	Guaranteed Limit	imit	todinys					
Symbol	circuitry to guard against the minigh static voltages floats. However, arecauti	Parameter			VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay	, Input A or B t	o Output Y		2.0	100	125	150	ns
tPHL	(Figures 1 and 2)				4.5	20	25	30	
	voltages so this high-in				6.0	17	21	26	
tTLH,	Maximum Output Transition	Time, Any Outp	out	de la constitución de la constit	2.0	75	95	110	ns
tTHL	(Figures 1 and 2)				4.5	15	19	22	100
9943	too Vite nevite divid agreen				6.0	13	16	19	63
Cin	Maximum Input Capacitance		900	CONTRACTO	200	10	10	10	pF

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate) anothers of the second learning and t	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	Functional
	Used to determine the no-load dynamic power consumption: $P_D = C_{PD} \ V_{CC}^{2f} + I_{CC} \ V_{CC}$	mod 3° Was 0 20 SIG Simbo3	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	med 2°TVkm To Separatif 2'OB	



### MC54/74HC34

### Product Preview

# Hex Noninverting Buffer High-Performance Silicon-Gate CMOS

The MC54/74HC34 is identical in pinout to the HC04 and LS04, but the HC34 has noninverting outputs. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 48 FETs or 12 Equivalent Gates

# 14

J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



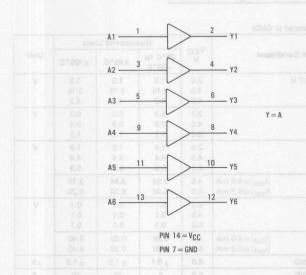
D SUFFIX SOIC CASE 751A

### ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM



### PIN ASSIGNMENT

	THE ADDIGITATION OF THE PROPERTY OF THE PROPER		
A1 [	1 •	14	vcc
Y1 [	2	13	] A6
A2 [	3	12	1 Y6
Y2 [	4	11	] A5
A3 [	5	10	1 Y5
Y3 [	6	9	] A4
GND [	7 000	8	] Y4

### FUNCTION TABLE

Input A	Output
L	L
Н	Н

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

#### MAYIMIIM BATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA -
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND  $\leq$  (Vin or Vout)  $\leq$  VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to G	ND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (F	eferenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V	0	1000 500	ns
		V <sub>CC</sub> = 6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	e she		W	Guaranteed Limit			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{\text{out}} = V_{\text{CC}} - 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{iH}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=V <sub>CC</sub> or GND	6.0	± 0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 µA	6.0	2	20	40	μΑ

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

#### AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

			Projected Limit			
Symbol	Parameter	Vcc	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input A to Output (Figures 1 and 2)	2.0 4.5 6.0	90 18 15	115 23 20	135 27 23	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	_	10	10	10	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	TBD TBD	pF

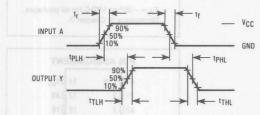
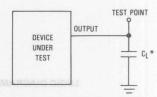


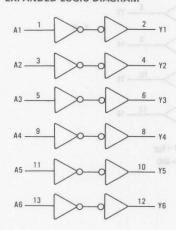
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

#### EXPANDED LOGIC DIAGRAM



## Hex Noninverting Buffer with LSTTL-Compatible Inputs

**High-Performance Silicon-Gate CMOS** 

The MC54/74HCT34 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT34 is identical in pinout to the LS04 and HCT04, but the HCT34 has non-inverting outputs.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 60 FETs or 15 Equivalent Gates



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



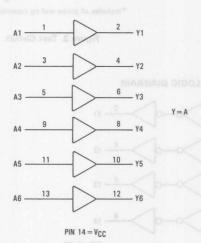
D SUFFIX SOIC CASE 751A

#### ORDERING INFORMATION

MC74HCTXXN MC54HCTXXJ MC74HCTXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



#### 

#### **FUNCTION TABLE**

Input A	Output
L	L
Н	Н

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

#### **MAXIMUM RATINGS\***

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND≤(Vin or Vout)≤VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	٧
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Figure 2. Test Circuit		Van	Guaranteed Limit			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
VIL	Maximum Low-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu\text{A}$	4.5 5.5	0.8	0.8 0.8	0.8 0.8	٧
VOH Minimum High-Le Voltage	Minimum High-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}}$ $ I_{\text{out}}  \le 20 \mu\text{A}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
	4 12	$V_{in} = V_{IH}$ $ I_{out}  \le 4.0 \text{ mA}$	4.5	3.98	3.84	3.70	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	٧
	CV andiana	$V_{in} = V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	5.5	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 µA	5.5	2	20	40	μΑ

ΔICC	Additional Quiescent Supply	Vin=2.4 V, Any One Input	1	≥ -55°C	25°C to 125°C	
	Current	V <sub>in</sub> =V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> =0 μA	5.5	2.9	2.4	mA

#### NOTES:

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5.0 V ±10%, C<sub>I</sub> =50 pF, Input t<sub>r</sub>=t<sub>f</sub>=6 ns)

	Value Unit This device contains		Projected Limit				
Symbol	Parameter of 3.0 (CMD)	25°C to -55°C	≤85°C	≤125°C	Unit		
tPLH, tPHL	Maximum Propagation Delay, Input (Figures 1 and 2)	A to Output Y	(GMD)	22	28	33	ns
tTLH, tTHL	Maximum Output Transition Time, A (Figures 1 and 2)	Any Output		15	19	22	ns
Cin	Maximum Input Capacitance	m 08±	2579	10	10	10	pF

#### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
   Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	TBD TO CATANANT TBD	pF

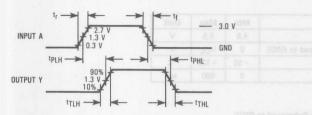
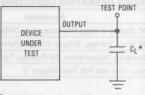


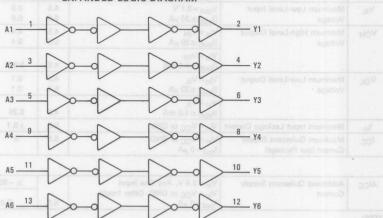
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

#### **EXPANDED LOGIC DIAGRAM**



## Product Preview

## **Hex Noninverting Buffer with Open-Drain Outputs**

## **High-Performance Silicon-Gate CMOS**

The MC54/74HC35 is identical in pinout to the LS05 and HC05, but the HC35 has noninverting outputs. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each of the HC35 outputs is fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable output pullup resistor, this gate can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

- Output Drive Capability: 10 LSTTL Loads with Suitable Pullup Resistor
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 48 FETs or 12 Equivalent Gates

## MC54/74HC35



CERAMIC **CASE 632** 



N SUFFIX PLASTIC **CASE 646** 



D SUFFIX SOIC CASE 751A

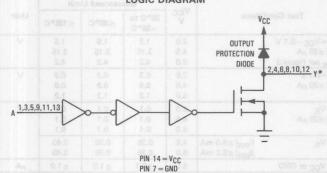
#### ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



\*Denotes open-drain outputs.



#### **FUNCTION TABLE**

Input A	Output
L	L
Н	Z

Z = high impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

I	
ŀ	0

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	٧
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±25	mA
Icc	DC Supply Current, VCC and GND Pins	±50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stq</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND≤(Vin or Vout)≤VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referen	ced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	LE A DEY		N	Gua	imit		
Symbol	Parameter	Test Conditions	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{\text{out}} = V_{\text{CC}} - 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu\text{A}$ $R_{\text{pu}}$ per Figure 2	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IL}$ $ I_{out}  \le 4.$ $ I_{out}  \le 5.$		0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	6.0	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	2	20	40	μΑ
loz	Maximum Output Leakage Current	A=V <sub>IH</sub> V <sub>out</sub> =V <sub>CC</sub> or GND	6.0	±0.5	±5.0	± 10.0	μΑ

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

#### AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

Symbol			Pr			
	Parameter	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
tPLZ,	Maximum Propagation Delay, Input A to Output Y	2.0	110	140	165	ns
tPZL	(Figures 1 and 2)	4.5	22	28	33	
	CONTRACT ANTICAL base	6.0	19	24	28	FI GIR
tTHL	Maximum Output Transition Time, Any Output	2.0	75	95	110	ns
	(Figures 1 and 2)	4.5	15	19	22	
		6.0	13	16	19	
Cin	Maximum Input Capacitance		10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	y unca te	10	10	10	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance	(Per Buffer) and a service as a service and a service as	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load PD = CPD VCC <sup>2</sup> f + ICC VCC	dynamic power consumption:	dall residence can be used so an LED	orie enel
		apter 4 subject listing on page 4-2.	Janua griena a	pr <sub>jet</sub>

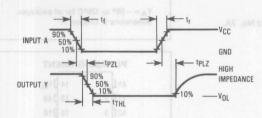
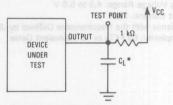
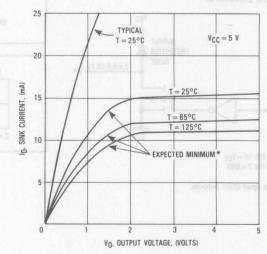


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit



\*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics

## Product Preview

# Hex Noninverting Buffer with Open-Drain Outputs and LSTTL-Compatible Inputs

**High-Performance Silicon-Gate CMOS** 

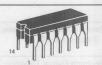
The MC54/74HCT35 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT35 is identical in pinout to the LS05 and HCT05, but the HCT35 has non-inverting outputs.

Each of the HCT35 outputs is fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable output pullup resistor, this gate can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

- Output Drive Capability: 10 LSTTL Loads with Suitable Pullup Resistor
- TTL/NMOS-Compatible Input Levels
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 60 FETs or 15 Equivalent Gates

## MC54/74HCT35



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646

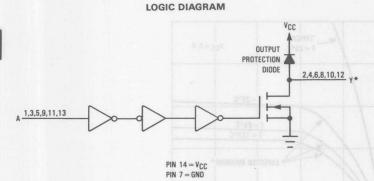


D SUFFIX SOIC CASE 751A

#### ORDERING INFORMATION

MC74HCTXXN MC54HCTXXJ MC74HCTXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.



\*Denotes open-drain outputs.

#### **FUNCTION TABLE**

Input A	Output Y
L	L
Н	Z

Z = high impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Symbol	Parameter	Value	Unit
VCC	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Huesi Direct S esupt		V/2000	Guaranteed Limit			
Symbol	Parameter	Test Conditions	Vcc	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =V <sub>CC</sub> -0.1 V  I <sub>out</sub>  ≤20 μA, R <sub>pu</sub> per Figure 2	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	٧
VIL	Maximum Low-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu \text{A}$	4.5 5.5	0.8	0.8 0.8	0.8 0.8	. V
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	٧
		$V_{in} = V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	5.5	±0.1	±1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 µA	5.5	2	20	40	μΑ
loz	Maximum Output Leakage Current	A=VIH Vout=VCC or GND	5.5	±0.5	±5.0	± 10.0	μΑ

ΔICC	Additional Quiescent Supply	V <sub>in</sub> =2.4 V, Any One Input		≥ -55°C	25°C to 125°C	
	Current	$V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0 \mu A$	5.5	2.9	2.4	mA

#### NOTES

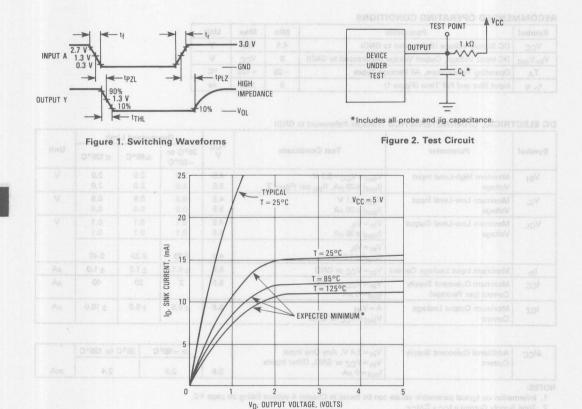
- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

				Pr	ojected Lir	nit	
Symbol	circulity vs. guard against due to high static voltages i fields. However, precaute	Parameter 1 01 0.0	1010	25°C to -55°C	≤85°C	≤125°C	Unit
tPLZ, tPZL	Maximum Propagation Delay, (Figures 1 and 2)	Input A to Output Y	(OND)	24	30	36	ns
<sup>t</sup> THL	Maximum Output Transition T (Figures 1 and 2)	ime, Any Output		15	19	22	ns
Cin	Maximum Input Capacitance	TALL AGE	T FBITT - Investor S As A	10	10	10	pF
Cout	Maximum Three-State Output	Capacitance (Output in High-Im	pedance State)	10	10	10	pF
TES:						el ensual	

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	Ametions
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	Center Car May Car mW/°C from 60° to 601C Package - 2 mW/°C from 60° to	pF



\*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics

## 1-of-10 Decoder High-Performance Silicon-Gate CMOS

The MC54/74HC42 is identical in pinout to the LS42. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTI outputs

The HC42 decodes a BCD Address to one-of-ten active-low outputs. For Address inputs with a hexadecimal equivalent greater than 9, all outputs, Y0-Y9, remain high (inactive)

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 104 FETs or 26 Equivalent Gates

## MC54/74HC42



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

Plastic

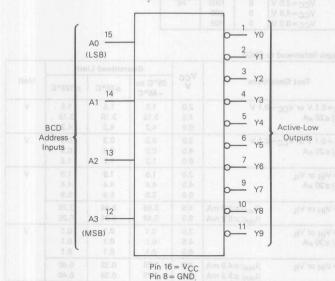
Ceramic SOIC

#### ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT

FIN	ASSI	GIAIAIEIAI
YOU	1 •	16 VC
TOATY1	2	15 A0
Y2	3	14 A1
Y30	4	13 A2
Y40	5	12 A3
Y5 C	6	11 Y9
Y6	7	10 Y8
GND	8	9 Y7

#### MAXIMUM BATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	٧
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{\text{in}}$  and  $V_{\text{out}}$  should be constrained to the range  $\text{GND} \leq |V_{\text{in}} \cap V_{\text{Out}}| \leq V_{\text{CC}}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to G	ND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (R	referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package	Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	AT EDEY		1 6	W	Gua	aranteed Li	imit	
Symbol	Parameter	Test Co	nditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub>  I <sub>out</sub>   ≤ 20 μA	-0.1 V	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub>  I <sub>out</sub>   ≤ 20 μA	-0.1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Vон	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	17 <u>a</u>	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		Vin=VIH or VIL	I <sub>out</sub>   ≤4.0 mA  I <sub>out</sub>   ≤5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	[ 4 - 4	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
		Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	8	80	160	μΑ

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

### MC54/74HC42

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

		.,	Gua	aranteed Li	mit	
Symbol	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, Input A to Output Y	2.0	150	190	225	ns
tPHL	(Figures 1 and 2)	4.5	30	38	45	
21 7112 E	beautiful top only dold man	6.0	26	33	38	
tTLH,	Maximum Output Transition Time, Any Output	2.0	75	95	110	ns
tTHL	(Figures 1 and 2)	4.5	15	19	22	
		6.0	13	16	19	
Cin	Maximum Input Capacitance	_	10	10	10	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCc <sup>2</sup> f + ICC VCC	65	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

FIGURE 1 - SWITCHING WAVEFORMS

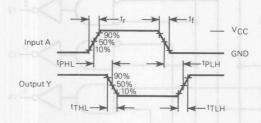
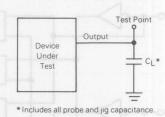


FIGURE 2 - TEST CIRCUIT



#### **FUNCTION TABLE**

	Inp	uts					(	Dut	outs				
АЗ	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9
L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	Н	L	Н	Н	Н	Н	Н	H	Н	H
L	L	H	L	Н	Н	L	H	H	Н	Н	Н	Н	Н
L	L	Н	Н	Н	Н	Н	L	H	H	H	Н	Н	Н
L	Н	L	L	Н	Н	Н	H	L	Н	Н	Н	Н	Н
L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	H	Н	Н
L	Н	Н	L	Н	Н	H	H	H	Н	L	H	Н	Н
L	Н	Н	Н	Н	Н	Н	Н	H	H	Н	L	Н	H
Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
Н	L	Н	L	Н	Н	Н	Н	Н	Н.	Н	Н	Н	Н
H	L	Н	Н	Н	H	Н	H	Н	Н	Н	H	Н	Н
Н	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
Н	Н	L	Н	Н	H	Н	H	H	Н	Н	Н	H	Н
H	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
Н	H	Н	Н	Н	Н	H	Н	Н	H	Н	Н	Н	Н

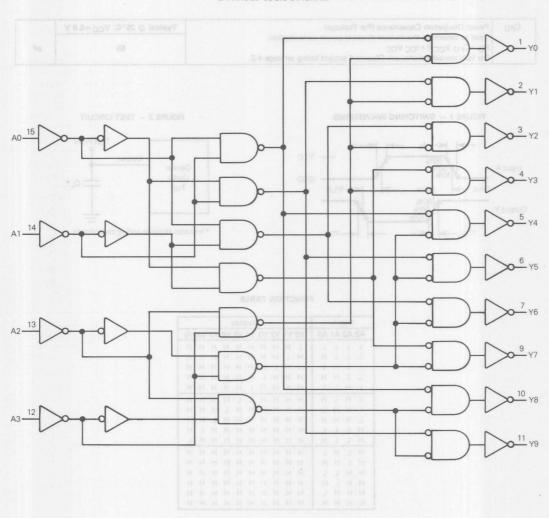
A0, A1, A2, A3, (PINS 15, 14, 13, 12) — BCD Address Inputs. The BCD address present at these inputs determines which output is active-low. These inputs are arranged such that A3 is the most-significant bit and A0 is the least-significant bit. Addresses with a hexadecimal equivalent

number greater than nine are not decoded.

#### OUTPUTS

Y0-Y9 (PINS 1-7, 9-11) — Active-Low Decoded Outputs. These outputs assume a low level when addressed and remain high when not addressed.

#### EXPANDED LOGIC DIAGRAM



## 2-Wide, 2-Input/2-Wide, 3-Input **AND-NOR Gates High-Performance Silicon-Gate CMOS**

The MC54/74HC51 is identical in pinout to the LS51. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 42 FETs or 10.5 Equivalent Gates

## MC54/74HC51



J SUFFIX CERAMIC **CASE 632** 



N SUFFIX PLASTIC **CASE 646** 



D SUFFIX SOIC CASE 751A

#### ORDERING INFORMATION

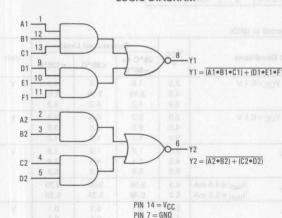
MC74HCXXN MC54HCXXJ

Ceramic

MC74HCXXD SOIC

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



PIN ASSIGNMENT

A1 [	1 •	14	1 v <sub>CC</sub>
A2 [	2	13	] C1
B2 [	3	12	] B1
C2 [	4	- 11	]F1
D2 [	5	10	] E1
Y2 [	6	9	01
GND [	7	8	] Y1

5

#### FUNCTION TABLES

		Output				
A1	B1	C1	D1	E1	F1	Y1
н	Н	Н	X	X	X	L
X	X	X	Н	Н	Н	L
All	oth	er co	ombi	natio	ons	Н

	Inp	uts		Output
A2	B2	C2	D2	Y2
Н	Н	X	X	L
X	X	Н	Н	DOL
All o	ther co	mbina	tions	Н

#### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
lcc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
VCC	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	CC = 2.0 V CC = 4.5 V CC = 6.0 V	0 0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Gua	imit		
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Uni
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	SE V
Vон	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V 23
	AT BY CT OF ET PS	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	10
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	etugal	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	± 1.0	± 1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 µA	6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

#### AC ELECTRICAL CHARACTERISTICS (C1 = 50 pF, Input tr = tf = 6 ns)

			Gua				
Symbol	Parameter Parameter Company Co	VCC	25°C to -55°C	≤85°C	≤125°C	Unit	
tPLH, tPHL	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns	
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns ABOM	
Cin	Maximum Input Capacitance	ducture.	10	10	10	pF	

#### NOTES:

- 1. For propagation delays witj loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Section)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	illamo!
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	call in lowlyn3 3.01 v <sub>23</sub> 39 SA syrivale	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

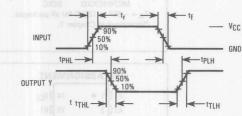
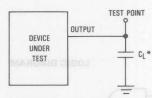


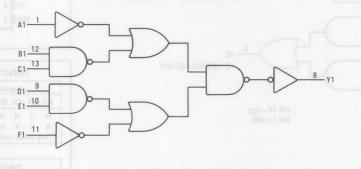
Figure 1. Switching Waveforms

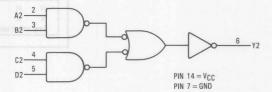


\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

#### **EXPANDED LOGIC DIAGRAM**

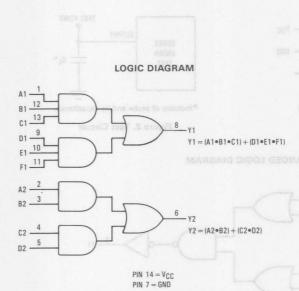




## **High-Performance Silicon-Gate CMOS**

The MC54/74HC58 is identical to the MC54/74HC51 except that the outputs are inverted. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 42 FETs or 10.5 Equivalent Gates





J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

#### ORDERING INFORMATION

MC74HCXXN Plastic
MC54HCXXJ Ceramic
MC74HCXXD SOIC

T<sub>A</sub> = -55° to 125°C for all packages.
Dimensions in Chapter 7.

## PIN ASSIGNMENT

1000	A1 0 1 • 14 V <sub>CC</sub> A2 0 2 13 C1 B2 0 3 12 B1 C2 0 4 11 F1		
A1 [	1 •	14	vcc
A2 [	2	13	] C1
B2 [	3	12	] B1
C2 [	4	11	] F1
D2 [	5	10	] E1
Y2 [	6	9	01
GND [	7	8	1 Y 1
1			1

#### **FUNCTION TABLES**

		Output				
A1	B1	C1	D1	E1	F1	Y1
Н	Н	Н	X	X	X	Н
X	X	X	Н	Н	Н	Н
An	y ot	her o	comb	oinat	ion	L

	Inp	uts		Output
A2	B2	C2	D2	Y2
н	Н	X	X	Н
X	X	Н	Н	Н
Any	other o	combin	ation	L

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	٧
Vout	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	od occ

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\text{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{\text{CC}}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{\text{CC}}$ ). Unused outputs must be left open.

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> = 2.0 V	0	1000	ns
	(Figure 1)	$V_{CC} = 4.5 V$	0	500	
	notudies all probe and jid capacitance.	V <sub>CC</sub> = 6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Gua			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH Minimum High-Level Outp Voltage	Minimum High-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=Vcc or GND	6.0	± 0.1	± 1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 µA	6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

<sup>†</sup>Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	This dayles contains			Gua	imit	Symbol	
Symbol	due to high static voltages	Parameter Parame	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Dela (Figures 1 and 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns	
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 2)			75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitano	ce ANA	_SUE Protes	10	10	10	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Section)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	seitmu-
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	mon 0° Won 01 900 scent -	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	Color Designation of the state of the	

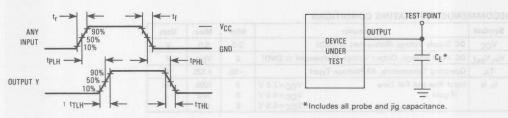
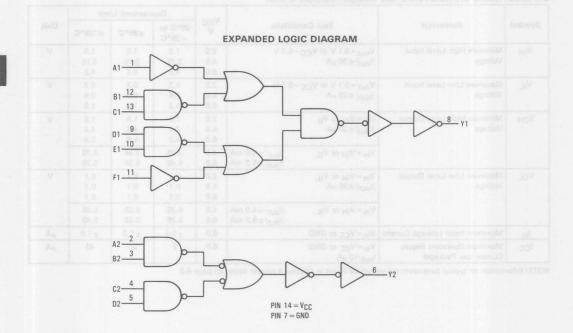


Figure 1. Switching Waveforms

Figure 2. Test Circuit

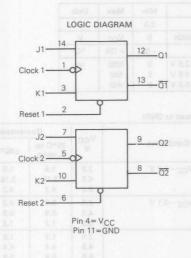


## Dual J-K Flip-Flop with Reset High-Performance Silicon-Gate CMOS

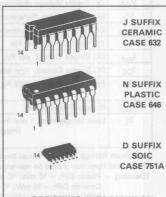
The MC54/74HC73 is identical in pinout to the LS73. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has an active-low asynchronous reset. The MC54/74HC73 is identical in function to the HC107, but has a different pinout.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 92 FETs or 23 Equivalent Gates



## MC54/74HC73



#### **ORDERING INFORMATION**

MC74HCXXN Plastic MC54HCXXJ Ceramic MC74HCXXD SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### 

FUNCTION TABLE

	Inpu	Out	puts		
Reset	Clock	J	K	Q	ā
L	X	X	X	L	Н
Н	~	L	L	No Change	
Н	7	L	Н	LU	Н
Н	7	H	L	Н	L
Н	~	H	Н	Toggle	
Н	L	X	X	No Change	
Н	Н	X	X	No Change	
Н	5	X	X	No C	hange

HØ.	
•	

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq \mathsf{VCC}$ . Unused inputs must always be tied to an appropriate logic voltage level

(e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
VCC	DC Supply Voltage (Referenced to G	2.0	6.0	V	
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (R	0	Vcc	V	
TA	Operating Temperature, All Package	Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				V	Guaranteed Limit			
Symbol	Parameter 18 18 18 18 18 18 18 18 18 18 18 18 18	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIA	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
No Cha	X X X I	Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
No Cha	X X H H H	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	± 0.1	± 1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA		6.0	4	40	80	μΑ

			Vcc	Gua			
Symbol Para	Parameter	imeter		25°C to -55°C	≤85°C	≤125°C	Unit
fmax	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	534	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to $Q$ or $\overline{Q}$ (Figures 1 and 4)	GND	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tPLH, tPHL	Maximum Propagation Delay, Reset to Q or $\overline{\mathbf{Q}}$ (Figures 2 and 4)		2.0 4.5 6.0	155 31 26	195 39 33	235 47 40	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)		2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance		-	10	10	10	pF

#### NOTES

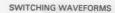
1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

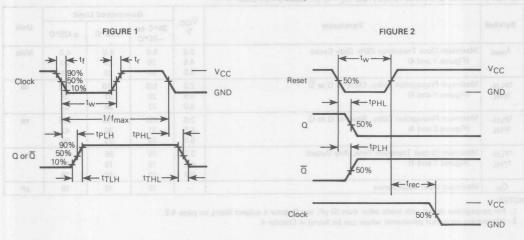
2. Information on typical parametric values can be found in Chapter 4.

Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
Used to determine the no-load dynamic power consumption:	5 5 5 1 1 mg	
	35	pF
		Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC  35

#### TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

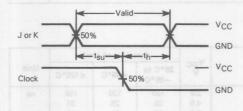
	* p == 1		W	Guaranteed Limit			1
Symbol	Parameter	30V	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, J or K to Clock (Figure 3)	ONO	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Clock to J or K (Figure 3)		2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
trec	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	Jaunner 	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)		2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
tw	Minimum Pulse Width, Reset (Figure 2)		2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	-80	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

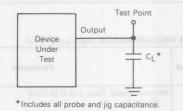




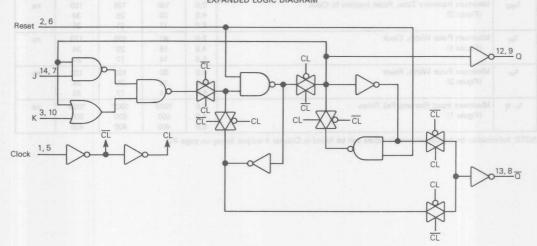
### FIGURE 3

FIGURE 4 - TEST CIRCUIT





### EXPANDED LOGIC DIAGRAM



## Dual D Flip-Flop with Set and Reset

## **High-Performance Silicon-Gate CMOS**

The MC54/74HC74 is identical in pinout to the LS74. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two D flip-flops with individual Set, Reset, and Clock inputs. Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and  $\overline{Q}$  outputs are available from each flip-flop. The Set and Reset inputs are asynchronous.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 128 FETs or 32 Equivalent Gates

## MC54/74HC74



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



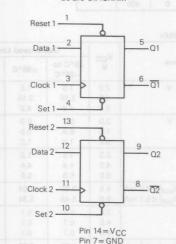
D SUFFIX SOIC CASE 751A

#### ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT

Reset 1	10:	14	VCC
Data 1	2	13	Reset 2
Clock 1	3	12	Data 2
Set 1	4	11	Clock 2
Q1 <b>E</b>	5	10	Set 2
01 0	6	9	Q2
GND	7	8	<u>Q2</u>

#### FUNCTION TABLE

	Inp	Out	puts			
Set	Reset	Clock	Data	Q	Q	
L	Н	X	X	H	L	
Н	L	X	X	L	Н	
L	L	X	X	H*	H*	
Н	Н.		Н	Н	L	
Н	Η.	_	L	L	Н	
H	Н	L	X	No Change		
H	Н	Н	X	No Change		
H	H	1	X	No Change		

\*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

ľ	10.0		4	
		ľ	4	

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† 750 SOIC Package† 500		mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Parameter Test Conditions		W	Guaranteed Limit			
Symbol			VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤ 20 μA		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{Out}}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
Outpu	Inputs Set Reset Goot Date	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	1 - 1 1	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 µA	6.0	4	40	80	μΑ

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

#### AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

		Vcc	Gua			
Symbol	Parameter		25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to $Q$ or $\overline{Q}$ (Figures 1 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLH, tPHL	Maximum Propagation Delay, Set or Reset to Q or Q (Figures 2 and 4)		230 46 39	290 58 49	345 69 59	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns D 10
Cin	Maximum Input Capacitance		10	10	10	pF

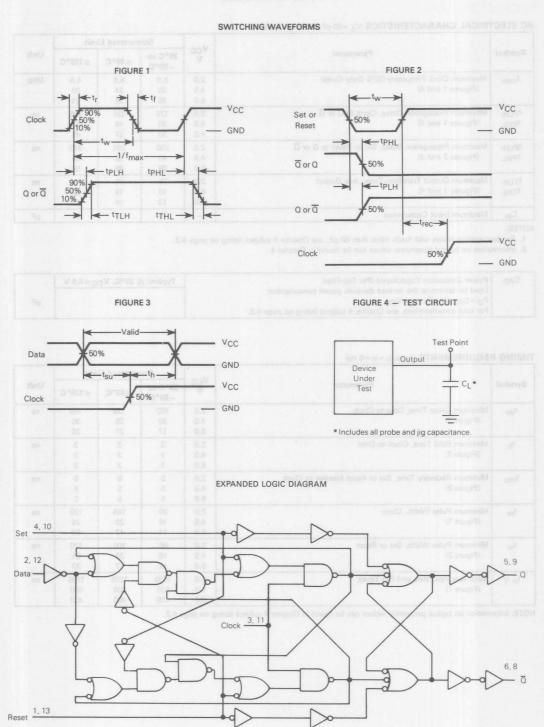
#### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
   Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC STANCE  For load considerations, see Chapter 4 subject listing on page 4-2.	£ 3/RJ 39	pF

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	Parameter	Van	Guaranteed Limit			
Symbol		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Data to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Clock to Data (Figure 3)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
trec	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t <sub>W</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
tw	Minimum Pulse Width, Set or Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns



## **Dual 2-Bit Transparent Latch High-Performance Silicon-Gate CMOS**

The MC54/74HC75 is identical in pinout to the LS75. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 2-bit transparent latches. Each latch stores the input data while Latch Enable is at a logic low. The outputs follow the data inputs when Latch Enable is at a logic high.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 80 FETs or 20 Equivalent Gates

## MC54/74HC75



J SUFFIX CERAMIC **CASE 620** 



N SUFFIX PLASTIC **CASE 648** 



D SUFFIX SOIC **CASE 751** 

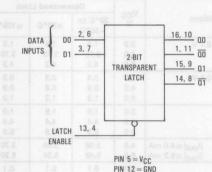
#### ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD

Plastic Ceramic SOIC

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



PIN	ASSI	GNMI	ENT
00 <sub>a</sub> [	1 •	16	] 00a
DO <sub>a</sub> [	2	15	101a
D1 <sub>a</sub> [	3	14	] 01 <sub>a</sub>
LE <sub>b</sub> [	4	13	] LE <sub>a</sub>
V <sub>CC</sub> [	5	12	GND
DOb	6	11	] 00 <sub>b</sub>
D1 <sub>b</sub> [	7	10	ao <sub>b</sub>
01 <sub>b</sub> [	8	9	] a1 <sub>b</sub>

#### **FUNCTION TABLE**

- 1	nputs	Out	puts
D	Latch Enable	Q	ā
L	Н	L	Н
Н	Н	Н	L
X	L	QO	Q0

X = don't care Q0 = latched data

5	

		value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	٧
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL NUS G	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND≤(Vin or Vout)≤VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	ed to GND)	0	Vcc	٧
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Parameter Test Conditions			V	Gua	ranteed Li	mit	
Symbol			VCC	25°C to -55°C	≤85°C	≤125°C	Uni	
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Vон	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	o ristal o	Vin=VIH or VIL	I <sub>out</sub>   ≤4.0 mA  I <sub>out</sub>   ≤5.2 mA	4.5	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	-04	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
0.5	X = don't care	Vin=VIH or VIL	I <sub>out</sub>   ≤4.0 mA  I <sub>out</sub>   ≤5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	4	40	80	μΑ

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

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	Parameter	.,	Gua			
Symbol		Vcc	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, D to Q (Figures 1 and 5)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tPLH, tPHL	Maximum Propagation Delay, D to $\overline{\mathbb{Q}}$ (Figures 1 and 5)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
tPLH, tPHL	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	ns
tPLH, tPHL	Maximum Propagation Delay, Latch Enable to $\overline{\mathbf{Q}}$ (Figures 2 and 5)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 3 and 5)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	- 1	10	10	10	pF

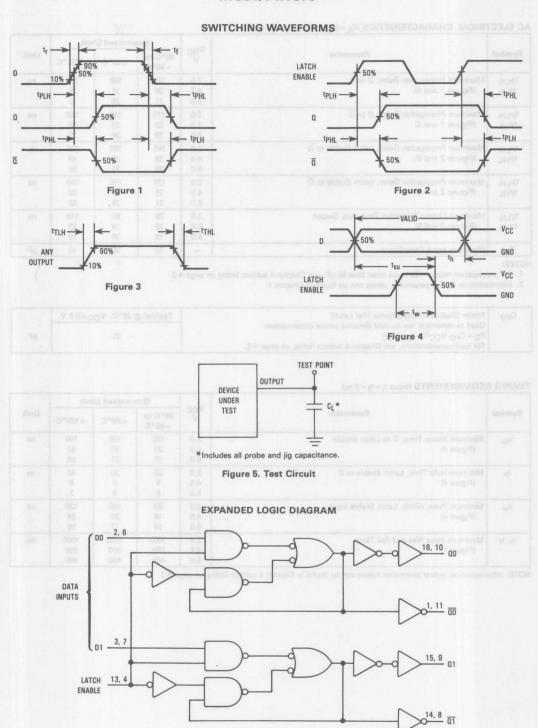
#### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
   Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Latch)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:		
	PD = CPD VCC2f + ICC VCC	35	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

#### TIMING REQUIREMENTS (Input to

	Parameter	Vcc V	Gua	imit		
Symbol			25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, D to Latch Enable (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Latch Enable to D (Figure 4)	2.0 4.5 6.0	25 5 5	30 6 6	40 8 7	ns
tw	Minimum Pulse Width, Latch Enable Input (Figure 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns



## **Dual J-K Flip-Flop with Set** and Reset

## **High-Performance Silicon-Gate CMOS**

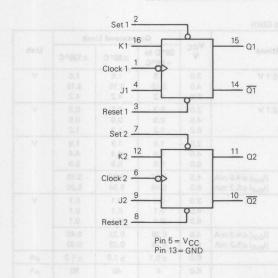
The MC54/74HC76 is identical in pinout to the LS76. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has active-low asynchronous Set and Reset inputs.

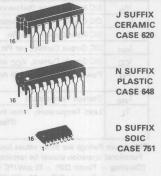
The HC76 is identical in function to the HC112, but has a different pinout.

- Similar in Function to the LS76 Except When Set and Reset are Low Simultaneously
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 100 FETs or 25 Equivalent Gates

#### LOGIC DIAGRAM



## MC54/74HC76



#### ORDERING INFORMATION

MC74HCXXN Plastic MC54HCXXJ Ceramic MC74HCXXD SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT

Clock 1	10	16 K1
Set 1	<b>C</b> 2	15 1 Q1
Reset 1	<b>L</b> 3	14 0 Q1
J1	4	13 GND
Vcc	<b>1</b> 5	12 K2
Clock 2	<b>C</b> 6	11 02
Set 2	7	10 02
Reset 2	8	9 J J2
	-	1

#### **FUNCTION TABLE**

	Inputs					puts
Set	Reset	Clock	J	K	Q	Q
L	Н	X	X	X	Н	L
H	a L	X	X	X	L	Н
L	L	X	X	X	L*	L*
Н	Н	~	L	L	No CI	hange
Н	Н	~	L	Н	L	Н
Н	Н	~	Н	L	Н	L
Н	Н	~	Н	Н	Tog	ggle
H	Н	Link	X	X	No CI	hange
H	H	Н	X	X	No CI	nange
H	Н	5	X	X	No CI	nange

\* Both outputs will remain low as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

#### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
alin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	d to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>		/ <sub>CC</sub> =2.0 V / <sub>CC</sub> =4.5 V	0	1000 500	ns
		/CC = 6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Parameter	Test Conditions		Guaranteed Limit			-
Symbol			VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out}$ =0.1 V or $V_{CC}$ -0.1 V $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
	8ut Recot Clock J E	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
DOOT I		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	6.0	± 0.1	± 1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	80	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

#### MC54/74HC76

#### AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	Parameter		Gua			
Symbol		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle)	2.0	6.0	4.8	4.0	MHz
	(Figures 1 and 4)	4.5	30	24	20	
	AND STREET, ST	6.0	35	28	24	
tPLH,	Maximum Propagation Delay, Clock to Q or Q	2.0	125	155	190	ns
tpHL (Figures 1 and 4)	(Figures 1 and 4)	4.5	25	31	38	
	[Hd]-[a] 46-	6.0	21	26	32	
tPLH,	Maximum Propagation Delay, Reset to Q or Q	2.0	155	195	235	ns
tPHL	(Figures 2 and 4)	4.5	31	39	47	
	and the same of th	6.0	26	33	40	
tPLH,	Maximum Propagation Delay, Set to Q or Q	2.0	165	205	250	ns
tPHL	(Figures 2 and 4)	4.5	33	41	50	
	1902 G 1000	6.0	28	35	43	
tTLH,	Maximum Output Transition Time, Any Output	2.0	75	95	110	ns
tTHL (Figures 1 and 4)	(Figures 1 and 4)	4.5	15	19	22	
DOY !	Antini regioni di seria di ser	6.0	13	16	19	
Cin	Maximum Input Capacitance	_	10	10	10	pF

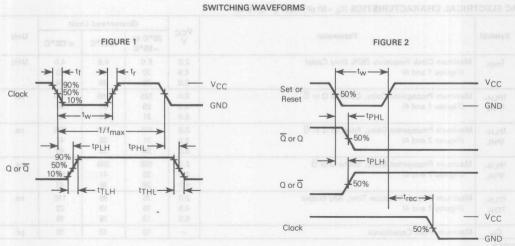
#### NOTES:

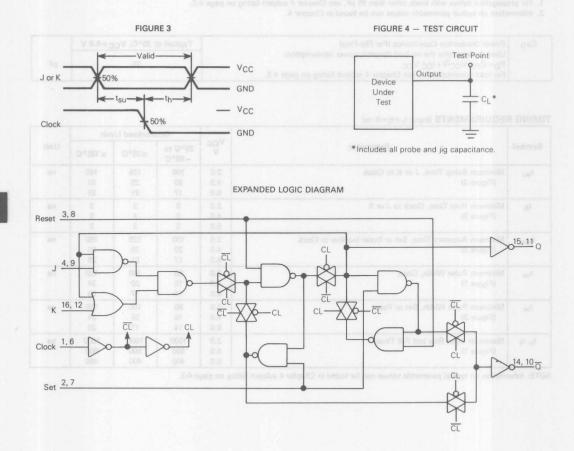
- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	page and the control of the control	
	PD = CPD VCC <sup>2</sup> f + ICC VCC	35	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	mental.	

### TIMING REQUIREMENTS (Input tr = tf = 6 ns)

	Account toward on the account to Parameter		Gua			
Symbol		V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, J or K to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Clock to J or K (Figure 3)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
trec	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>W</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>w</sub>	Minimum Pulse Width, Set or Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns





## 4-Bit Magnitude Comparator High-Performance Silicon-Gate CMOS

The MC54/74HC85 is identical in pinout and function to the LS85. This device is similar in function to the MM74C85 and L85, but has a different pinout. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This 4-Bit Magnitude Comparator compares two 4-bit nibbles and gives a high voltage level on either the A>B<sub>out</sub>, A=B<sub>out</sub>, or A<B<sub>out</sub> output, leaving the other two at a low voltage level. This device also has A>B<sub>in</sub>, A=B<sub>in</sub>, and A<B<sub>in</sub> inputs, eliminating the need for external gates when cascading.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 248 FETs or 62 Equivalent Gates

## MC54/74HC85



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

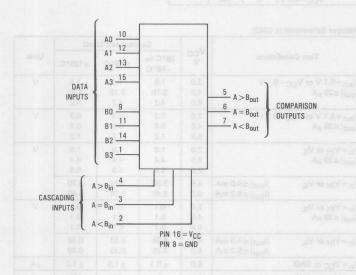
#### ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



## PIN ASSIGNMENT

PIN	ASSIG	IAIAIEI	41
В3 [	1 •	16	VCC
A < Bin [	2	15 ]	A3
A = B <sub>in</sub> [	3	14 ]	B2
$A > B_{in} \Gamma$	4	13 ]	A2
A > B <sub>out</sub> [	5	12	A1
$A = B_{out} \square$	6	11 ]	B1
$A < B_{out}$	7	10	A0
GND [	8	9 ]	ВО

r	
E	20
ē	
	-

Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds	>Bin, A=Bin, and	°C
	(Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	

due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND  $\leq$  (Vin or Vout)  $\leq$  VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter		Min	Max	Unit
VCC	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (	Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
tr, tf	Input Rise and Fall Time	V <sub>CC</sub> =2.0 V	0	1000	ns
(Figure 1)	(Figure 1)	V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	A Dall-4				Gua	aranteed L	imit	
Symbol	Symbol Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit	
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> − 0.  l <sub>out</sub>   ≤ 20 μA	1 V	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  l <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Vон	VOH Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	Vin=VIH or VIL	I <sub>out</sub>   ≤4.0 mA  I <sub>out</sub>   ≤5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20		
VOL	VOL Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		Vin=VIH or VIL	I <sub>out</sub>   ≤4.0 mA  I <sub>out</sub>   ≤5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	± 1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

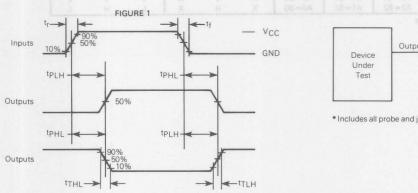
		VCC	Gua	aranteed Li	mit	Unit
Symbol	Parameter again united by the second of the		25°C to -55°C	≤85°C	≤125°C	
tPLH, tPHL	Maximum Propagation Delay, Inputs A or B to Outputs A > B or A < B (Figures 1 and 2)	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
tPLH, tPHL	Maximum Propagation Delay, Inputs A or B to Output A = B (Figures 1 and 2)	2.0 4.5 6.0	200 40 34	250 50 43	300 60 51	ns
tPLH, tPHL	Maximum Propagation Delay, Inputs A < B or A = B to Output A > B (Figures 1 and 2)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLH, tPHL	Maximum Propagation Delay, Inputs A > B or A = B to Output A < B (Figures 1 and 2)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLH, tPHL	Maximum Propagation Delay, Input A = B to Output A = B (Figures 1 and 2)	2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	-	10	10	10	pF

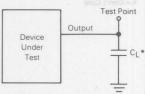
- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	A DOUGHOUSE SERVICE	
	PD = CPD Vcc <sup>2</sup> f+Icc Vcc For load considerations, see Chapter 4 subject listing on page 4-2.	\$8 >\$A 88 = EA	pF



#### FIGURE 2 - TEST CIRCUIT





\*Includes all probe and jig capacitance.

#### PIN DESCRIPTIONS

#### **INPUTS**

A0, A1, A2, A3 (Pins 10, 12, 13, 15) — Data Nibble A Inputs. The data nibble present at these inputs is compared to Data Nibble B. A3 is the most significant bit and A0 is the least significant bit.

B0, B1, B2, B3 (Pins 9, 11, 14, 1) — Data Nibble B Inputs. The data nibble present at these inputs is compared to Data Nibble A. B3 is the most significant bit and B0 is the least significant bit.

#### CONTROLS

 $A>B_{in}$ ,  $A=B_{in}$ ,  $A<B_{in}$  (Pins 4, 3, 2) — Cascading Inputs. These inputs determine the states of the outputs only when Data Nibble A equals Data Nibble B. The  $A=B_{in}$  input overrides both the  $A>B_{in}$  and  $A<B_{in}$  inputs.

For single stage operation or for the least significant stage in cascaded operation, the  $A\!<\!B_{in}$  and  $A\!>\!B_{in}$  inputs should be tied to ground and the  $A\!=\!B_{in}$  input tied to VCC. Between cascaded comparators, the  $A\!<\!B_{out},\,A\!=\!B_{out},\,$  and  $A\!>\!B_{out}$ 

outputs should be tied to  $A < B_{in}$ ,  $A = B_{in}$ , and  $A > B_{in}$ , respectively, of the succeeding stage.

#### **OUTPUTS**

 $A>B_{out}$  (Pin 5) — A-Greater-Than-B Output. This output is at a high voltage level when Nibble A is greater than Nibble B, regardless of the data present at the cascading inputs. This output is also high when Nibble A equals Nibble B and the  $A>B_{in}$  input is high ( $A<B_{in}$  and  $A=B_{in}$  are at a low voltage level)

 $\mathbf{A} = \mathbf{B_{out}}$  (Pin 6) — A-Equals-B Output. This output is high when Nibble A equals Nibble B and the  $\mathbf{A} = \mathbf{B_{in}}$  input is high.  $\mathbf{A} < \mathbf{B_{in}}$  and  $\mathbf{A} > \mathbf{B_{in}}$  have no effect when the comparator is in this condition and  $\mathbf{A} = \mathbf{B_{in}}$  is at a high voltage level.

 $A < B_{out}$  (Pin 7) — A-Less-Than-B Output. This output is at a high voltage level when Nibble A is less than Nibble B, regardless of data present at the cascading inputs. This output is also high when Nibble A equals Nibble B and the  $A < B_{in}$  input is high  $(A > B_{in}$  and  $A = B_{in}$  are at a low voltage level).

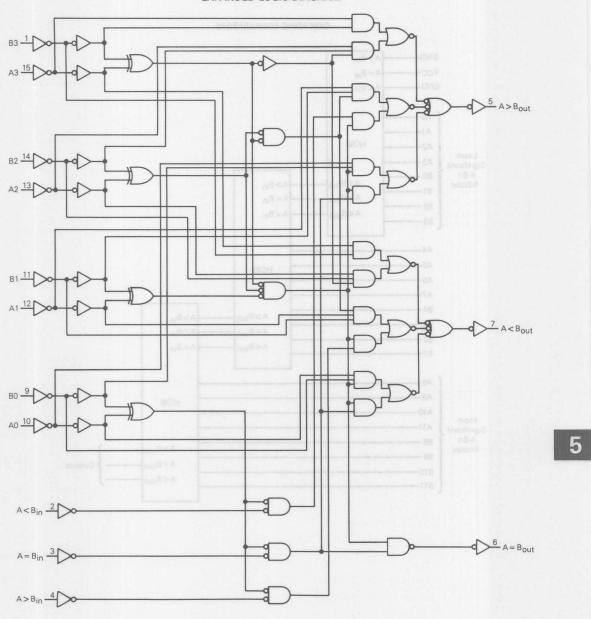
#### **FUNCTION TABLE**

	Data	Inputs		Cas	cading Inp	outs	BRIDLY DATE	Output	UNA 410 138
A3, B3	A2, B2	A1, B1	A0, B0	A>Bin	$A = B_{in}$	A <b<sub>in</b<sub>	A>B <sub>out</sub>	$A = B_{out}$	A < Bout
A3>B3	X	X	X	X	X	X	н	o akassi	and Lave
A3 < B3	X	X	×	X	X	X	teacLon e	de a Lemma	H
A3 = B3	A2>B2	X	×	X	X	X	H	Land	not-
A3 = B3	A2 < B2	×	X	X	X	X	L L	L	Н
A3 = B3	A2=B2	A1>B1	X	X	X	X	Н	L	L
A3 = B3	A2=B2	A1 < B1	X	X	X	X	L	L	Н
A3 = B3	A2=B2	A1 = B1	A0>B0	X	X	X	Н	L	L
A3 = B3	A2=B2	A1 = B1	A0 < B0	X	X	X	L	L	Н
A3 = B3	A2=B2	A1 = B1	A0 = B0	L	L	L	Н	L	Н
A3 = B3	A2=B2	A1 = B1	A0 = B0	L	L	Н	L	L	Н
A3 = B3	A2=B2	A1 = B1	A0 = B0	H	ENER	O TO LAW	Н	18 -L 13	S COL
A3 = B3	A2=B2	A1 = B1	A0 = B0	Н	L	H	L	L	L
A3 = B3	A2=B2	A1 = B1	A0 = B0	×	Н	X	L	Н .	L

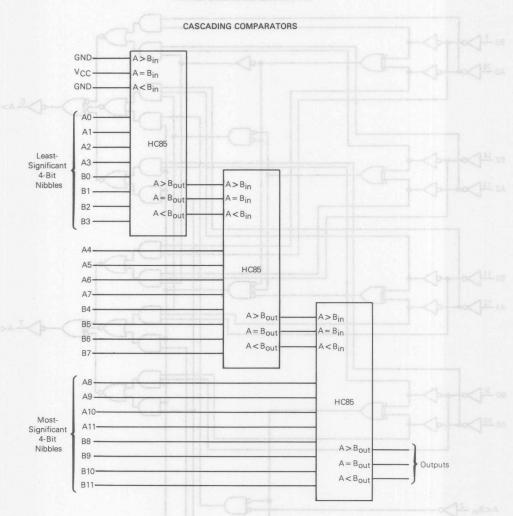
X = Don't Care

### MC54/74HC85

#### EXPANDED LOGIC DIAGRAM



TYPICAL APPLICATION



## MC54/74HC86

## **Quad 2-Input Exclusive OR Gate High-Performance Silicon-Gate CMOS**

The MC54/74HC86 is identical in pinout to the LS86; this device is similar in function to the MM74C86 and L86, but has a different pinout. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 56 FETs or 14 Equivalent Gates

J SUFFIX CERAMIC **CASE 632** 



N SUFFIX PLASTIC **CASE 646** 



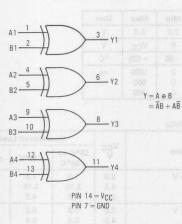
D SUFFIX SOIC CASE 751A

#### ORDERING INFORMATION

MC74HCXXN MC54HCXXJ MC74HCXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



## PIN ASSIGNMENT

A1 [	1 •	14	VCC
B1 [	2	13	] B4
Y1 [	3	12	] A4
A2 [	4	11	] Y4
B2 [	5	10	<b>B</b> 3
Y2 [	6	9	] A3
GND [	7	8	] Y3

### **FUNCTION TABLE**

Inp	uts	Output
А	В	Υ
L	L	L
L	Н	Н
H	L	Н
Н	Н	L

#### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
VCC	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	٧
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq \mathsf{VCC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referen	ced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V	0	1000 500	ns
		V <sub>CC</sub> = 6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				.,	Guaranteed Limit			
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub>  I <sub>out</sub>   ≤ 20 μA	-0.1 V	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub>  I <sub>out</sub>   ≤ 20 μA	-0.1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	* A	Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	± 0.1	± 1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA		6.0	2	20	40	μА

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

<sup>†</sup>Derating - Plastic DIP:  $-10 \text{ mW/}^{\circ}\text{C}$  from 65° to 125°C

#### AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

Symbol			Gua			
	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	asit for LEGH	10	10	10	pF

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	1150 m stemped 15 to 33 14 50 white-on	pF

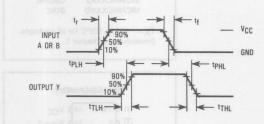
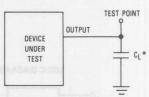


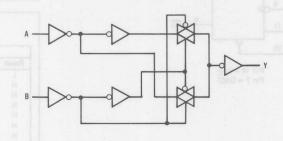
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

## EXPANDED LOGIC DIAGRAM (¼ of Device)

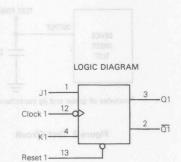


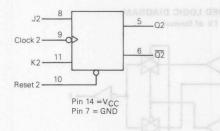
## Dual J-K Flip-Flop with Reset High-Performance Silicon-Gate CMOS

The MC54/74HC107 is identical in pinout to the LS107. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has an active-low asynchronous reset. The HC107 is identical in function to the HC73, but has a different pinout.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 92 FETs or 23 Equivalent Gates





## MC54/74HC107



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT

J1 I	10	14 VCC	
Q1	2	13 Reset 1	
Q1 I	3	12 Clock 1	
K1	4	11 K2	
Q2 I	5	10 Reset 2	
Q2 I	6	9 Clock 2	
GND I	7	8 <b>j</b> J2	

#### **FUNCTION TABLE**

	Inpu	Out	puts			
Reset	Clock	J	K	Q	ā	
L	X	X	X	L	Н	
Н	~	L L	No C	hange		
Н	~	L	Н	L	Н	
Н	~	Н	L	Н	L	
Н	~	Н	Н	Tog	ggle	
Н	L	X	X	No C	hange	
Н	Н	X	X	No C	hange	
Н	5	X	X	No Change		

IAXIIVIU	IVI KATINGS*	in the street to both of the	08 = 50 R
Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to ₹7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
lcc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	O ynA al

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND  $\leq$  (Vin or Vout)  $\leq$  VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GNE	))	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Refe	erenced to GND)	0	Vcc	٧
TA	Operating Temperature, All Package Ty	Operating Temperature, All Package Types		+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	17 21 28	0.8		Guaranteed Limit			
Symbol	Parameter	0.9 Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} = 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	1009 1000 1000	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	13 152
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V nobst (31)
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	6.0	±0.1	±1.0	± 1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	80	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

			Gu	10000		
Symbol	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to Q or $\overline{\mathbb{Q}}$ (Figures 1 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tPLH, tPHL	Maximum Propagation Delay, Reset to Q or $\overline{\mathbb{Q}}$ (Figures 2 and 4)	2.0 4.5 6.0	155 31 26	195 39 33	235 47 40	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance		10	10	10	pF

#### NOTES

- IOTES:

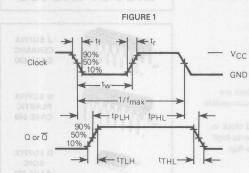
  1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	MINIOS
	Used to determine the no-load dynamic power consumption:  PD = CPD VCc <sup>2</sup> f + ICC VCC	netronizad 35	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	DC Bugsty Voltage (Antended to SHD)	Yec

#### TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

			Guaranteed Limit			-
Symbol	Parameter DA 0 V 0 B-00V	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, J or K to Clock (Figure 3)  HIME of becomes the	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Clock to J or K (Figure 3)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
trec	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>W</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>W</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.



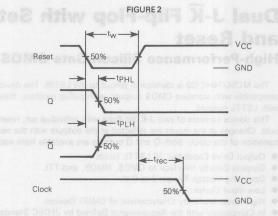


FIGURE 3

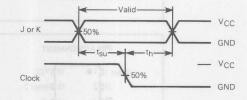
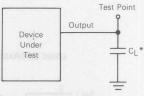
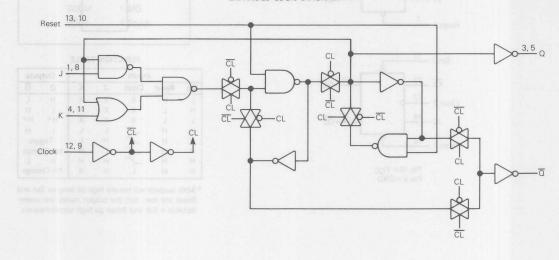


FIGURE 4 - TEST CIRCUIT



\*Includes all probe and jig capacitance.

EXPANDED LOGIC DIAGRAM



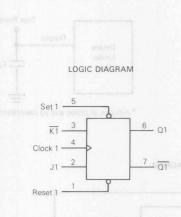
## Dual J-K Flip-Flop with Set and Reset

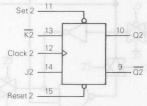
## **High-Performance Silicon-Gate CMOS**

The MC54/74HC109 is identical in pinout to the LS109. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two J- $\overline{K}$  flip-flops with individual set, reset, and clock inputs. Changes at the inputs are reflected at the outputs with the next low-to-high transition of the clock. Both Q and  $\overline{Q}$  outputs are available from each flip-flop.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 148 FETs or 37 Equivalent Gates





Pin 16 = V<sub>CC</sub> Pin 8 = GND

## MC54/74HC109



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT

Reset 1	1.	16 VCC
J10	2	15 Reset 2
K10	3	14 <b>1</b> J2
Clock 1	4	13 1K2
Set 1	5	12 Clock 2
010	6	11 Set 2
010	7	10 02
GND	8	9 1 02

#### **FUNCTION TABLE**

		Inputs			Out	puts
Set	Reset	Clock	J	K	Q	ā
L	Н	X	X	X	Н	L
Н	L	X	X	×.	L	Н
L	L	X	X	X	H*	H*
Н	Н	5	L	L	L	Н
H	H	5	Н	L	Tog	gle
H	Н	5	ol	Н	No Ch	
Н	H	_	H	Н	Н	L
H	Н	L	X	X	No Ch	ange

\*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

IAXIIVIO	IN HATHINGS.		1547 Book
Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	um Veq
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
2023	SOIC Packaget	500	Sat or Ra
T <sub>stg</sub>	Storage Temperature	-65  to  +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds		°C
\$n	(Plastic DIP or SOIC Package)	260 300	ynA ;emil

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referen	ced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	17 21 28	0.8		Gua			
Symbol	Parameter	7.5 Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $  l_{out}   \le 20 \mu \text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
	0001 0001 0001	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V Hal 13 TO
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	± 0.1	±1.0	± 1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	80	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

#### AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	This device contains				Gua	mit	Unit	
Symbol	display to grand against an against a said	Parameter 0.5 + 0.5 0.5		VCC	25°C to -55°C	≤85°C		≤125°C
f <sub>max</sub>	Maximum Clock Frequency (Figures 1 and 4)	(50% Duty Cycle)	-	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Dela (Figures 1 and 4)	ay, Clock to Q or Q	remis DIPF	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLH, tPHL	Maximum Propagation Dela (Figures 2 and 4)	ey, Set or Reset to Q or Q	Pedaget	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
tTLH, tTHL	Maximum Output Transition (Figures 1 and 4)	n Time, Any Output	C Packaget samic DIPI	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitano	e Continons Continons	regt) bibasawa	positi orb	10	10	10	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
  2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	COM
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC	40	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	DC Simply Voltage (Referenced en	any.

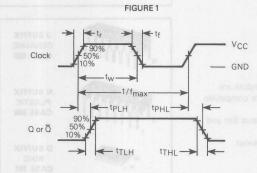
#### TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

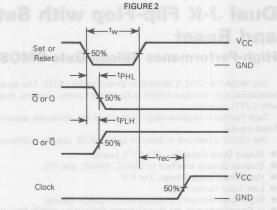
	N=33A N=32A	W	Gua	ranteed Li	mit	
Parameter 000 V 03 - 50V		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
id to GND).	consist e	2.0 4.5	100 20	125 25	150 30	ns
		6.0	17	21	26	
encirions	O ren7	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
ive to Clock	Au, 02	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
	Au 05	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
	Audi	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
n S. Bir (tup)	The second	2.0 4.5	1000 500	1000 500	1000 500	ns
	18 5 (No.)	1001 28 E o	2.0	2.0 1000 4.5 500	2.0 1000 1000 4.5 500 500	2.0 1000 1000 1000 4.5 500 500 500

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

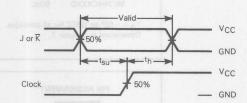
#### MC54/74HC109

#### SWITCHING WAVEFORMS

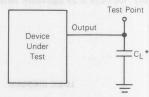




### FIGURE 3

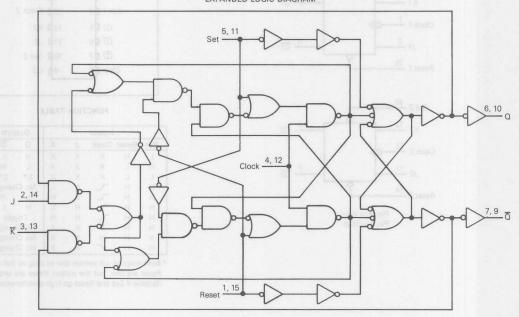


#### FIGURE 4 - TEST CIRCUIT



\*Includes all probe and jig capacitance.

#### EXPANDED LOGIC DIAGRAM



MOTOROLA HIGH-SPEED CMOS LOGIC DATA

## Dual J-K Flip-Flop with Set and Reset

## **High-Performance Silicon-Gate CMOS**

The MC54/74HC112 is identical in pinout to the LS112. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has active-low asynchronous Set and Reset inputs.

The HC112 is identical in function to the HC76, but has a different pinout.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Similar in Function to the LS112 Except When Set and Reset are Low Simultaneously
- Chip Complexity: 100 FETs or 25 Equivalent Gates

## MC54/74HC112

16

J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



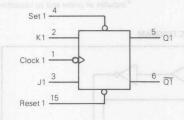
D SUFFIX SOIC CASE 751

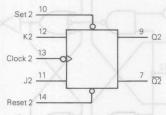
#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM





Pin 16 = VCC Pin 8 = GND

#### PIN ASSIGNMENT

Clock 1 l	10	16	VCC
K1 I	2	15	Reset
J1 I	3	140	Reset 2
Set 1	4	13	Clock 2
Q1 !	5	12	K2
Q1 I	6	110	J2
Q2 1	7	10	Set 2
GND I	8	91	Q2

#### FUNCTION TABLE

1	-	Inputs			Out	puts
Set	Reset	Clock	J	K	Q	Q
11/	Н	X	X	X	Н	L
Н	L	X	X	X	L	Н
L	L	X	X	X	L*	L*
H	Н	~	L	L	No CI	nange
H	Н	7	L	Н	T.C.	H
Н	Н	7	H	L	Н	L
Н	Н	~	Н	Н	Tog	ggle
Н	H		X	X	No CI	
Н	Н	Н	X	X	No CI	nange
Н	H	5	X	X	No CI	nange

\* Both outputs will remain low as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

#### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	$-1.5$ to $V_{CC} + 1.5$	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced	to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	CC = 2.0 V CC = 4.5 V CC = 6.0 V	0 0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	0.98-		Voo	Guaranteed Limit			
Symbol Parameter 00	Parameter 000		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V or } V_{\text{CC}} = 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
	14 17 20 80 100 129	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	800 800 500 400 400 400	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 µA	6.0	4	40	80	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

	anishop speed and substitution and and substitutio		V <sub>CC</sub>	Guaranteed Limit			tedmys
Symbol				25°C to -55°C	≤85°C	≤125°C	Unit
fmax	Maximum Clock Frequency (50% Duty Cycle)		2.0	6.0	4.8	4.0	MHz
	(Figures 1 and 4)		4.5 6.0	30 35	24	20 24	
tPLH, tPHL	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	1910 66	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tPLH,	Maximum Propagation Delay, Reset to Q or Q (Figures 2 and 4)	Tagasca	2.0 4.5	155 31	195 39	235 47	ns
tPLH,	Maximum Propagation Delay, Set to Q or Q (Figures 2 and 4)	abnoca togović (SIG pire	2.0 4.5	26 165 33	205 41	250 50	ns
tTLH,	Maximum Output Transition Time, Any Output (Figures 1 and 4)	edit of ac O betree	6.0 2.0 4.5 6.0	28 75 15 13	35 95 19	43 110 22 19	ns
Cin	Maximum Input Capacitance	- 50	-	10	10	10	pF

#### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

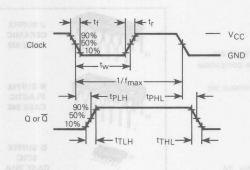
CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	201
	Used to determine the no-load dynamic power consumption:	DC Input Viringe Durgen Settings Referen	no Venil
	PD = CPD VCC2f + ICC VCC	35	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	STORY CONTRACTOR OF THE PROPERTY OF THE STORY OF THE STOR	

#### TIMING REQUIREMENTS (Input tr = tf = 6 ns)

	Parameter IONS at block after	V	Guaranteed Limit			
Symbol		VCC	25°C to -55°C	≤85°C	≤125°C	Uni
t <sub>su</sub>	Minimum Setup Time, J or K to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Clock to J or K (Figure 3)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
<sup>t</sup> rec	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>W</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>W</sub>	Minimum Pulse Width, Set or Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

FIGURE 2



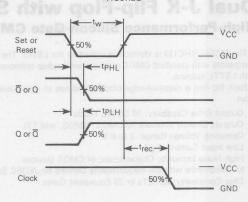


FIGURE 3

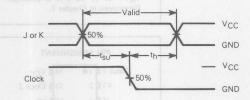
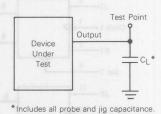
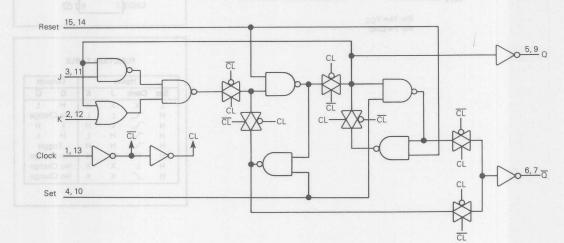


FIGURE 4 - TEST CIRCUIT



EXPANDED LOGIC DIAGRAM



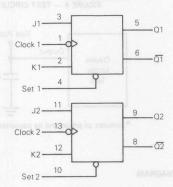
## **Dual J-K Flip-Flop with Set** High-Performance Silicon-Gate CMOS

The MC54/74HC113 is identical in pinout to the LS113. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has an active-low asynchronous set input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 92 FETs or 23 Equivalent Gates

#### LOGIC DIAGRAM



Pin 14 = V<sub>CC</sub> Pin 7 = GND

### MC54/74HC113



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT

Clock 1	10	140	VCC
K1 C	2	13	Clock 2
J1 <b>C</b>	3	12	K2
Set 1	4	11	J2
Q1 <b>C</b>	5	10	Set 2
010	6	90	Q2
GND	7	80	<u>02</u>

#### FUNCTION TABLE

puts	Out	Inputs				
Q	Q	K	J	Clock	Set	
L	Н	X	X	X	L	
hange	No C	LS	L	7	Н	
Н	L	Н	L	~	Н	
L	Н	L	Н	7	Н	
ggle	Tog	Н	Н	~	H	
hange	No Change		X	H	H	
hange	No C	X	X	L	H	
hange	No C	X	X	5	Н	

#### MC54/74HC113

#### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	2-h an	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)			Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	/ <sub>CC</sub> =2.0 V / <sub>CC</sub> =4.5 V	0	1000 500	ns
	es 3 lat 1 lat 1	/CC = 6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	17 21 29	Test Conditions		Guaranteed Limit			
Symbol	Parameter		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V	2.0	1.5	1.5	1.5	V
	Voltage	I <sub>out</sub>   ≤20 μA	4.5 6.0	3.15 4.2	3.15 4.2	3.15 4.2	2817
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	Minimum High-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	1000 1000 1000	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	1515
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V SAM 13
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	4	40	80	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

#### AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

	Value this this this contains		Guaranteed Limit			lodeny?
Symbol	Parameter ATS of S.B.	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
fmax	Maximum Clock Frequency (50% Duty Cycle)	2.0	6.0	4.8	4.0	MHz
	(Figures 1 and 4)	4.5 6.0	30 35	24 28	20 24	
tPLH, tPHL	Maximum Propagation Delay, Clock to Q or Q (Figures 1 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tPLH,	Maximum Propagation Delay, Set to Q or Q (Figures 2 and 4)	2.0	165 33	205	250 50	ns
PHL	11 Iguito 2 and 47	6.0	28	35	43	
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	20.0	10	10	10	pF

#### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	ECONER
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	35	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	DC Supply Voltage (Referenced to CND)	aaV.

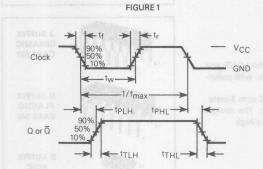
#### TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

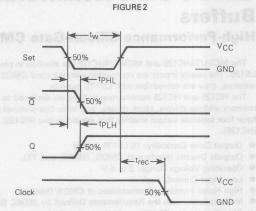
	V02 = 0 V03 = 00V	V	Guaranteed Limit			
Symbol	Parameter WA V D B - 50.9	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, J or K to Clock	2.0	100	125	150	ns
	(Figure 3)	4.5	20	25	30	
	ried beamsund	6.0	17	21	26	
th	Minimum Hold Time, Clock to J or K	2.0	3	3	3	ns
	(Figure 3)	4.5	3	3	3	
	At At At Ac VEG-NAVAVS	6.0	3	3	3	
trec	Minimum Recovery Time, Set Inactive to Clock	2.0	100	125	150	ns
100	(Figure 2)	4.5	20	25	30	
	50 50 63 0C VIA-WV-WV	6.0	17	21	26	
tw	Minimum Pulse Width, Clock	2.0	80	100	120	ns
	(Figure 1)	4.5	16	20	24	
	81 81 81 65 SV NV	6.0	14	17	20	
tw	Minimum Pulse Width, Set	2.0	80	100	120	ns
	(Figure 2)	4.5	16	20	24	
	05 C 18 E 68 S A Am 0 Am 1 Am 1 Am 1	6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times Am Care Land	2.0	1000	1000	1000	ns
	(Figure 1)	4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

### MC54/74HC113

#### SWITCHING WAVEFORMS





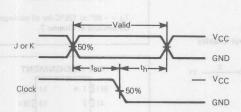
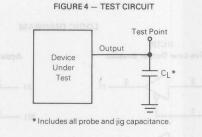
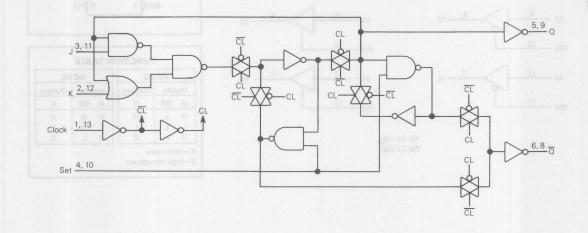


FIGURE 3



#### EXPANDED LOGIC DIAGRAM



## Quad 3-State Noninverting Buffers

## **High-Performance Silicon-Gate CMOS**

The MC54/74HC125 and MC54/74HC126 are identical in pinout to the LS125 and LS126. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC125 and HC126 noninverting buffers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The devices have four separate output enables that are active-low (HC125) or active-high (HC126)

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates

#### LOGIC DIAGRAM

## 

PIN  $14 = V_{CC}$ PIN 7 = GND

## MC54/74HC125 MC54/74HC126



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

#### ORDERING INFORMATION

MC74HCXXXN Plastic MC54HCXXXJ Ceramic MC74HCXXXD SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT

0E1 [	1 •	14 D VC
A1 [	2	13 0E
Y1 [	3	12 A4
0E2 [	4	11 X4
A2 [	5	10 0E
Y2 [	6	9 A3
GND [	7	8 1 Y3

#### FUNCTION TABLE

	HC125			HC126				
Inp	outs	Output	Inp	uts	Output			
Α	OE	Υ	A	OE	Υ			
Н	L	Н	Н	Н	Н			
L	LL	L	L	Н	L			
X	H	Z	X	L	Z			

X = don't care Z = high impedance

#### MC54/74HC125•MC54/74HC126

#### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	٧
Vout	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	a AV.
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260 300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Refere	enced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Type	es san	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> = 2.0 V	0	1000	ns
	(Figure 1)	V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	The state of the s	R - HESTORISE	noV	.,	Gua	aranteed L	imit	
Symbol	Parameter	Test Cond	litions	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤20 μA	JI	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V 18199
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤20 μA	3937	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	Rgue 2	V <sub>in</sub> =V <sub>IH</sub>	I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
MINN DOV O	TOURST CHARGE TERRORS	V <sub>in</sub> = V <sub>IL</sub>	$ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
In 0	Maximum Input Leakage Current	Vin = VCC or GND		6.0	±0.1	±1.0	± 1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impeda Vin = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	ance State	6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$		6.0	8 TORS IN DA	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

			.,	Gua	imit	Syambo		
Symbol	spariov usual to full to a constant spariov usual to be to be sparious and to be to	Parameter 0.1 = 0.2 = 0.		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tpLH,	Maximum Propagation Delay	Input A to Output Y	100	2.0	100	125	150	ns
<sup>†</sup> PHL	(Figures 1 and 3)			4.5 6.0	20 17	25 21	30 26	nil.
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay (Figures 2 and 4)	Output Enable to Y	1910 simes	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tPZL,	Maximum Propagation Delay (Figures 2 and 4)		Tage cope	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tTLH,	Maximum Output Transition (Figures 1 and 3)	Time, Any Output	Pactuget carrie DB1	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	rating Conditions	eqO-batmam	model or	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Outpu State)	t Capacitance (Output in High-In	npedance	01 9001	15	15	15	pF

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
	Used to determine the no-load dynamic power consumption:	DC I nour Vottage, Output Voltage (Batere	usV.
	PD = CPD VCC <sup>2</sup> f+ICC VCC For load considerations, see Chapter 4 subject listing on page 4-2.	Operating Temperature, All Packers Types	pF

#### SWITCHING WAVEFORMS

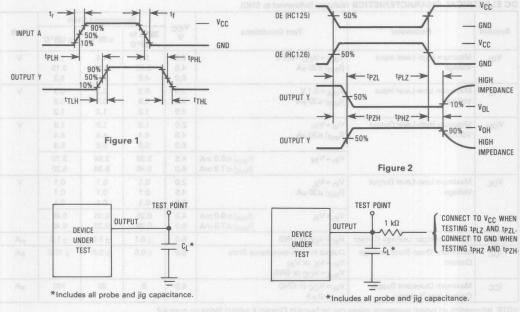


Figure 3. Test Circuit

Figure 4. Test Circuit



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CHARDM HC126
(1/4 of the Device)

SEACTION TABLE

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# Quad 2-Input NAND Gate with Schmitt-Trigger Inputs High-Performance Silicon-Gate CMOS

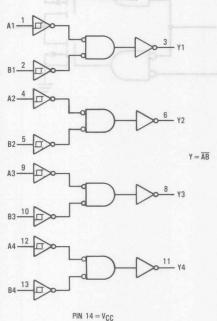
The MC54/74HC132 is identical in pinout to the LS132. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible

with LSTTL outputs.

The HC132 can be used to enhance noise immunity or to square up slowly changing waveforms.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates

#### LOGIC DIAGRAM



PIN 7 = GND

## MC54/74HC132



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT

- I.	ACCIT	OT STATE	
A1 [	1 •	14	] v <sub>cc</sub>
B1 [	2	13	] B4
Y1 [	3	12	] A4
A2 [	4	11	] Y4
B2 [	5	10	B3
Y2 [	6	9	] A3
GND [	7	8	] Y3

#### FUNCTION TABLE

Ir	nputs	Output
А	В	Y
L	L	Н
L	H	Н
Н	L	Н
Н	Н	L

#### **MAXIMUM RATINGS\***

Symbol	Amil been Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{In}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{In} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused

outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	-	no limit*	ns

\*When  $V_{in} \sim 0.5 V_{CC}$ ,  $I_{CC} >$  quiescent current.

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

		und to Chapter 4.	of earning	Guaranteed Limit			moint .
Symbol	Parameter / 0.0 = pgV .2 18 19 laskerT	Test Conditions	V <sub>CC</sub> V	25°C	-40°C to +85°C	-55°C to +125°C	Unit
V <sub>T+</sub> max	Maximum Positive-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> =0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.50 3.15 4.20	1.50 3.15 4.20	1.50 3.15 4.20	٧
V <sub>T +</sub> min	Minimum Positive-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> =0.1 V  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	1.00 2.30 3.00	0.95 2.25 2.95	0.95 2.25 2.95	V
V <sub>T</sub> _max	Maximum Negative-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> =V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	0.90 2.00 2.60	0.95 2.05 2.65	0.95 2.05 2.65	٧
V <sub>T</sub> _ min	Minimum Negative-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> =V <sub>CC</sub> -0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.30 0.90 1.20	0.30 0.90 1.20	0.30 0.90 1.20	V A
V <sub>H</sub> max Note 2	Maximum Hysteresis Voltage (Figure 3)	$V_{\text{out}} = 0.1 \text{ V or } V_{\text{CC}} - 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.20 2.25 3.00	1.20 2.25 3.00	1.20 2.25 3.00	V
V <sub>H</sub> min Note 2	Minimum Hysteresis Voltage (Figure 3)	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.20 0.40 0.50	0.20 0.40 0.50	0.20 0.40 0.50	V

#### NOTES:

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2.  $V_H min > (V_{T+} min) (V_{T-} max); V_H max = (V_{T+} max) + (V_{T-} min).$

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	t This device contains	Visitors I Dril		Guaranteed Limit			Lodwys
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
Voн	Minimum High-Level Output	V <sub>in</sub> ≤V <sub>T</sub> _min or V <sub>T+</sub> max	2.0	1.9	1.9	1.9	V
	Voltage	I <sub>out</sub>   ≤20 μA	4.5 6.0	4.4 5.9	4.4 5.9	4.4 5.9	
	Vous should be constructed angle of the construction of the const	$V_{in} \le V_{T-min}$ or $V_{T+max}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{\text{in}} \ge V_{\text{T}} + \text{max}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
- 178	ego zhel edi heum asugasio	$V_{in} \ge V_{T+} \max$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	± 1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 µA	6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol		.,,	Guaranteed Limit			mani
	Parameter matter matter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input A or B to Output Y	2.0	125	155	190	ns
	(Figures 1 and 2)	4.5	25	31	38	
	39 257 52	6.0	21	26	32	
tTLH, tTHL	Maximum Output Transition Time, Any Output	2.0	75	95	110	ns
	(Figures 1 and 2)	4.5	15	19	22	
		6.0	13	16	19	
Cin	Maximum Input Capacitance	_	10	10	10	pF

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	grico a 24 % mentico M   agestov olodarni / agest	pF

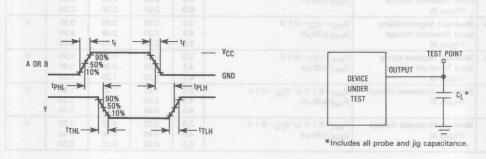


Figure 1. Switching Waveforms

Figure 2. Test Circuit

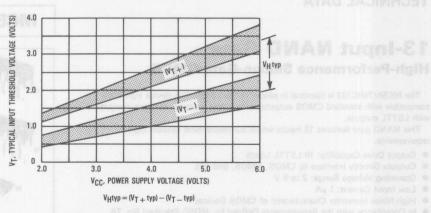
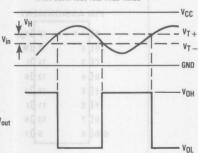


Figure 3. Typical Input Threshold, V<sub>T+</sub>, V<sub>T-</sub>,
Versus Power Supply Voltage

V<sub>cc</sub>

(a) A SCHMITT TRIGGER SQUARES UP INPUTS WITH SLOW RISE AND FALL TIMES



(b) A SCHMITT TRIGGER OFFERS MAXIMUM NOISE IMMUNITY

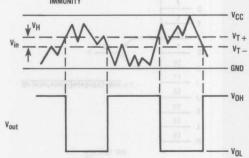


Figure 4. Typical Schmitt-Trigger Applications

## 13-Input NAND Gate

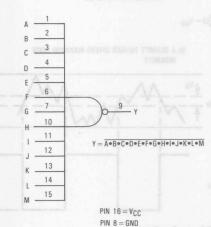
## **High-Performance Silicon-Gate CMOS**

The MC54/74HC133 is identical in pinout to the LS133. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This NAND gate features 13 inputs which surpasses most random logic requirements.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 68 FETs or 17 Equivalent Gates

#### LOGIC DIAGRAM



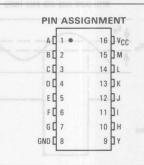
## MC54/74HC133



#### ORDERING INFORMATION

MC74HCXXXN Plastic MC54HCXXXJ Ceramic MC74HCXXXD SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.



#### FUNCTION TABLE

Inputs A through M	Output
All inputs H	L
All other combinations	Н

#### **MAXIMUM RATINGS\***

Symbol	House begins Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	-

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{\text{In}}$  and  $V_{\text{Out}}$  should be constrained to the range  $\text{GND} \leq (V_{\text{In}} \text{ or } V_{\text{Out}}) \leq V_{\text{CC}}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> =2.0 V	0	1000	ns
	(Figure 1)	V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter Parameter	Test Conditions	V	Guaranteed Limit			A. Oak
			VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ m/s}$ $ I_{out}  \le 5.2 \text{ m/s}$		3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ m/s}$ $ I_{out}  \le 5.2 \text{ m/s}$		0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	± 1.0	± 1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 µA	6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input  $t_f = t_f = 6 \text{ ns}$ )

	This device contains	tint/ euteV			Gua	lodinyB		
Symbol	disgs though of ymports	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit	
tPLH, tPHL	Maximum Propagation Dela (Figures 1 and 2)	y, Any Input to Output Y	0	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tTLH, tTHL	Maximum Output Transition (Figures 1 and 2)	Time, Any Output	791G pine	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	0.00	Pagadagat	2010	10	10	10	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	neithin
	Used to determine the no-load dynamic power consumption:	- Placed DIP;10 mW/*C from E8* to 1	neith is
	PD = CPD VCC <sup>2</sup> f + ICC VCC	1001 con 2" West 01 -27 Std 2 minut	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	TOTAL COLLEGE TO SECURE THE PARTY OF THE PAR	

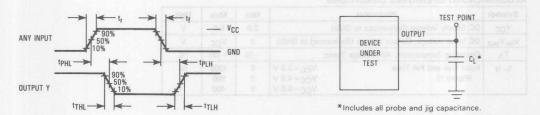
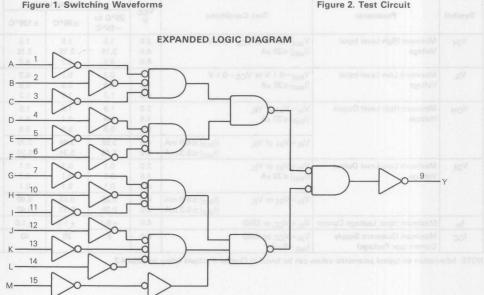


Figure 1. Switching Waveforms Figure 2. Test Circuit



# 1-of-8 Decoder/Demultiplexer with Address Latch

**High-Performance Silicon-Gate CMOS** 

The MC54/74HC137 is identical in pinout to the LS137. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC137 decodes a three-bit Address to one-of-eight active-low outputs. The device has a transparent latch for storage of the Address. Two Chip Selects, one active-low and one active-high, are provided to facilitate the demultiplexing, cascading, and chip-selecting functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the other one active.

The HC137 is the inverting version of the HC237.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 152 FETs or 38 Equivalent Gates

# MC54/74HC137



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648

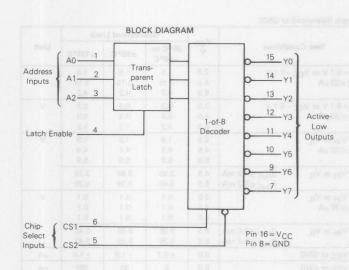


D SUFFIX SOIC CASE 751

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.



A0 1	16 VCC
A1 C 2	15 YO
A2 1 3	14 7 Y1
atch Enable [ 4	13 72
CS2 C 5	12 Y3
CS1 <b>C</b> 6	11 Y4
Y7 <b>0</b> 7	10 Y5
GND 8	9 <b>1</b> Y6

#### **FUNCTION TABLE**

		Inpu	ts			Outputs							
LE	CS1	CS2	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	Н	X	X	X	Н	Н	Н	Н	Н	Н	Н	Н
X	L	X	X	X	X	Н	Н	H	H	Н	H	Н	Н
L	Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
L	Н	L	L	L	Н	Н	L	H	H	Н	Н	Н	H
L	Н	L	L	Н	L	Н	Н	L	H	H	Н	Н	H
L	Н	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
L	Н	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
L	Н	L	Н	L	Н	Н	H	H	H	Н	L	Н	Н
L	Н	L	Н	H	L	H	H	H	H	H	H	L	Н
L	Н	L	Н	Н	Н	H	H	Н	Н	H	Н	H	L
Н	Н	L	X	X	X				+				

\* = Depends upon the Address previously applied while LE was at a low level.

#### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \le (V_{in} \text{ or } V_{out}) \le V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	0	Vcc	V	
TA	Operating Temperature, All Package Types	- 55	+ 125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 2)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Lauri Fraterilla 100		Vcc	Gua	aranteed L	imit	Unit
Symbol	Parameter	Test Conditions	V	25°C to -55°C	≤85°C	≤125°C	
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{Out}  \le 20 \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	ELEST ESSEAS AT ACIVO YT YZ W	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	HERHHIJ H.	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin = VCC or GND	6.0	± 0.1	± 1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

				Gu	aranteed L	mit	
Symbol	s lavel was A zerobA an certail tugit sim is level	asa inguta,	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH	Maximum Propagation Delay, Input A to Output Y	shitphothip	2.0	170	215	255	ns
	(Figures 1 and 6)		4.5 6.0	34 29	43 37	51 43	berople
tPHL	OUTPUTS		2.0	240	300	360	ОЯТИ
Studing	Y0-Y7 — Active-low outputs. One of these eight	a to 185 to	4.5	48	60	72	o rat
	selected when the chip is enabled (CST=H and CI	est one bel	6.0	41	51	61	level d
tPLH	Maximum Propagation Delay, CS1 or CS2 to Output Y	L). For any	2.0	150	190	225	ns
	(Figures 2, 3 and 6)	rigirt a ris to	4.5	30	38	45	mos te
	all others remain at a high level.		6.0	26	33	38	.ls
tPHL			2.0	195	245	295	T By
			4.5	39	49	59	
					42	50	
tPLH	Maximum Propagation Delay, Latch Enable to Output Y	PRECHANCE	2.0	175	220	265	ns
	(Figures 4 and 6)	and the same	4.5	35	44	53	
			6.0	30	37	45	
tPHL			2.0	250	315	375	
	PIGURE 2		4.5	50	63	75	
			6.0	43	54	64	
tTLH,	Maximum Output Transition Time, Any Output		2.0	75	95	110	ns
THL	(Figures 2 and 6)		4.5	15	19	22	
Yec		DOV -	6.0	13	16	19	
Cin	Maximum Input Capacitance		JE.	10	10	10	pF

#### NOTES

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	100	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

#### TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	aros de la proper		Vcc	Gua			
Symbol	Parameter dead	Parameter dend		25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Input A to Latch Enable (Figure 5)		2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns Y augn
th	Minimum Hold Time, Latch Enable to Input A (Figure 5)	H	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
tw	Minimum Pulse Width, Latch Enable (Figure 4)		2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 2)	gaV -	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

A0, A1, A2 (PINS 1, 2, 3) — Address inputs. These inputs, when the chip is enabled, determine which of the eight outputs is selected.

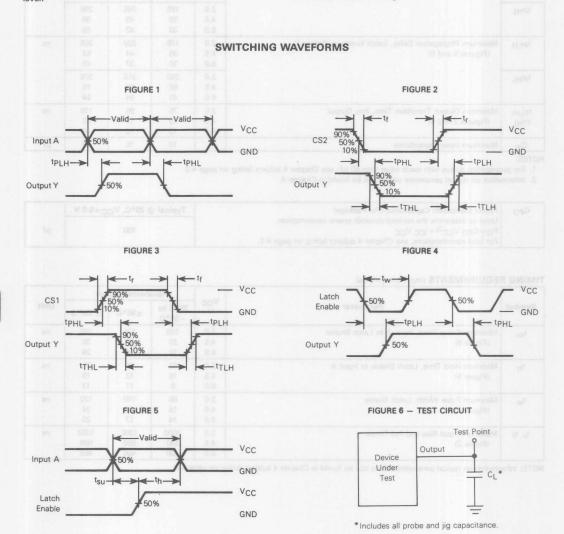
#### **CONTROL INPUTS**

CS1, CS2 (PINS 6, 5) — Chip-Select inputs. For CS1 at a high level and CS2 at a low level, the chip is enabled and the outputs follow the address inputs (Latch Enable = L). For any other combination of CS1 and CS2, the outputs are at a high level.

**LATCH ENABLE (PIN 4)** — Latch-Enable input. A high level at this input latches the Address. A low level at this input allows the outputs to follow the data at the Address pins (CS1 = H and CS2 = L).

#### **OUTPUTS**

Y0-Y7 — Active-low outputs. One of these eight outputs is selected when the chip is enabled (CS1=H and CS2=L) and the data on the A0, A1, and A2 inputs correspond to that particular output. The selected output is at a low level while all others remain at a high level.



# 1-of-8 Decoder/Demultiplexer High-Performance Silicon-Gate CMOS

The MC54/74HC138 is identical in pinout to the LS138. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC138 decodes a three-bit Address to one-of-eight active-low outputs. This device features three Chip Select inputs, two active-low and one active-high to facilitate the demultiplexing, cascading, and chip-selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices

5

CS3

- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 116 FETs or 29 Equivalent Gates

#### LOGIC DIAGRAM 15 YO A0 14 Δ1 Inputs 13 Y2 12 Y3 Active-Low Outputs 11 Y4 10 Y5 9 Y6 CS1 Chip-4 Select Inputs

Pin  $16 = V_{CC}$ Pin 8 = GND

# MC54/74HC138



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT 16 VCC A0 0 1 0 A1 [ 2 15 YO 14 7 Y1 A2 03 CS2 1 4 13 Y2 12 1 Y3 CS3 0 5 11 7 Y4 CS1 0 6 Y7 0 7 10 b Y5 9 1 Y6 GND C

#### **FUNCTION TABLE**

Inputs							Outputs						
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	Н	X	X	X	F,	Н	Н	Н	Н	Н	Н	Н
X	H	X	X	X	X	Н	Н	Н	Н	Н	Н	H	Н
L	X	X	X	X	Χ	Н	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	Н	Н	L	Н	H	Н	H	Н	Н
Н	L	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
Н	L	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
Н	L	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
Н	L	L	H	L	Н	Н	H	Н	Н	Н	L	Н	Н
Н	L	L	H	Н	L	Н	Н	Н	Н	Н	Н	L	Н
Н	L	L	Н	H	Н	Н	H	Н	H	H	H	Н	L

H = high level (steady state) L = low level (steady state) X = don't care

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, VCC and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GN	D)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Ref	erenced to GND)	0	Vcc	٧
TA	Operating Temperature, All Package Ty	/pes	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> =2.0 V	0	1000	ns
	(Figure 2)	V <sub>CC</sub> = 4.5 V	0	500	
	Market Control of the	V <sub>CC</sub> = 6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

		ANTOHING WAVEFORMS	.,	Gua			
Symbol	Parameter	Test Conditions	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  l <sub>out</sub>   ≤20 μA		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Vон	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$		3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	Test Cont.	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}} $ $ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

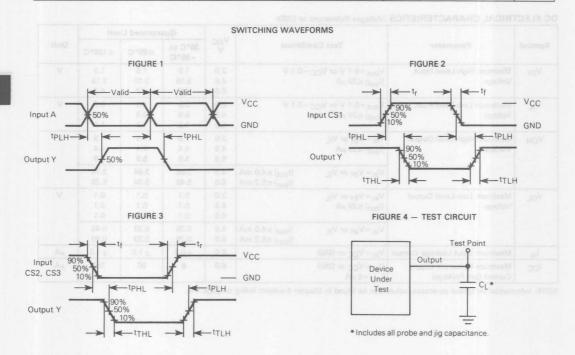
AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input  $t_f = t_f = 6 \text{ ns}$ )

	This device contains p					Gua	aranteed Li	mit	fodeny
Symbol	Symbol	circuitry to guard against	Parameter		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH	Maximum Propagation Delay	, Input A to Out	put Y		2.0	150	190	225	ns
batik mi sanabsa	(Figures 1 and 4)				4.5 6.0	30 26	38 33	45 38	nd.
<sup>t</sup> PHL	elicult. For proper operation Vous should be constraint mone GND's (Violar Vous)				2.0 4.5 6.0	200 40 34	250 50 43	300 60 51	legt lecc Fo
tPLH, tPHL	Maximum Propagation Delay (Figures 2 and 4)		197.5	regularii abarasal	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
<sup>t</sup> PLH	Maximum Propagation Delar (Figures 3 and 4)	, CS2 or CS3 to	Output Y	Package) ando DIP)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
<sup>t</sup> PHL					2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	snolfan godss
tTLH, tTHL	Maximum Output Transition (Figures 2 and 4)		ut og no gasal sag	due A surger?	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance				amor	10	10	10	pF

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	12.0
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	55 (S. mug/R)	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		Pi



#### PIN DESCRIPTIONS

#### ADDRESS INPUTS

A0, A1, A2 (PINS 1, 2, 3) — Address inputs. These inputs, when the chip is selected, determine which of the eight outputs is active-low.

#### CONTROL INPUTS

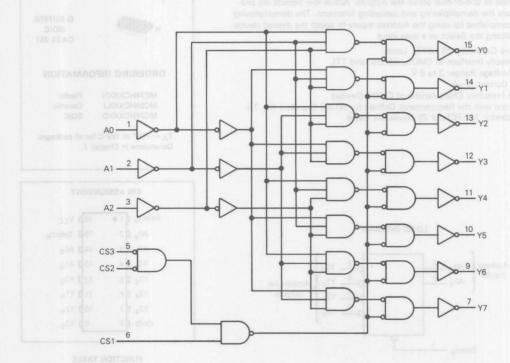
CS1, CS2, CS3 (PINS 6, 4, 5) — Chip select inputs. For CS1 at a high level and CS2, CS3 at a low level, the chip is selected and the

outputs follow the Address inputs. For any other combination of CS1, CS2, and CS3, the outputs are at a logic high.

#### **OUTPUTS**

Y0-Y7 (PINS 15, 14, 13, 12, 11, 10, 9, 7) — Active-low Decoded outputs. These outputs assume a low level when addressed and the chip is selected. These outputs remain high when not addressed or the chip is not selected.

#### EXPANDED LOGIC DIAGRAM



# Dual 1-of-4 Decoder/ Demultiplexer

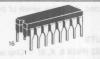
**High-Performance Silicon-Gate CMOS** 

The MC54/74HC139 is identical in pinout to the LS139. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 1-of-4 decoders, each of which decodes a two-bit Address to one-of-four active-low outputs. Active-low Selects are provided to facilitate the demultiplexing and cascading functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and utilizing the Select as a data input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 100 FETs or 25 Equivalent Gates

# MC54/74HC139



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



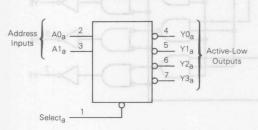
D SUFFIX SOIC CASE 751

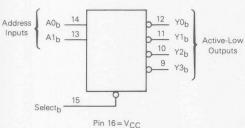
#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM





Pin 8 = GND

#### PIN ASSIGNMENT

Selecta	10	16 VC	
A0a	2	15 Sel	ectb
A1a	13	14 A0b	
Y0a	<b>C</b> 4	13 A1 <sub>b</sub>	
Y1 <sub>a</sub>	<b>C</b> 5	12 Y0b	
Y2 <sub>a</sub>	6	11 7 Y1b	
Y3 <sub>a</sub>	7	10 7 Y2b	
GND	8	9 1 Y3 <sub>b</sub>	
	Con I I		

#### FUNCTION TABLE

Inputs				Out	puts	
Select	A1	A0	Y0	Y1	Y2	Y3
Н	X	X	Н	Н	Н	Н
L	L	L	L	Н	H	H
L	L	Н	Н	L	H	Н
L	Н	L	Н	H	L	Н
L	Н	Н	Н	Н	H	L

X = don't care

### MAXIMUM RATINGS\*

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
7L 7g	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC. Unused inputs must always be tied

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to	GND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (	Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package	Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V	0	1000 500	ns
	(Figure 1)	V <sub>CC</sub> =6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	K A 2007	Advant	Acres 1		Gua			
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	- Cannon	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		Vin=VIH or VIL	I <sub>out</sub>   ≤4.0 mA  I <sub>out</sub>   ≤5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	oswes) haltinU mail	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
		Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	Grane the appropriate	6.0	±0.1	±1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

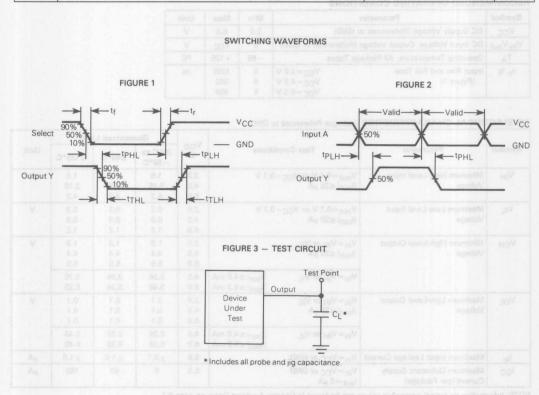
AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	This device contains		Hold water		Gua	mit	Symbo	
Symbol	due to high state of space	Parameter 100 - 10		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Dela			2.0	150	190	225	ns
tpHL (Figures 1 and 3)				4.5 6.0	30 26	38 33	45 38	
	Maximum Propagation Dela (Figures 2 and 3)	y, Input A to Output Y		2.0	150 30	190 38	225 45	ns
33V26	oV to mV3≥ 0V9 egran 2			6.0	26	33	38	
tTLH,	Maximum Output Transition	Time, Any Output	C Perchagar	2.0	75	95	110	ns
<sup>t</sup> THL	(Figures 1 and 3)			4.5 6.0	15 13	19 16	22 19	
Cin	Maximum Input Capacitano	e	(C Package)	D2 TI	10	10	10	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Decoder)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	55	pF



#### PIN DESCRIPTIONS

#### ADDRESS INPUTS

A0<sub>a</sub>, A1<sub>a</sub>, A0<sub>b</sub>, A1<sub>b</sub> (PINS 2, 3, 14, 13) — Address inputs. These inputs, when the respective 1-of-4 decoder is enabled, determine which of its four active-low outputs is selected.

#### CONTROL INPUTS

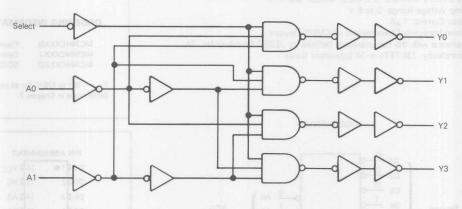
Select<sub>a</sub>, Select<sub>b</sub> (PINS 1, 15) — Active-low select inputs. For a low level on this input, the outputs for that particular

decoder follow the Address inputs. A high level on this input forces all outputs to a high level.

# OUTPUTS TO THE TOTAL THE TOTAL TO THE TOTAL

 $Y0_a-Y3_a$ ,  $Y0_b-Y3_b$  (PINS 4-7, 12, 11, 10, 9) — Active-low outputs. These outputs assume a low level when addressed and the appropriate Select input is active. These outputs remain high when not addressed or the appropriate Select input is inactive.

# EXPANDED LOGIC DIAGRAM (1/2 OF DEVICE)



# Advance Information

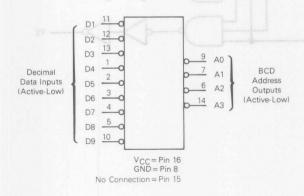
# Decimal-to-BCD Encoder High-Performance Silicon-Gate CMOS

The MC54/74HC147 is identical in pinout to the LS147. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device encodes nine active-low data inputs to four active-low BCD Address Outputs, ensuring that only the highest order active data line is encoded. The implied decimal zero condition is encoded when all nine data inputs are at a high level (inactive)

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 136 FETs or 34 Equivalent Gates

#### LOGIC DIAGRAM



# MC54/74HC147



#### ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramio
MC74HCXXXD	SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# PIN ASSIGNMENT D4 1 1 16 VCC D5 2 15 NC D6 3 14 A3 D7 4 13 D3 D8 5 12 D2 A2 6 11 D1 A1 7 10 D9 GND 8 9 A0 NC = No Connection

#### FUNCTION TABLE

			Ir	npu	ts					Out	put	S
D9	D8	D7	D6	D5	D4	D3	D2	D1	АЗ	A2	A1	A0
Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
H	Н	Н	Н	Н	Н	Н	H	L	Н	Н	Н	L
H	Н	Н	Н	Н	H	Н	L	X	Н	H	L	Н
Н	Н	Н	Н	Н	Н	L	X	X	Н	Н	L	L
H	Н	Н	Н	Н	L	X	X	X	Н	L	Н	Н
Н	Н	Н	Н	L	X	X	X	X	Н	L	Н	L
Н	Н	Н	L	X	X	X	X	X	Н	L	L	Н
Н	Н	L	X	X	X	X	X	X	Н	L	L	L
Н	L	X	X	X	X	X	X	Χ	L	Н	Н	Н
L	X	X	X	X	X	X	X	X	L	Н	Н	L

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\text{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to G	IND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (F	Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

		a		Vcc	Gua	aranteed Li	mit	
Symbol	Parameter	Test Cond	Test Conditions		25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> -  I <sub>out</sub>   ≤ 20 μA	-0.1 V	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -  I <sub>out</sub>   ≤20 μA	-0.1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	VOH Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or $V_{IL}$	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	± 0.1	± 1.0	± 1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

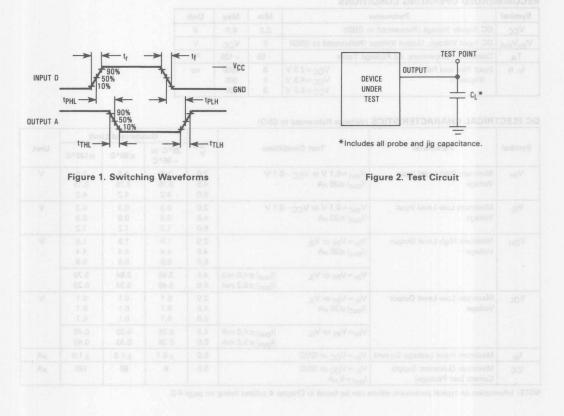
AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

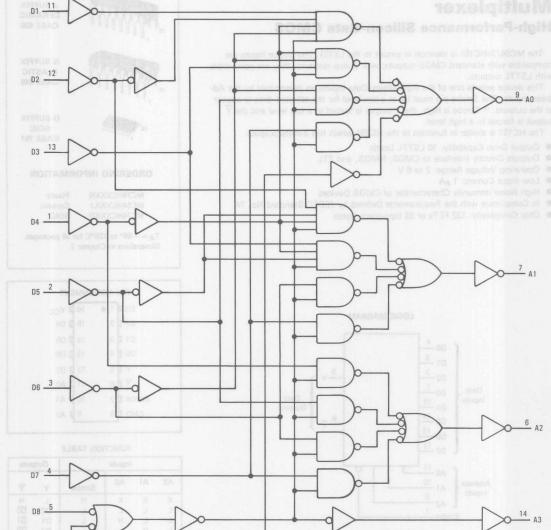
	ardistrios epivob aletT			.,	Gua	aranteed Li	mit	tedmyl
Symbol	directory to quard against	Parameter		VCC	25°C to	-0500	12500	Unit
	sepation offsta right of sub-			1070	-55°C	≤85°C	≤125°C	
tPLH,	Maximum Propagation Dela	y, Input D to Output	A	2.0	220	275	330	ns
tPHL	(Figures 1 and 2)			4.5	44	55	66	
Uditherin oppulisasi	pleded side of property			6.0	37	47	56	
tTLH,	Maximum Output Transition	Time, Any Output	40.4	2.0	75	95	110	ns
THL	(Figures 1 and 2)			4.5	15	19	22	
annV2	range GND s (Vic or Veus)			6.0	13	16	19	
Cin	Maximum Input Capacitance	9	-002 to	gering Parkag	10	10	10	pF

#### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	Plante St. may 2 Verm 35 St. Steel 4	pF





5

D9 10

The MC54/74HC151 is identical in pinout to the LS151. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Strobe pin must be at a low level for the selected data to appear at the outputs. If Strobe is high, the Y output is forced to a low level and the  $\overline{Y}$  output is forced to a high level.

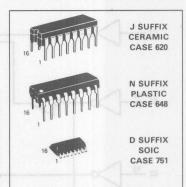
The HC151 is similar in function to the HC251 which has 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 132 FETs or 33 Equivalent Gates

#### LOGIC DIAGRAM D0 -D1 3 D2 -2 Data D3 -D4 15 Inputs D5 14 D6 13 12 D7 A0 -11 Address Inputs A2 -Strobe -Pin 16 = VCC

Pin 8 = GND

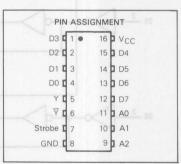
MC54//4HC151



#### ORDERING INFORMATION

MC74HCXXXN Plastic MC54HCXXXJ Ceramic MC74HCXXXD SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.



#### **FUNCTION TABLE**

		Inputs	1	Out	puts
A2	A1	A0	Strobe	Y	7
X	X	X	Н	L	Н
L	L	L	L	DO	DO
L	L	Н	L	D1	D1
L	Н	L	L	D2	D2
L	Н	Н	L	D3	D3
Н	L	L	L	D4	D4
Н	L	Н	L	D5	D5
H	Н	L	L	D6	D6
Н	Н	Н	L	D7	D7

D0, D1. . . D7= the level of the respective D input

Data

Outputs

Symbol	Simil beath Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	.E-0 m	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1) V	CC = 2.0 V CC = 4.5 V CC = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

					Gua	aranteed L	imit	
Symbol	Parameter	rest Conditions		VCC V	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> −  I <sub>out</sub>   ≤ 20 μA	0.1 V 988 30 00 1	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	y V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -  I <sub>out</sub>   ≤20 μA			0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Vон	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
		Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

<sup>†</sup>Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

#### AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	bus Unit This daylos contains			Gua	Bymhol		
Symbol	Parameter D. C. o.		V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, Input D to Output Y o	Ϋ́	2.0	185	230	280	ns
tPHL (Figures 1, 3 and 6)	(Figures 1, 3 and 6)		4.5 6.0	37 31	46 39	56 48	
t <sub>PLH</sub> , Maximum Propagation De t <sub>PHL</sub> (Figures 2 and 6)	Maximum Propagation Delay, Input A to Output Y o (Figures 2 and 6)	rΫ	2.0 4.5	205 41	255 51	310 62	ns
	759 movi sange GND sc(V) <sub>In</sub> or V <sub>OM</sub>	T 1980 pinus	6.0	35	43	53	OF
tPLH,	Maximum Propagation Delay, Strobe to Output Y or	▼ 1eeeeee	2.0	125	155	190	ns
<sup>t</sup> PHL	(Figures 4, 5 and 6)		4.5 6.0	25 21	31 26	38 32	ers <sup>T</sup>
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 6)		2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	mended Operation C	100071 9	10	10	10	pF

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	ECOMN
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+I <sub>CC</sub> VCC	36	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	DC Specify Volumes (Referenced or	any

#### PIN DESCRIPTIONS

#### INPUTS

D0, D1, . . . , D7 (PINS 4, 3, 2, 1, 15, 14, 13, 12) — Data inputs. Data on any one of these eight binary inputs may be selected to appear on the output.

#### CONTROL INPUTS

A0, A1, A2 (PINS 11, 10, 9) — Address inputs. The data on these pins are the binary address of the selected input (see the Function Table).

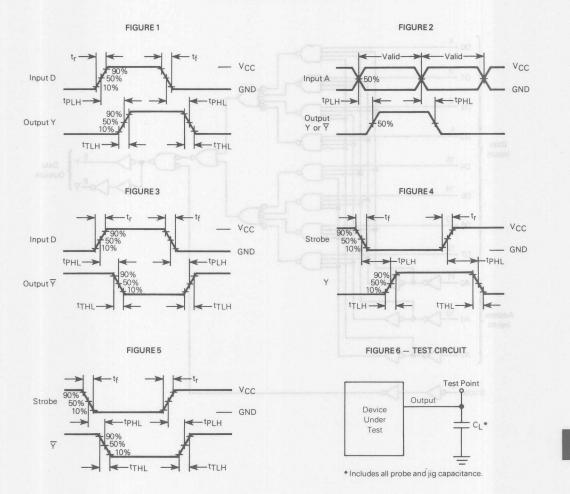
STROBE (PIN 7) — Strobe. This input pin must be at a low level for the selected data to appear at the outputs. If the Strobe pin is high, the Y output is forced to a low level and the  $\overline{Y}$  output is forced to a high level.

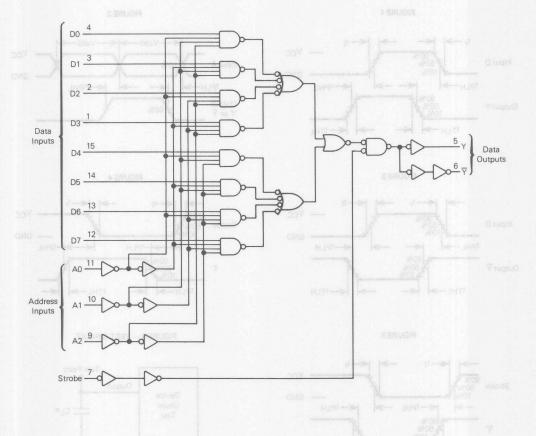
#### **OUTPUTS**

Y,  $\overline{Y}$  (PINS 5, 6) — Data outputs. The selected data is presented at these pins in both true (Y output) and complemented ( $\overline{Y}$  output) forms.

#### MC54/74HC151

#### **SWITCHING WAVEFORMS**





# MC54/74HC153

# Dual 4-Input Data Selector/ Multiplexer

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC153 is identical in pinout to the LS153. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The Address Inputs select one of four Data Inputs from each multiplexer. Each multiplexer has an active-low Strobe control and a noninverting output.

The HC153 is similar in function to the HC253, which has 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 108 FETs or 27 Equivalent Gates



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



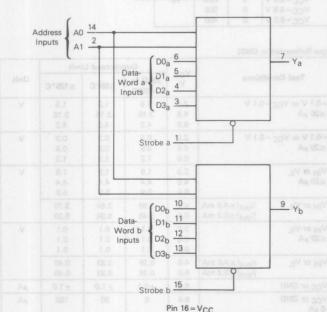
D SUFFIX SOIC CASE 751

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.





Pin 8 = GND

#### PIN ASSIGNMENT

1 •	16	VCC
2	15	Strobe
3	140	A0
4	13	D3 <sub>b</sub>
5	12	D2 <sub>b</sub>
6	11 2	D1 <sub>b</sub>
7 999	10	D0b
8	9	Yb
	1 • 2 3 4 5 6 7 8	2 15 3 3 14 4 13 5 12 3 6 11 3 7 10 3

#### FUNCTION TABLE

	Inputs		
A1	A0	Strobe	Y
X	X	Н	L
L	L	norm Ferm	D0
L	Н	anthon	D1
Н	L	L	D2
Н	Н	L	D3

D0, D1, D2, and D3= the level of the respective Data

#### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GN	ND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	٧
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	. 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	fer shaen	2, 1		V	Guaranteed Limit			
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Uni
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
VOH	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
Y	A) A0 Strobe	Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
EQ .	j H H	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	201	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

#### AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

Symbol Parameter Parameter	-4-12-1-1-1-1-1 CO - 2-10-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1	200000		Gua	UL ATA		
	na) — Osta	VCC	25°C to -55°C	≤85°C	≤125°C	Unit	
tPLH, tPHL	Maximum Propagation Delay, Input D to Output Y (Figures 1 and 4)		2.0 4.5 6.0	140 28 24	175 35 30	210 42 36	ns
tPLH, tPHL	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 4)	atugal east ad) is ass	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLH, tPHL	Maximum Propagation Delay, Strobe to Output Y (Figures 3 and 4)		2.0 4.5 6.0	95 19 16	120 24 20	145 29 25	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)		2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	o i dadinatica	_	10	10	10	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Multiplexer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC	31	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

#### SWITCHING WAVEFORMS

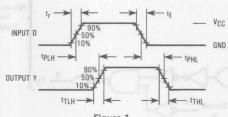


Figure 1

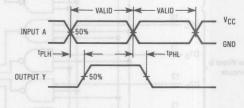


Figure 2

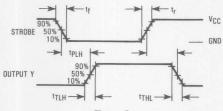
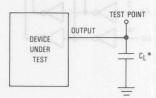


Figure 3



\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

# DATA INPUTS

 $D0_a$ - $D3_a$ ,  $D0_b$ - $D3_b$  (PINS 3, 4, 5, 6, 10, 11, 12, 13) — Data Inputs. With the outputs enabled, the addressed Data Inputs appear at the Y outputs.

#### **CONTROL INPUTS**

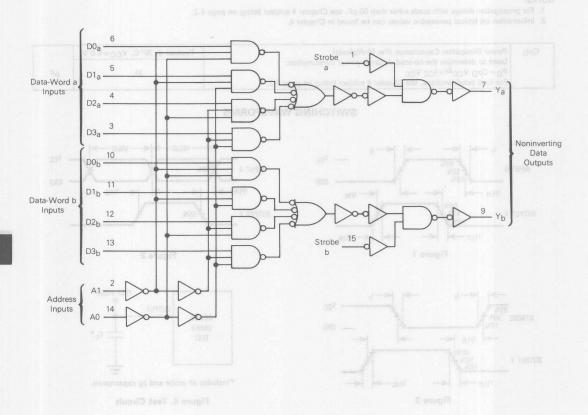
A0, A1 (PINS 2, 14) - Address Inputs. These inputs address the pair of Data Inputs which appear at the corresponding outputs.

STROBE (PINS 1, 15) — Active-low Strobe. A low level applied to these pins enables the corresponding outputs.

#### OUTPUTS of a highly valid mollegeon 4 man

Ya, Yb (PINS 7, 9) - Noninverting data outputs.

EXPANDED LOGIC DIAGRAM



# 1-of-16 Decoder/Demultiplexer High-Performance Silicon-Gate CMOS

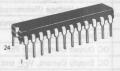
The MC54/74HC154 is identical in pinout to the LS154. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device, when enabled, selects one of 16 active-low outputs. Two active-low Chip Selects are provided to facilitate the chip-select, demultiplexing, and cascading functions. When either Chip Select is high, all outputs are high. The demultiplexing function is accomplished by using the Address inputs to select the desired device output. Then, while holding one chip select input low, data can be applied to the other chip select input (see Application Note).

The HC154 is primarily used for memory address decoding and data routing applications.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 192 FETs or 48 Equivalent Gates

# MC54/74HC154



J SUFFIX CERAMIC CASE 758



N SUFFIX PLASTIC CASE 724



DW SUFFIX SOIC CASE 751E

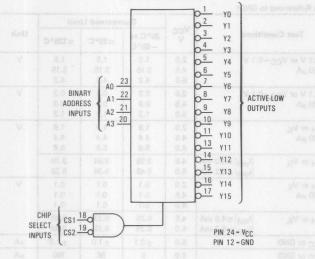
#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXDW

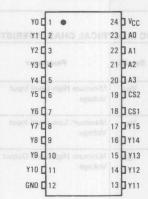
Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT



#### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	٧
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±25	mA
ICC	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND≤(Vin or Vout)≤VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced	to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 2) V	CC = 2.0 V CC = 4.5 V CC = 6.0 V	0 0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	1203		11 14 20		Gua	ranteed Li	imit	
Symbol	Parameter	Test Cond	ditions	VCC	25°C to -55°C	≤85°C	≤125°C	Uni
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -  I <sub>out</sub>   ≤20 μA	-0.1 V	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 * 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -  I <sub>out</sub>   ≤20 μA	-0.1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
VOH	Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	at Tro	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
	610 12	Vin=VIH or VIL	$ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	any Arc	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	V <sub>in</sub> =	Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	33
lin	Maximum Input Leakage Current	Vin=VCC or GND	088-15 (89	6.0	±0.1	± 1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

#### AC ELECTRICAL CHARACTERISTICS (C1 = 50 pF. Input tr = tf = 6 ns)

Symbol		Vcc	Gua			
	Parameter		25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, Input A to Output Y	2.0	190	240	285	ns
tPHL	tpHL (Figures 1 and 3)	4.5	38	48	57	
Well and		6.0	32	41	48	
tPLH,	Maximum Propagation Delay, CS to Output Y	2.0	175	220	265	ns
tPHL	(Figures 2 and 3)	4.5	35	44	53	
	The state of the s	6.0	30	37	45	HALLA
tTLH,	Maximum Output Transition Time, Any Output	2.0	75	95	110	ns
tTHL	(Figures 2 and 3)	4.5	15	19	22	
		6.0	13	16	19	
Cin	Maximum Input Capacitance	-	10	10	10	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:		
	PD=CPD VCC2f+ICC VCC	80	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

#### PIN DESCRIPTIONS

#### **INPUTS**

A0, A1, A2, A3 (PINS 23, 22, 21, 20) — Address inputs. These inputs, when the 1-of-16 decoder is enabled, determine which of its sixteen active-low outputs is selected.

#### **OUTPUTS**

Y0-Y15 (PINS 1-11, 13-17) — Active-low outputs. These outputs assume a low level when addressed and both chip-

select inputs are active. These outputs remain high when not addressed or a chip-select input is high.

#### **CONTROL INPUTS**

CS1, CS2 (PINS 18, 19) — Active-low chip-select inputs. With low levels on both of these inputs, the outputs of the decoder follow the Address inputs. A high level on either input forces all outputs high.

#### **FUNCTION TABLE**

		INP	UTS										OUT	PUTS	3						
CS	1 CS2	A3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15
L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	H	H	H	H	H	L	H	Н	Н	H	H	Н	Н	Н	H	H	H	Н
L	L	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	H	Н	H	Н	Н	Н
L	L	L	H	L	H	H	H	Н	H	Н	L	H	Н	H	Н	Н	H	Н	H	Н	Н
L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	H	H	Н	Н	H	Н	H	Н	Н	H	L	Н	Н	H	H	Н	Н	Н	H
L	L	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	H	Н	Н	Н	Н	H
L	L	Н	L	L	Н	H	H	H	H	Н	Н	Н	H	H	L	Н	Н	Н	Н	Н	Н
L	L	Н	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
L	L	Н	L	Н	Н	Н	H	H	H	H	Н	H	Н	H	H	H	L	H	Н	Н	Н
L	L	Н	Н	L	L	Н	H	H	H	Н	H	H	Н	Н	Н	H	H	L	Н	Н	Н
L	L	Н	Н	L	Н	Н	Н	H	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
L	L	H	H	H	L	Н	Н	Н	H	Н	H	Н	H	H	Н	Н	H	H	Н	L	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	X	X	X	X	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
H	L	X	X	X	X	Н	Н	H	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
Н	Н	X	X	X	X	H.	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н

H = High Level, L = Low Level, X = Don't Care

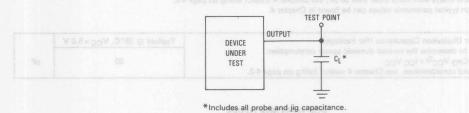
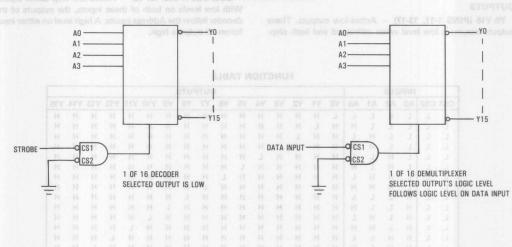
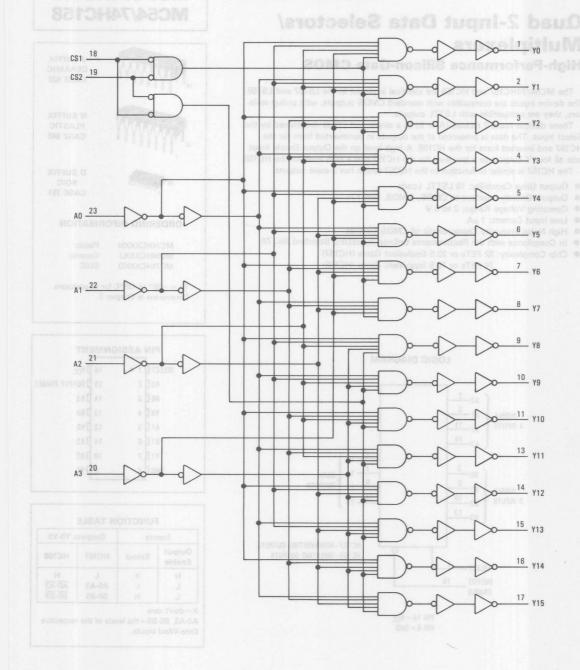


Figure 3. Test Circuit

## atugal toolee-gifu wol-evitoA - (et at auris TYPICAL APPLICATIONS





# Quad 2-Input Data Selectors/ Multiplexers

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC157 and HC158 are identical in pinout to the LS157 and LS158. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices route 2 nibbles (A or B) to a single port (Y) as determined by the Select input. The data is presented at the outputs in noninverted form for the HC157 and inverted form for the HC158. A high level on the Output Enable input sets all four Y outputs to a low level for the HC157 and a high level for the HC158.

The HC157 is similar in function to the HC257 which has 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 82 FETs or 20.5 Equivalent Gates (HC157)

74 FETs or 18.5 Equivalent Gates (HC158)

# MC54/74HC157 MC54/74HC158



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



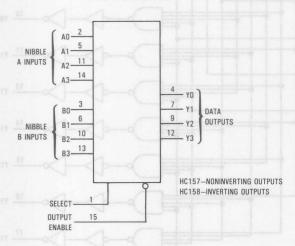
D SUFFIX SOIC CASE 751

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



PIN 16 = VCC

PIN 8 = GND

#### PIN ASSIGNMENT

SELECT [	1 •	16	Dvcc
A0 [	2	15	OUTPUT ENABLE
В0 [	3	14	] A3
YO [	4	13	<b>1</b> B3
A1 [	5	12	1 Y3
B1 [	6	11	] A2
Y1 [	7	10	] B2
GND [	8	9	1 Y2

#### **FUNCTION TABLE**

Inp	uts	Outputs Y0-			
Output Enable	Select	HC157	HC158		
Н	X	L	Н		
L	L	A0-A3	A0-A3		
L	Н	B0-B3	B0-B3		

X = don't care

A0-A3, B0-B3 = the levels of the respective Data-Word Inputs.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and

#### MC54/74HC157•MC54/74HC158

#### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	TO Visign
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

SOIC Package: -7 mW/°C from 65° to 125°C

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	(National & Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	9.4.2	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referen	ced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V	0	1000 500	ns
		V <sub>CC</sub> =6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	BIOH and too level virol a rated	outputs in level, the outputs i	V <sub>CC</sub>	Gua	oi s s		
Symbol	Parameter	Test Conditions		25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
VoH	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### MC54/74HC157 • MC54/74HC158

AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	This device contains	Parameter 0.V or 3.0			Gua	losimy?		
Symbol	enlings braug of virtuality engastory offsets rigin of sub-				25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay,	Input A or B to Output Y		2.0	125	155	190	ns
tPHL	(Figures 1, 2, and 7)			4.5 6.0	25 21	31 26	38 32	
tPLH, tPHL	Maximum Propagation Delay, (Figures 3, 4, and 7)	Select to Output Y	1910 oim	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tPLH, tPHL	Maximum Propagation Delay, (Figures 5, 6, and 7)	Output Enable to Output Y	fegulas?	2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
tTLH, tTHL	Maximum Output Transition T (Figures 1, 2, and 7)	ime, Any Output	Packaged and DIP)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	anulifon Confidence	oO between	Tico <del>ol</del> i si	10	10	10	pF

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	HMOS
	Used to determine the no-load dynamic power consumption:  PD = CPD VCc <sup>2</sup> f + ICC VCC	33 (HC157)	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	35 (HC158)	nav

#### PIN DESCRIPTIONS

#### INPUTS

A0, A1, A2, A3 (PINS 2, 5, 11, 14) — Nibble A inputs. The data present on these pins is transferred to the outputs when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form for the HC157 and inverted form for the HC158.

B0, B1, B2, B3 (PINS 3, 6, 10, 13) — Nibble B inputs. The data present on these pins is transferred to the outputs when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form for the HC157 and inverted form for the HC158.

#### **OUTPUTS**

Y0, Y1, Y2, Y3 (PINS 4, 7, 9, 12) — Data outputs. The selected input Nibble is presented at these outputs when the

Output Enable input is at a low level. The data present on these pins is in its noninverted form for the HC157 and inverted form for the HC158. For the Output Enable input at a high level, the outputs are at a low level for the HC157 and at a high level for the HC158.

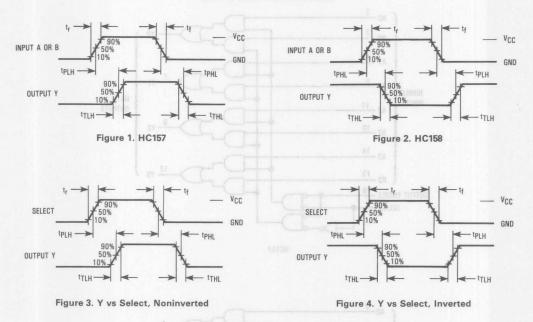
#### **CONTROL INPUTS**

**SELECT (PIN 1)** — Nibble select. This input determines the data word to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

OUTPUT ENABLE (PIN 15) — Output Enable input. A low level on this input allows the selected input data to be presented at the outputs. A high level on this input sets all outputs to a low level for the HC157 and to a high level for the HC158.

## MC54/74HC157•MC54/74HC158

#### SWITCHING WAVEFORMS



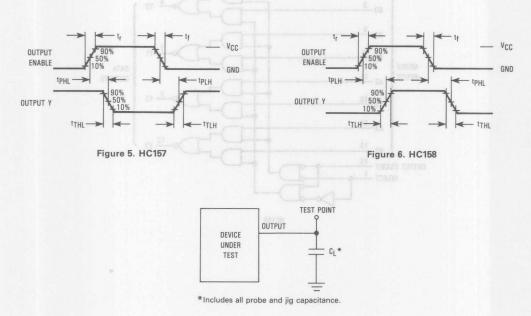


Figure 7. Test Circuit

A0 -2

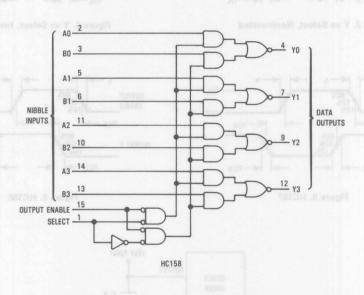
OUTPUT ENABLE 15
SELECT 1

HC157

DATA

12 Y3

OUTPUTS



# Presettable Counters High-Performance Silicon-Gate CMOS

The MC54/74HC160 through HC163 are identical in pinout to the LS160 through LS163, respectively. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC160 and HC162 are programmable BCD counters with asynchronous and synchronous Reset inputs, respectively. The HC161 and HC163 are programmable 4-bit binary counters with asynchronous and synchronous reset, respectively.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates

Count

Mode

BCD

Binary

BCD

Binary

Device

HC160

HC161

HC162

HC163

MC54/74HC160 MC54/74HC161 MC54/74HC162 MC54/74HC163



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



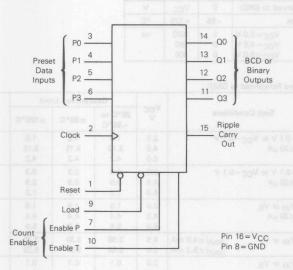
D SUFFIX SOIC CASE 751

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



Reset Mode

Asynchronous

Asynchronous

Synchronous

Synchronous

#### PIN ASSIGNMENT

Reset [	10	16 VCC
Clock [	2	15 Ripple Carry Out
P0 [	3	14 <b>1</b> Q0
P1 [	4	13 01
P2 [	5	12 <b>2</b> Q2
P3 [	6	11 D Q3
Enable P I	7	10 Enable T
GND I	8	9 Load

#### **FUNCTION TABLE**

		Inputs		Output	
Clock	Reset*	Load	Enable P	Enable T	Q
5	L	X	X	X	Reset
_	Н	L	X	X	Load Preset Data
5	H	H	Н	H	Count
_	Н	Н	Pacifical Pacific	X	No Count
_	Н	Н	X	L	No Count

\*HC162 and HC163 only. HC160 and HC161 are Asynchronous-Reset Devices

H = high level

L = low level

X = don't care

gluÖ leveli-woll m

#### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND≤(Vin or Vout)≤VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from  $100^\circ$  to  $125^\circ$ C SOIC Package: -7 mW/°C from  $65^\circ$  to  $125^\circ$ C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

		( E0	Vcc	Gua	aranteed L	imit	
Symbol	Symbol Parameter	Parameter Test Conditions		25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VILO	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤20 μA		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	le el ons	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
tuspoO O	Ingess Load Snable P Enable T	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	6.0	±0.1	±1.0	± 1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA		8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

	Successed Limit				Guaranteed Limit				
Symbol	D*857 2 0*88		arameter		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
fmax	Maximum Clock Fre	equency (50%	Duty Cycle)*	destil	2.0	6.0	4.8	4.0	MH
IIIux	(Figures 1 and 7)				4.5	30	24	20	
	33 35				6.0	35	28	24	
tPLH	Maximum Propagat	ion Delay, Clo	ock to Q		2.0	170	215	255	ns
	(Figures 1 and 7)				4.5	34	43	51	
	25 25				6.0	29	37	43	
tPHL	200 240			Irdno 8819H box 9	2.0	205	255	310	
	69 69				4.5	41	51	62	
	11 NE	22	0.0		6.0	35	43	53	
tPHL	Maximum Propagat	ion Delay, Re	set to Q (HC160	and HC161 Only)	2.0	210	265	315	ns
	(Figures 2 and 7)				4.5	42	53	63	
	43 81				6.0	36	45	54	
tPLH	Maximum Propagat	ion Delay, En	able T to Ripple	Carry Out	2.0	160	200	240	ns
	(Figures 3 and 7)	101	8.6		4.5	32	40	48	
	13				6.0	27	34	41	
tPHL	9 5				2.0	195	245	295	
					4.5	39	49	59	
	E 2				6.0	33	42	50	
tPLH	Maximum Propagat	ion Delay, Clo	ock to Ripple Car	ry Out	2.0	175	220	265	ns
	(Figures 1 and 7)				4.5	35	44	53	
	8 8				6.0	30	37	45	
tPHL	2 1				2.0	215	270	325	
	3 3				4.5	43	54	65	
	8 8				6.0	37	46	55	
tPHL	Maximum Propagat	ion Delay, Res	set to Ripple Carn	Out (HC160 and HC161	2.0	220	275	330	ns
	Only)		8.8		4.5	44	55	66	
	(Figures 2 and 7)		0.8		6.0	37	47	56	
tTLH,	Maximum Output T	ransition Time	e, Any Output	.5000	2.0	75	95	110	ns
tTHL	(Figures 1 and 7)		8.6		4.5	15	19	22	
	26 32				6.0	13	16	19	
	-					10		-	pF

<sup>\*</sup>Applies to noncascaded/nonsynchronously clocked configurations only. With synchronously cascaded counters, (1) Clock to Ripple Carry Out propagation delays, (2) Enable T or Enable P to Clock setup times, and (3) Clock to Enable T or Enable P hold times determine f<sub>max</sub>. However, if Ripple Carry Out of each stage is tied to the Clock of the next stage (nonsynchronously clocked), the f<sub>max</sub> in the table above is applicable. See Applications Information in this data sheet.

For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	polmi (370
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	60	pF

#### TIMING REQUIREMENTS (Input t==t4=6 ps)

	Van Gustarisad Umit	1/	Gua	aranteed L	imit	
Symbol	OFERS OFERS Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Preset Data Inputs to Clock (Figure 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t <sub>su</sub>	Minimum Setup Time, Load to Clock (Figure 5)	2.0 4.5 6.0	135 27 23	170 34 29	205 41 35	ns
t <sub>su</sub>	Minimum Setup Time, Reset to Clock (HC162 and HC163 only) (Figure 4)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
t <sub>su</sub>	Minimum Setup Time, Enable T or Enable P to Clock (Figure 6)	2.0 4.5 6.0	200 40 34	250 50 43	300 60 51	ns
th	Minimum Hold Time, Clock to Preset Data Inputs (Figure 5)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
th	Minimum Hold Time, Clock to Load (Figure 5)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
th	Minimum Hold Time, Clock to Reset (HC162 and HC163 only) (Figure 4)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
th	Minimum Hold Time, Clock to Enable T or Enable P (Figure 6)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (HC160 and HC161 only) (Figure 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
<sup>t</sup> rec	Minimum Recovery Time, Load Inactive to Clock (Figure 5)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>W</sub>	Minimum Pulse Width, Reset (HC160 and HC161 only) (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

MC54/74HC160•MC54/74HC161•MC54/74HC162•MC54/74HC163

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### **FUNCTION DESCRIPTION**

The HC160/161/162/163 are programmable 4-bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading, and count-enable controls.

The HC160 and HC162 are BCD counters with asynchronous Reset, and synchronous Reset, respectively. The HC161 and HC163 are binary counters with asynchronous Reset and synchronous Reset, respectively.

#### **INPUTS**

Clock (Pin 2) — The internal flip-flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as resetting (HC162 and HC163) and loading occur with the rising edge of the Clock input.

Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6) — These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip-flops and appear at the counter outputs. P0 (pin 3) is the least-significant bit and P3 (pin 6) is the most-significant bit.

#### OUTPUTS

Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11) — These are the counter outputs (BCD or binary). Q0 (pin 14) is the least-significant bit and Q3 (pin 11) is the most-significant bit.

Ripple Carry Out (Pin 15) — When the counter is in its maximum state (1001 for the BCD counters or 1111 for the binary counters), this output goes high, providing an external look-ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equations for this output are:

Ripple Carry Out = Enable T•Q0•Q1•Q2•Q3 for BCD counters HC160 and HC162

Ripple Carry Out = Enable T•Q0•Q1•Q2•Q3
for binary counters HC161 and HC163

#### CONTROL FUNCTIONS

Resetting — A low level on the Reset pin (pin 1) resets the internal flip-flops and sets the outputs (Q0 through Q3) to a low level. The HC160 and HC161 reset asynchronously, and the HC162 and HC163 reset with the rising edge of the Clock input (synchronous reset).

Loading — With the rising edge of the Clock, a low level on Load (pin 9) loads the data from the Preset Data Input pins (P0, P1, P2, P3) into the internal flip-flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

Although the HC160 and HC162 are BCD counters, they may be programmed to any state. If they are loaded with a state disallowed in BCD code, they will return to their normal count sequence within two clock pulses (see the Output State Disagram)

Count Enable/Disable — These devices have two countenable control pins: Enable P (pin 7) and Enable T (pin 10). The devices count when these two pins and the Load pin are high. The logic equation is:

#### Count Enable = Enable P. Enable T. Load

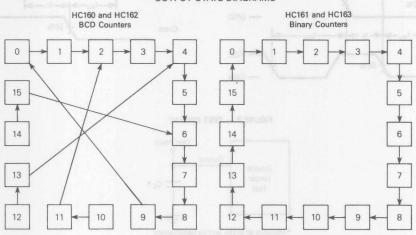
The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a countenable control; Enable T is both a count-enable and a Ripple-Carry Output control.

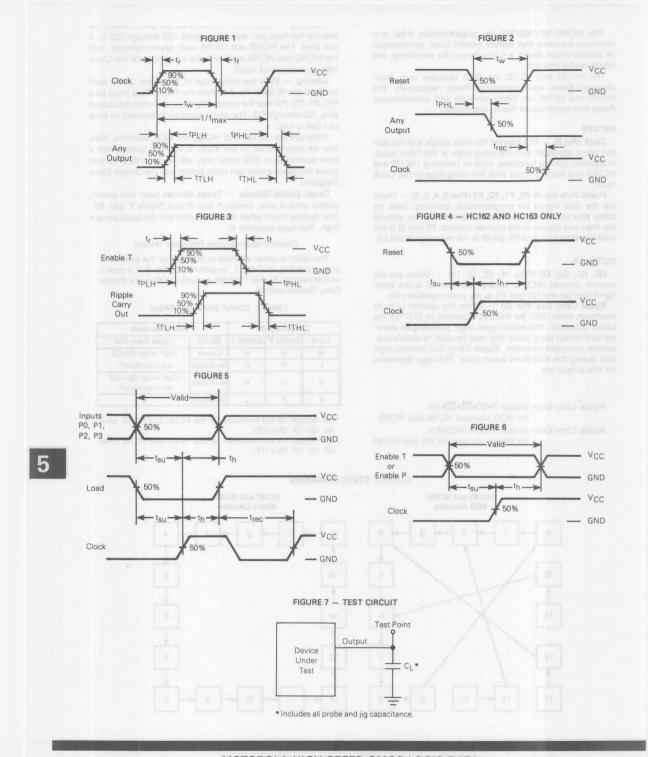
TABLE 1. COUNT ENABLE/DISABLE

(	Control Inpu	its	Result at Outputs		
Load	Enable P	Enable T	Q0-Q3	Ripple Carry Out	
Н	Н	Н	Count	High when Q0-Q3	
L	Н	Н	No Count	are maximum*	
×	L	н	No Count	High when Q0-Q3 are maximum*	
X	X	L	No Count	ule / _ Fa	

- \*Q0 through Q3 are maximum for the HC160 and HC162 when Q3 Q2 Q1 Q0=1001.
- Q0 through Q3 are maximum for the HC161 and HC163 when Q3 Q2 Q1 Q0=1111.

**OUTPUT STATE DIAGRAMS** 





QO

12 Q2

11

Ripple Carry Out 15

Load

5-169

Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

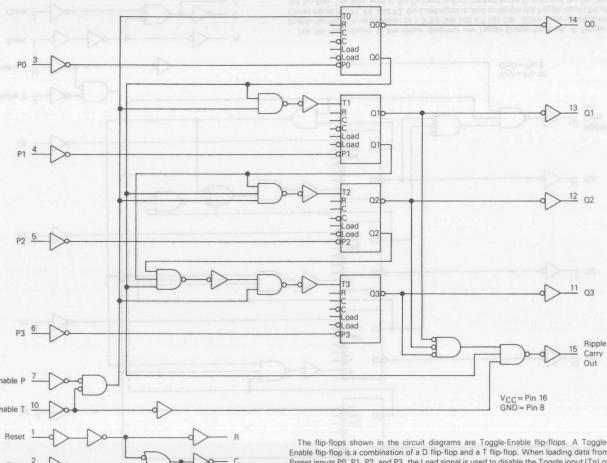
A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

- Load

Load

5-170

# MC54HC161 • MC74HC161 4-Bit Binary Counter with Asynchronous Reset



Load

Load

The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

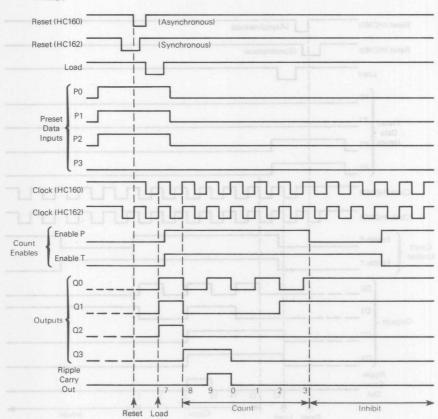
A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

### MC54/74HC160•MC54/74HC161•MC54/74HC162•MC54/74HC163

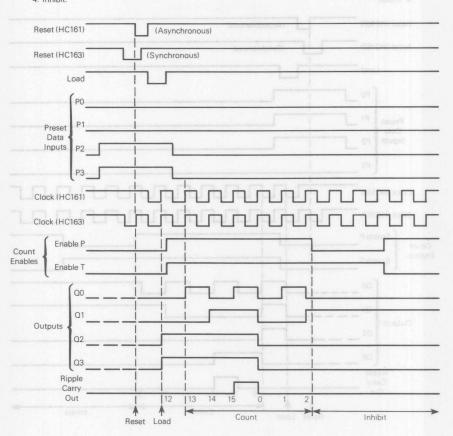
HC160, HC162 TIMING DIAGRAM

Sequence illustrated in waveforms:

- 1. Reset outputs to zero.
- 2. Preset to BCD seven.
- 3. Count to eight, nine, zero, one, two, and three.
- 4. Inhibit.

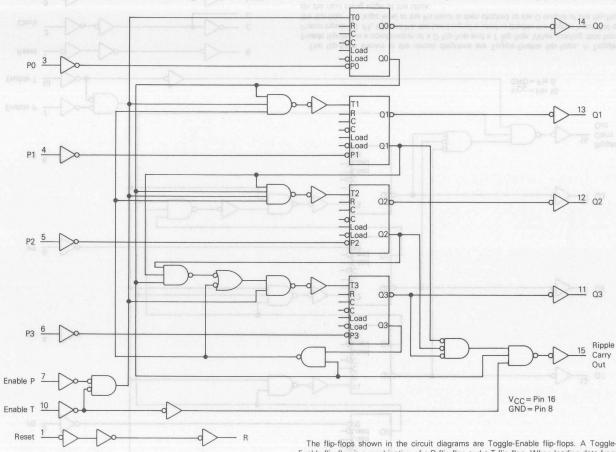


- 1. Reset outputs to zero.
- 2. Preset to binary twelve.
- 3. Count to thirteen, fourteen, fifteen, zero, one, and two.
- 4. Inhibit.



Load

5-173



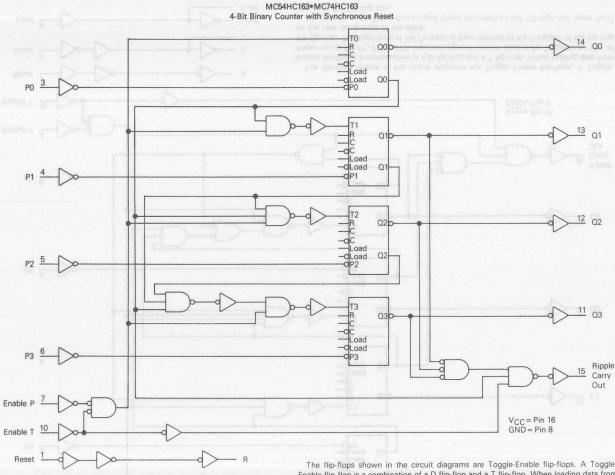
The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs PO, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

Load

Load

5-174



Load

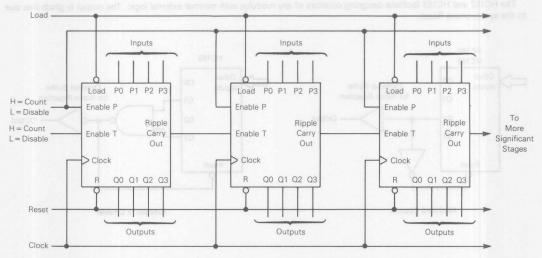
The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

#### MC54/74HC160•MC54/74HC161•MC54/74HC162•MC54/74HC163

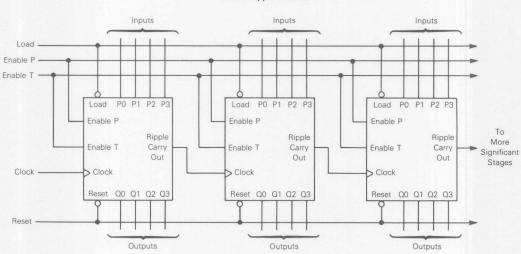
# TYPICAL APPLICATIONS CASCADING

#### N-Bit Synchronous Counters



NOTE: When used in these cascaded configurations the clock f<sub>max</sub> guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set up times between Enable (Port) and Clock.

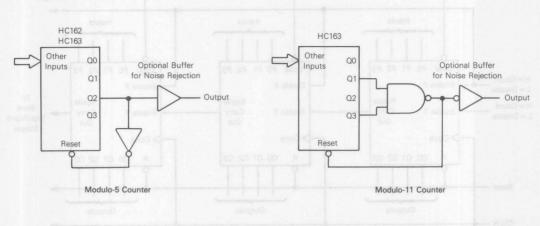
#### Nibble Ripple Counter



### MC54/74HC160•MC54/74HC161•MC54/74HC162•MC54/74HC163

# TYPICAL APPLICATIONS VARYING THE MODULUS

The HC162 and HC163 facilitate designing counters of any modulus with minimal external logic. The output is glitch-free due to the synchronous Reset.



# 8-Bit Serial-Input/Parallel-Output **Shift Register**

## **High-Performance Silicon-Gate CMOS**

The MC54/74HC164 is identical in pinout to the LS164. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The MC54/74HC164 is an 8-bit, serial-input to parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. The active-low asynchronous Reset overrides the Clock and Serial Data inputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 244 FETs or 61 Equivalent Gates

# MC54/74HC164



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC **CASE 646** 



D SUFFIX SOIC CASE 751A

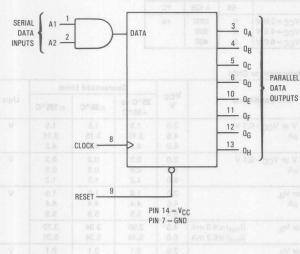
#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT 14 D VCC 13 1 aH 12 1 a<sub>G</sub> DAD a<sub>B</sub> [ 11 1 QF 10 ] QE ac [ 9 RESET

8 CLOCK

# **FUNCTION TABLE**

an [

GND [

Inputs				Out	pı	uts		
Reset	Clock	A1	A2	QA	QB			αн
L	X	X	Х	L	L			L
Н	~	X	X		no ch	na	ng	е
Н	1	Н	D	D	QAr			QGn
Н	_	D	Н	D				QGn

D = data input

QAn - QGn = data shifted from the previous stage on a rising edge at the clock input.

l	k	3	۹	
ľ	ě	2	2	

-,	A SECULIAR S		
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	٧
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GNE	0)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Refe	erenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Ty	pes	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V	0	1000 500	ns
		V <sub>CC</sub> = 6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	ff a limb	ATRO & OF		Gua	imit		
Symbol	Parameter	Test Conditions	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	Reset Clock A1A2 QA	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{Out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
n die pr	D = data Input OAn · Ogn = data sirted Inc	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	± 0.1	±1.0	± 1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

			Gu	aranteed L	imit	Unit
Symbol	Parameter Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	
f <sub>max</sub>	(Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
<sup>t</sup> PHL	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0 4.5 6.0	205 41 35	255 51 43	310 62 53	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	_	10	10	10	pF

#### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:		
	PD = CPD VCC2f + ICC VCC	140	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

#### TIMING REQUIREMENTS (Input tr = tf = 6 ns)

	- A		V	Gua	aranteed Li	mit	0
Symbol	Parameter		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, A1 or A2 to Clock (Figure 3)		2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
th	Minimum Hold Time, Clock to A1 or A2 (Figure 3)		2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
trec	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	nov	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	10k)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>W</sub>	Minimum Pulse Width, Reset (Figure 2)	ana	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)		2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

## PIN DESCRIPTIONS TO BE AN ADDITIONAL DATE OF THE PIN DESCRIPTIONS TO BE ADDITIONAL OF THE PIN DESCRIPTION OF THE PIN DESCRIPTION

#### INPUTS

A1, A2 (PINS 1, 2) — Serial Data Inputs. Data at these inputs determine the data to be entered into the first stage of the shift register. For a high level to be entered into the shift register, both A1 and A2 inputs must be high, thereby allowing one input to be used as a data-enable input. When only one serial input is used, the other must be connected to VCC.

CLOCK (PIN 8) — Shift Register Clock. A positive-going transition on this pin shifts the data at each stage to the next stage. The shift register is completely static, allowing clock rates down to DC in a continuous or intermittent mode.

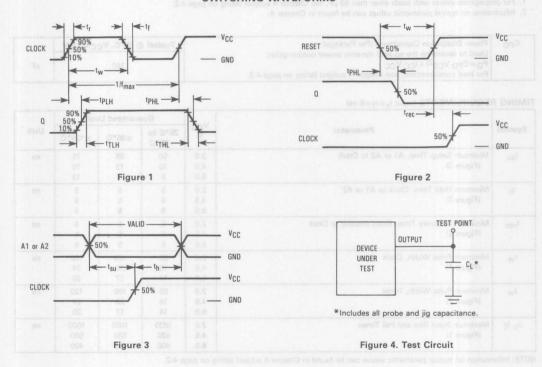
#### **OUTPUTS**

 $Q_A - Q_H$  (PINS 3, 4, 5, 6, 10, 11, 12, 13) — Parallel Shift Register Outputs. The shifted data is presented at these outputs in true, or noninverted, form.

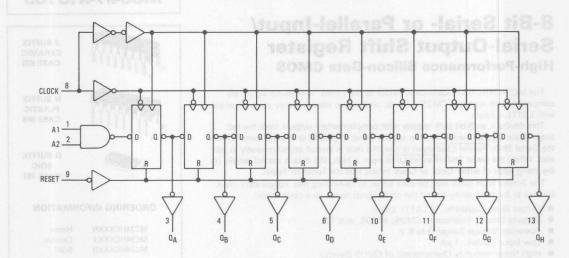
#### CONTROL INPUT

RESET (PIN 9) — Active-Low, Asynchronous Reset Input. A low voltage applied to this input resets all internal flip-flops and sets outputs  $Q_A = Q_H$  to the low level state.

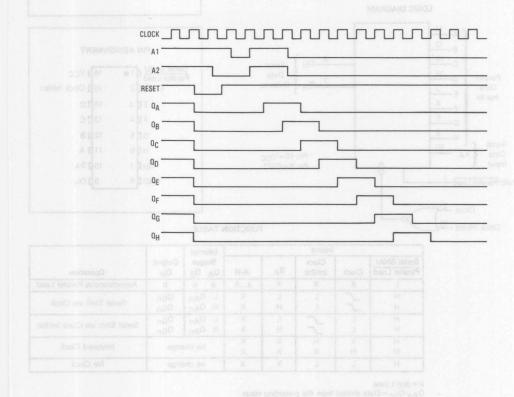
#### SWITCHING WAVEFORMS



#### **EXPANDED LOGIC DIAGRAM**



#### TIMING DIAGRAM



## **High-Performance Silicon-Gate CMOS**

The MC54/74HC165 is identical in pinout to the LS165. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is an 8-bit shift register with complementary outputs from the last stage. Data may be loaded into the register either in parallel or in serial form. When the Serial Shift/Parallel Load input is low, the data is loaded asynchronously in parallel. When the Serial Shift/Parallel Load input is high, the data is loaded serially on the rising edge of either Clock or Clock Inhibit (see the Function Table).

The 2-input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 286 FETs or 71.5 Equivalent Gates

# 16

J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



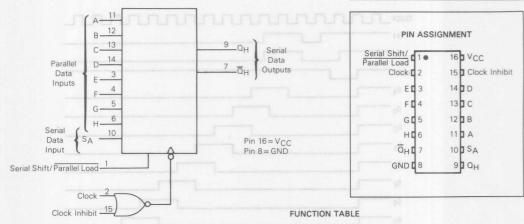
D SUFFIX SOIC CASE 751

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



		Inputs			Internal		
Serial Shift/ Parallel Load	Clock	Clock Inhibit	SA	A-H	Stages Q <sub>A</sub> Q <sub>B</sub>	Output Q <sub>H</sub>	Operation
L	X	X	X	ah	a b	h	Asynchronous Parallel Load
H	7	L L	L H	×	L Q <sub>An</sub> H Q <sub>An</sub>	Q <sub>Gn</sub> Q <sub>Gn</sub>	Serial Shift via Clock
H H	L L	7	L H	X	L Q <sub>An</sub> H Q <sub>An</sub>	Q <sub>Gn</sub> Q <sub>Gn</sub>	Serial Shift via Clock Inhibit
H H	X H	H X	×	X	no ch	ange	Inhibited Clock
Н	L	L	X	X	no ch	ange	No Clock

X = don't care

Q<sub>An</sub>-Q<sub>Gn</sub>= Data shifted from the preceding stage

#### MAXIMUM BATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$  VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referen	nced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	C. S. sand	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				V	Gua	No.		
Symbol	Parameter	Test Cor	ditions	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or VCC}$ $ I_{out}  \le 20 \mu\text{A}$	-0.1 V	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC}$ $ I_{out}  \le 20 \mu\text{A}$	-0.1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
		Vin=VIH or VIL	$ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin = VCC or GND		6.0	± 0.1	± 1.0	± 1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

## MC54/74HC165

AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	Value contain line device contains	.,	Gua	aranteed L	imit	Unit
Symbol	Parameter 1.5 of 3.0	VCC	25°C to -55°C	≤85°C	≤125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 8)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock (or Clock Inhibit) to $Q_{\mbox{\scriptsize H}}$ or $\overline{Q}_{\mbox{\scriptsize H}}$ (Figures 1 and 8)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPLH, tPHL	Maximum Propagation Delay, Serial Shift/ $\overline{Parallel}$ Load to $\Omega_H$ or $\overline{\Omega}_H$ (Figures 2 and 8)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLH, tPHL	Maximum Propagation Delay, Input H to $\Omega_H$ or $\overline{\Omega}_H$ (Figures 3 and 8)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	ят °20 m	10	10	10	pF

#### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	308
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	estelli e attov suguo erentov sugui 100 g	nF
	For load considerations, see Chapter 4 subject listing on page 4-2.	Operator Temperature, All Peckage Typ	A

| Commission | Com

TIMING REQUIREMENTS (Input te = te = 6 ns)

	FIGURE 2 - PARALLEL-LOAD MODE	V	Gua	aranteed Li	mit	
Symbol	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Parallel Data Inputs to Serial Shift/Parallel Load	2.0	100	125	150	ns
	(Figure 4)	4.5	20	25	30	liebel stood
מאם	The billing and	6.0	17	21	26	
t <sub>su</sub>	Minimum Setup Time, Input SA to Clock (or Clock Inhibit)	2.0	100	125	150	ns
	(Figure 5)	4.5	20	25	30	
	新	6.0	17	21	26	1,555
t <sub>su</sub>	Minimum Setup Time, Serial Shift/Parallel Load to Clock (or Clock Inhibit)	2.0	100	125	150	ns
	(Figure 6)	4.5	20	25	30	Disport
		6.0	17	21	26	
t <sub>su</sub>	Minimum Setup Time, Clock to Clock Inhibit	2.0	100	125	150	ns
Ju	(Figure 7)	4.5	20	25	30	
		6.0	17	21	26	
th	Minimum Hold Time, Serial Shift/Parallel Load to Parallel Data Inputs	2.0	5	5	5	ns
	(Figure 4)	4.5	5	5	5	
		6.0	5	5	5	
th	Minimum Hold Time, Clock (or Clock Inhibit) to Input SA	2.0	5	5	5	ns
	(Figure 5)	4.5	5	5	5	
	NGA H-A arron	6.0	5	5	5	Haugat.
th	Minimum Hold Time, Clock (or Clock Inhibit) to Serial Shift/Parallel Load	2.0	5	5	5	ns
	(Figure 6)	4.5	5	5	5	
	at months for the state	6.0	5	5	5	n Brand
trec	Minimum Recovery Time, Clock to Clock Inhibit	2.0	100	125	150	ns
	(Figure 7)	4.5	20	25	30	200 T 5
	Newscard Boot lidered Jes	6.0	17	21	26	
tw	Minimum Pulse Width, Clock (or Clock Inhibit)	2.0	80	100	120	ns
	(Figure 1)	4.5	16	20	24	
		6.0	14	17	20	
tw	Minimum Pulse Width, Serial Shift/Parallel Load	2.0	80	100	120	ns
	(Figure 2)	4.5	16	20	24	
	SCOM TERRELIAINSE - S INDOM	6.0	14	17 -	20	
tr, tf	Maximum Input Rise and Fall Times	2.0	1000	1000	1000	ns
	(Figure 1)	4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### PIN DESCRIPTIONS

#### INPUTS

A, B, C, D, E, F, G, H (PINS 11, 12, 13, 14, 3, 4, 5, 6) — Parallel Data inputs. Data on these inputs are asynchronously entered in parallel into the internal flip-flops when the Serial Shift/Parallel Load input is low.

SA (PIN 10) — Serial Data input. When the Serial Shift/Parallel Load input is high, data on this pin is serially entered into the first stage of the shift register with the rising edge of the Clock.

#### **CONTROL INPUTS**

SERIAL SHIFT/PARALLEL LOAD (PIN 1) — Data-entry control input. When a high level is applied to this pin, data at the Serial Data input  $(S_{\mbox{\scriptsize A}})$  are shifted into the register with the rising edge of the Clock. When a low level is applied to

this pin, data at the Parallel Data inputs are asynchronously loaded into each of the eight internal stages.

CLOCK, CLOCK INHIBIT (PINS 2, 15) — Clock inputs. These two clock inputs function identically. Either may be used as an active-high clock inhibit. However, to avoid double clocking, the inhibit input should go high only while the clock input is high.

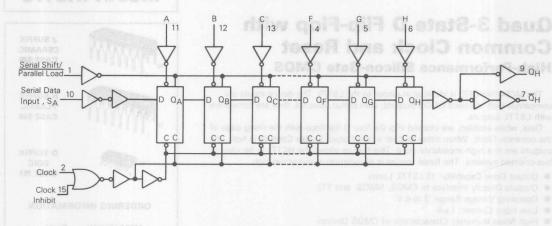
The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

#### OUTPUTS

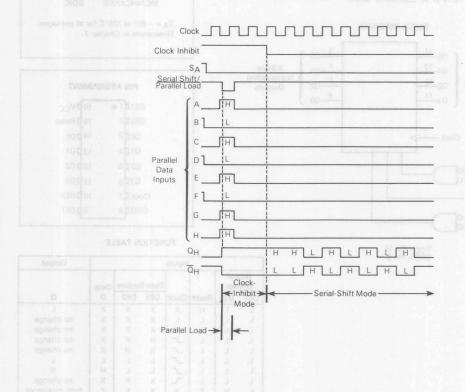
 $Q_H$ ,  $\overline{Q}_H$  (PINS 9, 7) — Complementary Shift Register outputs. These pins are the noninverted and inverted outputs of the eighth stage of the shift register.

FIGURE 2 - PARALLEL-LOAD MODE

FIGURE 1 - SERIAL-SHIFT MODE



TIMING DIAGRAM



# Quad 3-State D Flip-Flop with Common Clock and Reset

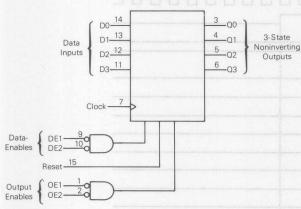
**High-Performance Silicon-Gate CMOS** 

The MC54/74HC173 is identical in pinout to the LS173. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data, when enabled, are clocked into the four D flip-flops with the rising edge of the common Clock. When either or both of the Output Enable Controls is high, the outputs are in a high-impedance sta\*e. This feature allows the HC173 to be used in bus-oriented systems. The Reset feature is asynchronous and active-high.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 208 FETs or 52 Equivalent Gates

#### **BLOCK DIAGRAM**



V<sub>CC</sub>= Pin 16 GND= Pin 8

## MC54/74HC173



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT

OE1	1 •	16	VCC
OE2	2	15	Reset
00	3	14	D0
Q1 [	4	13	D1
Q2 <b>E</b>	5	12	D2
03	6	11	D3
Clock [	7	10	DE2
GND	8	9	DE1

#### FUNCTION TABLE

		Output					
	tput			Data I	Enables	Data	
OE1	OE2	Reset	Clock		DE2	D	Q
L	L	Н	X	X	X	X	L
L	L	L	L	X	X	X	no change
L	L	- thou	Н	X	X	X	no change
L	L	L	5	Н	X	X	no change
L	L	L	5	X	Н	X	no change
L	L	L	5	L	L	L	L
L	L	L	5	L	L	н	Н
L	L	L	~	X	X	X	no change
L	Н	X	X	X	X	X	high impedance
Н	L	X	X	X	X	X	high impedance
Н	Н	X	X	X	X	X	high impedance

#### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP:  $-10~\text{mW}/^{\circ}\text{C}$  from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	southeant	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)			Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V	0	1000 500	ns
	VBB-say 200 m lesionT	V <sub>CC</sub> = 6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

		A Prese to politic towic	o A relia	Gua	aranteed Li	imit	
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
VOH	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	851 811 08	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5	0.1 0.1	0.1 0.1	0.1 0.1	V
	80 100 120 16 20 24 14 17 20	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 6.0 \text{ mA}$ $ I_{\text{out}}  \le 7.8 \text{ mA}$	6.0 4.5 6.0	0.1 0.26 0.26	0.1 0.33 0.33	0.1 0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	± 1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	6.0	±0.5	±5.0	± 10.0	μА
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

	Value Unit This device contains				Gua	aranteed Li	mit	Unit
Symbol	Parameter W. W. B. B. B.		VCC	25°C to -55°C	≤85°C	≤125°C		
fmax	Maximum Clock Frequency (Figures 1 and 5)	50% Duty Cycle)		2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Dela (Figures 1 and 5)	, Clock to Q	PHG Sines	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPHL	Maximum Propagation Dela (Figures 2 and 5)	, Reset to Q	Topsdage J	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPLZ, tPHZ	Maximum Propagation Dela (Figures 3 and 6)	, Output Enable to Q	Categoric CAP1	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL, tPZH	Maximum Propagation Dela (Figures 3 and 6)	, Output Enable to Q	oranmended Operation	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition (Figures 1 and 5)	Time, Any Output	District A set	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance			NOTE L	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Outp State)	ut Capacitance (Output in High-	mpedance	- 1 - 1	15	15	15	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption: PD = CPD VCC <sup>2</sup> f + ICC VCC	THICAL CHASENCTERISTICS IN	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

#### TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	Parameter		Guaranteed Limit			1919
Symbol			25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Input D or DE to Clock (Figure 4)	2.0 4.5	100 20	125 25	150 30	ns
W	0.1 0.1 0.0 0.0 0.0 0.0	6.0	17	21	26	Venu
th	Minimum Hold Time, Clock to Input D or DE (Figure 4)	2.0 4.5 6.0	3 3 3	3 3 3	3 3	ns
trec	Minimum Recovery Time, Reset Inactive to Clock	2.0	90	115	135	ns
ν	(Figure 2)	4.5 6.0	18 15	23 20	27 23	
t <sub>W</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
tw	Minimum Pulse Width, Reset	2.0	80	100	120	ns
	(Figure 2)	4.5 6.0	16 14	20 17	24 20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	2.0	1000	1000	1000	ns
	(Figure 1)	4.5 6.0	500 400	500 400	500 400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### **INPUTS**

D0, D1, D2, D3 (PINS 14, 13, 12, 11) — 4-bit data inputs. Data on these pins, when enabled by the Data-Enable Controls, are entered into the flip-flops on the rising edge of the clock

CLOCK (PIN 7) - Clock input.

#### **OUTPUTS**

Q0, Q1, Q2, Q3 (PINS 3, 4, 5, 6) — 3-state register outputs. During normal operation of the device, the outputs of the D flip-flops appear at these pins. During 3-state operation, these outputs assume a high-impedance state.

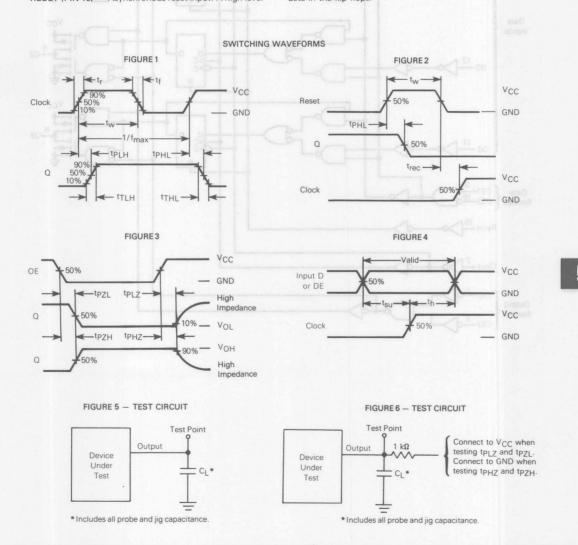
#### CONTROL INPUTS

RESET (PIN 15) - Asynchronous reset input. A high level

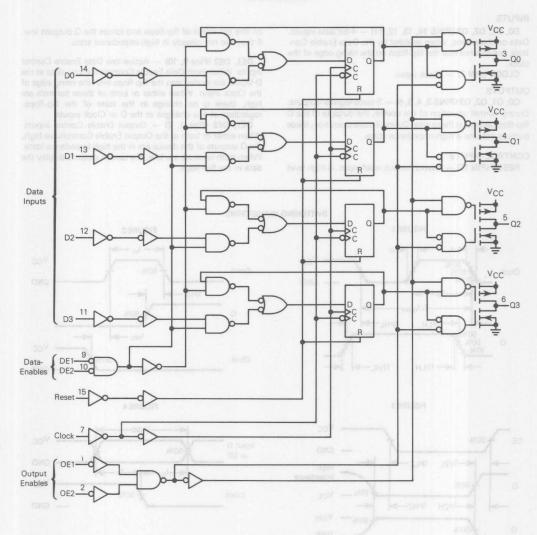
on this pin resets all flip-flops and forces the Q outputs low, if they are not already in high-impedance state.

DE1, DE2 (Pins 9, 10) — Active-low Data Enable Control inputs. When both Data Enable Controls are low, data at the D inputs are loaded into the flip-flops with the rising edge of the Clock input. When either or both of these controls are high, there is no change in the state of the flip-flops, regardless of any changes at the D or Clock inputs.

OE1, OE2 (Pins 1, 2) — Output Enable Control inputs. When either or both of the Output Enable Controls are high, the Q outputs of the device are in the high-impedance state. When both controls are low, the device outputs display the data in the flip-flops.



LOGIC DETAIL



# **Hex D Flip-Flop with Common Clock and Reset High-Performance Silicon-Gate CMOS**

The MC54/74HC174 is identical in pinout to the LS174. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active-low.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 162 FETs or 40.5 Equivalent Gates

# MC54/74HC174



J SUFFIX CERAMIC **CASE 620** 



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC **CASE 751** 

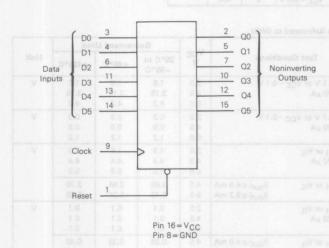
#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD SOIC

Plastic Ceramic

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT

Reset	1 •	16	Vcc
00 0	2	15	Q5
D0 C	3	14	D5
D1 D	4	13	D4
Q1 <b>C</b>	5	12	Q4
D2 <b>C</b>	6	110	D3
Q2 <b>[</b>	7	10	Q3
GND C	8	9	Clock

### FUNCTION TABLE

	Inputs		Output
Reset	Clock	D	Q
L	X	X	L
Н	_	Н	H_O
Н		L	L
Н	L	X	no change
Н	~	X	no change

г	Р		٩	
L	a	n	9	
7	٦	ν.	4	

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stq</sub>	Storage Temperature	-65 to +150	°C
TL PRIES O	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	et 50 00	1	V <sub>CC</sub>	Guaranteed Limit				
Symbol	Parameter	Test Conditions		25°C to -55°C	≤85°C	≤125°C	Uni	
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
Handa Clock D 0			l <sub>out</sub>   ≤ 4.0 mA l <sub>out</sub>   ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VoL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
agnario o			l <sub>out</sub>   ≤ 4.0 mA l <sub>out</sub>   ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	± 1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA		6.0	. 8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

Symbol		Vcc	Guaranteed Limit			
	Parameter		25°C to -55°C	≤85°C	≤125°C	Unit
fmax	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	165 33 28	205 41 35	250 50 43	ns
<sup>†</sup> PHL	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0 4.5 6.0	165 33 28	205 41 35	250 50 43	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance		10	10	10	pF

For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
 Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	35	pF

TIMING REQUIREMENTS (Input tr=tf=6 ns)

		Vcc	Guaranteed Limit			
Symbol	Parameter MARSAIG GLOCH GROWANG		25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Data to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Clock to Data (Figure 3)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
trec	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t <sub>W</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>W</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

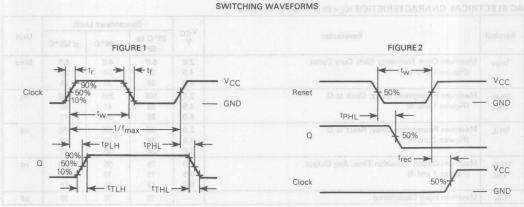
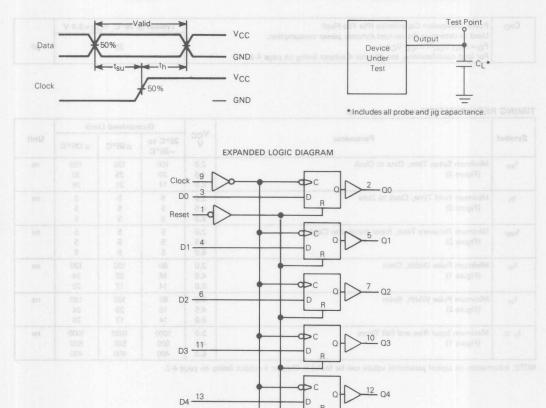


FIGURE 3

FIGURE 4 - TEST CIRCUIT



D5 14

# Quad D Flip-Flop with Common Clock and Reset

## **High-Performance Silicon-Gate CMOS**

The MC54/74HC175 is identical in pinout to the LS175. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of four D flip-flops with common Reset and Clock inputs, and separate D inputs. Reset (active-low) is asynchronous and occurs when a low level is applied to the Reset input. Information at a D input is transferred to the corresponding Q output on the next positive-going edge of the Clock input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 166 FETs or 41.5 Equivalent Gates

## MC54/74HC175



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



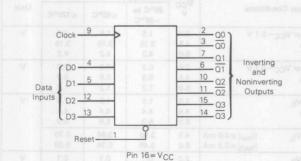
D SUFFIX SOIC CASE 751

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.





Pin 8 = GND

### PIN ASSIGNMENT

Reset [	1 •	16	Vcc
00 [	2	15	Q3
00	3	14 0	Q3
D0 [	4	130	D3
D1 [	5	12	D2
Q1 C	6	110	Q2
Q1 [	7	10	Q2
GND C	8	90	Clock

#### **FUNCTION TABLE**

Inputs			Outputs		
Reset	Clock	D	Q	Q	
L	X	X	IO C	Н	
Н	_	Н	H	L	
Н		- L	L	Н	
H L X			no ch	ange	

	8	8		
Ŀ	6	c	ч	
P	-6	9	3	
86.	37	3		

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, VCC and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq \mathsf{VCC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced	to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1) V	CC = 2.0 V CC = 4.5 V CC = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	RM EBOD			MARI	Gua	ranteed Li	imit	
Symbol	Parameter	Test Conditions		V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> -  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V	
VIL	Maximum Low-Level Input Voltage		-0.1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	1 (sp. 4)	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
enron	Ingots 0	Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
H egnerio	3 1 7 m on X 1 R	Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	± 0.1	± 1.0	± 1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA		6.0	8	80	160	μΑ

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

<sup>†</sup>Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

## MC54/74HC175

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

		v <sub>CC</sub>	Gua				
Symbol	Parameter		25°C to -55°C	≤85°C	≤125°C	Unit	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	35V +	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to Q or $\overline{\mathbf{Q}}$ (Figures 1 and 4)	ама -	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
<sup>†</sup> PHL	Maximum Propagation Delay, Reset to Q or $\overline{\mathbf{Q}}$ (Figures 2 and 4)		2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)		2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance		-	10	10	10	pF

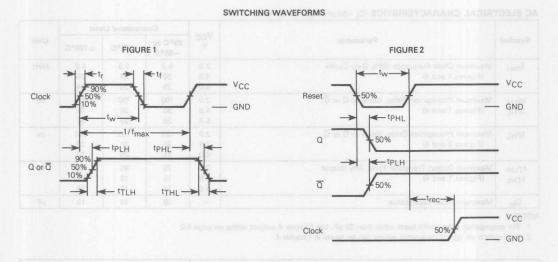
## NOTES

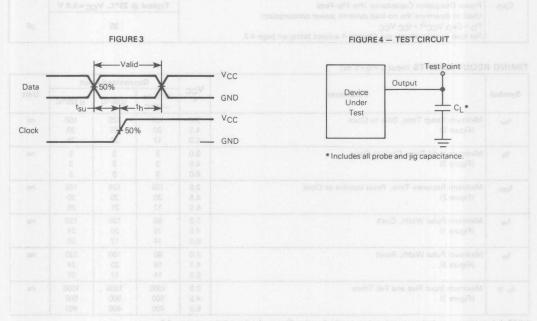
- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

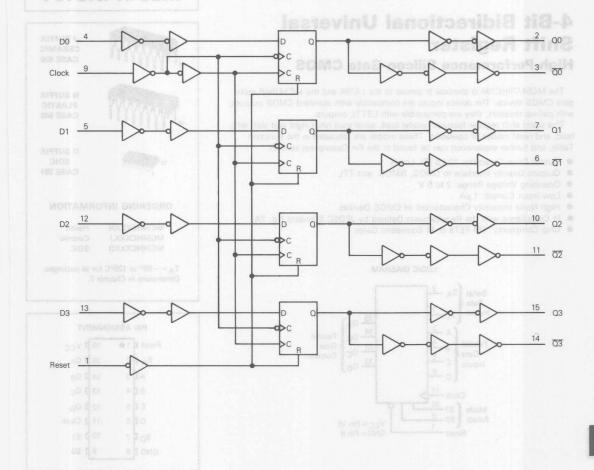
CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	35	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	ganting	

## TIMING REQUIREMENTS (Input t<sub>e</sub> = t<sub>f</sub> = 6 ms)

	tugio0			Gua	mit		
Symbol	Parameter		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Data to Clock (Figure 3)	GN9 20V	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Clock to Data (Figure 3)		2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)		2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>W</sub>	Minimum Pulse Width, Clock (Figure 1)		2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 2)		2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)		2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns







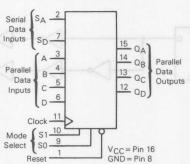
## **High-Performance Silicon-Gate CMOS**

The MC54/74HC194 is identical in pinout to the LS194 and the MC14194B metal gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

This static shift register features parallel load, serial load (shift right and shift left), hold, and reset modes of operation. These modes are tabulated in the Function Table, and further explanation can be found in the Pin Description section.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 164 FETs or 41 Equivalent Gates

## LOGIC DIAGRAM



## 16

J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

## ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

## PIN ASSIGNMENT

Reset	1 •	16	I VCC
SAC	2	15	I QA
AD	3	14	Q <sub>B</sub>
в	4	13	1 QC
C C	5	12	I QD
DC	6	.11	Clock
s <sub>D</sub> I	7	10	l S1
GND C	8	9	S0

## **FUNCTION TABLE**

				Inputs							Out			
		ode lect		1000	erial ata			alle ata	1					Operating
Reset	S1	S0	Clock	SD	SA	A	В	С	D	QA	QB	QC	$Q_D$	Mode
L	X	X	X	X	X	X	X	X	X	L	L	L	L	Reset
Н	Н	Н	5	X	X	а	b	С	d	а	b	С	d	Parallel Load
Н	L	Н	_	X	Н	X	X	X	X	Н	QAn	QBn	Qcn	Shift Right
Н	L	Н	5	X	L	X	X	X	X	L	QAn		QCn	
Н	Н	L	5	Н	X	X	X	X	X	QBn	QCn	QDn	Н	Shift Left
Н	Н	L	5	L	Χ	X	X	X	X	QBn	QCn	QDn	L	
Н	L	L	X	X	X	X	X	X	X		no cl	nange		Hold
Н	X	X	L	X	X	X	X	X	X			nange		
Н	X	X	Н	X	X	X	X	X	X		no cl	hange		

H = high level (steady state) L = low level (steady state)

X = don't care

 $\mathcal{L}$  = transition from low to high level.

 a, b, c, d= the level of steady-state input at inputs A, B, C, or D, respectively.

Q<sub>An</sub>, Q<sub>Bn</sub>, Q<sub>Cn</sub>, Q<sub>Dn</sub>= the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, or Q<sub>D</sub>, respectively, before the most-recent ✓ transition of the clock.

outputs must be left open.

fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance

## MC54/74HC194

## **MAXIMUM RATINGS\***

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	٧
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GN	2.0	6.0	V	
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Re	ferenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package T	ypes	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	100 126 190	2.0		Gua	aranteed Li	imit	Unit
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Vон	Minimum High-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
ngar	80 100 120 16 20 24	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
20	14 17 20	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Curren	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μΑ

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_f = t_f = 6 \text{ ns}$ )

	The device contains					Gua	mit	Symbo	
Symbol	niega trisug of yoturas againer state right or outs	Parameter			VCC	25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (5 (Figures 1 and 4)	0% Duty Cycle)	00 V or 8.0 — 00 k		2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay, (Figures 1 and 4)	Clock to Q	2.50 2.50 780	19Id sensi	2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	ns
tPHL	Maximum Propagation Delay, (Figures 2 and 4)		000 1 + 10+80 +	Photograph	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition 1 (Figures 1 and 4)	ime, Any Output	ORC	Coestue 9 2 PRO cimes	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	anni	Stano Y animos	nii Distribution	boot Turk	10	10	10	pF

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
   Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	-
	Used to determine the no-load dynamic power consumption:		SUILOU
	PD = CPD VCC2f + ICC VCC mild mild	potential 90	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	190 Supplied Validate (References) 2001	and -

## TIMING REQUIREMENTS (Input $t_f = t_f = 6 \text{ ns}$ )

	en 0007 0 V 0.S=20V	.,	Gua	at at		
Symbol	Parameter 000 V 8 A 9 00 V	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Parallel Data Inputs to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>su</sub>	Minimum Setup Time, S1 to S0 to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>su</sub>	Minimum Setup Time, S <sub>A</sub> or S <sub>D</sub> to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Clock to any Input (except Reset) (Figure 3)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
trec	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
tw	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>W</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
Au	101 00 00 00 00 00 00 00 00 00 00 00 00	6.0	400	400	400	ne

## PIN DESCRIPTIONS

## DATA INPUTS

A, B, C, D (PINS 3, 4, 5, 6) — Parallel data inputs.

SA (PIN 2) — Serial-data input when using shift-right mode. SD (PIN 7) — Serial-data input when using shift-left mode.

## **OUTPUTS**

 $\mathbf{Q_A},\,\mathbf{Q_B},\,\mathbf{Q_C},\,\mathbf{Q_D}$  (PINS 15, 14, 13, 12) — Parallel data outputs.

## CONTROL INPUTS

CLOCK (PIN 11) — Clock Input. The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

RESET (PIN 1) — A low level applied to this pin resets all stages and forces all outputs low.

S0, S1 (PINS 9, 10) — Mode-select inputs. These inputs control the mode of operation as described in the function table and below.

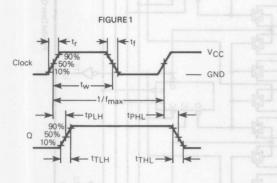
Parallel Load Mode (S1 = H, S0 = H) — Data is loaded into the device with a positive transition of the Clock input.

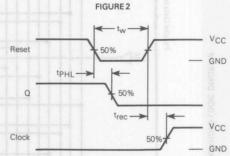
Shift Right Mode (S1=L, S0=H) — With a positive transition of the Clock input, each bit is shifted right (in the direction  $Q_A$  toward  $Q_D$ ) one stage and data on the  $S_A$  Serial Data Input is shifted into stage A.

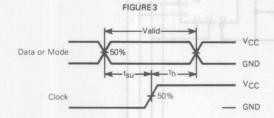
Shift Left Mode (S1=H, S0=L) — With a positive transition of the Clock input, each bit is shifted left (in the direction Q<sub>D</sub> toward Q<sub>A</sub>) one stage and data on the S<sub>D</sub> Serial Data Input is shifted into stage D.

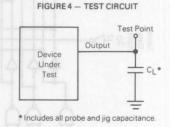
Hold Mode (S1 = L, S0 = L) - Outputs are held.

## SWITCHING WAVEFORMS



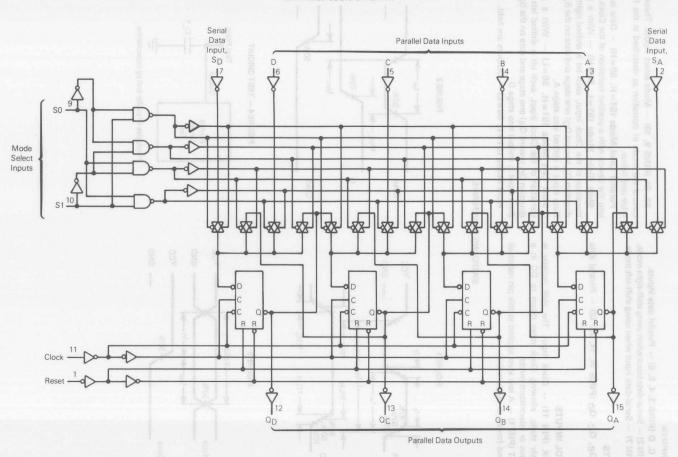




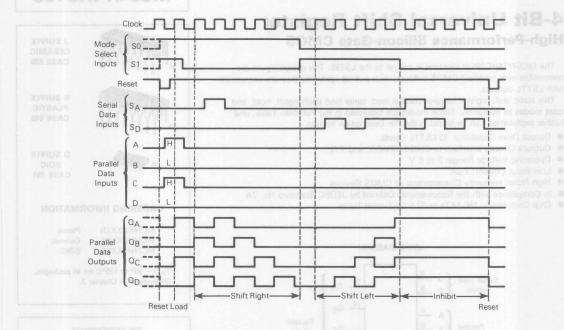


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## EXPANDED LOGIC DIAGRAM







## 4-Bit Universal Shift Register High-Performance Silicon-Gate CMOS

The MC54/74HC195 is identical in pinout to the LS195. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

This static shift register features parallel load, serial load (shift right), hold, and reset modes of operation. These modes are tabulated in the Function Table, and further explanation can be found in the Pin Description section.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 150 FETs or 37.5 Equivalent Gates

## LOGIC DIAGRAM Serial Data QA Inputs 14 QB Parallel Parallel QC Data Outputs Inputs 12 QD 11 $\overline{Q}_D$ Clock Serial Shift/ Parallel Load Reset Pin 16 = VCC Pin 8 = GND

## MC54/74HC195



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

## ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

## PIN ASSIGNMENT

Reset I	1 •	16	v <sub>cc</sub>
J	2	15	Q <sub>A</sub>
KI	3	14	O <sub>B</sub>
AI	4	13	a oc
В [	5	12	αD
CI	6	11	αD
DI	7	10	Clock
GND [	8	9	Serial Shift/

## **FUNCTION TABLE**

Inputs								Outputs								
	Shift/ Serial Parallel		Serial Parallel		Serial											
Reset	Load	Clock	J	K	A	В	С	D	QA	QB	QC	QD	$\overline{a}_D$	Operating Mode		
L	X	×	X	X	X	X	X	X	L	L	L	L	Н	Reset		
Н	L		X	X	a	b	С	d	а	b	С	d	d	Parallel Load		
Н	Н	L	X	X	X	X	X	X		n	o chan	ge		Hold		
Н	Н		L	Н	X	X	X	X	QAO	QAO	QBn	Qcn	QCn	Retain First Stage	Serial	
Н	Н		L	L	X	X	X	X	L	QAn	QBn	QCn	Q <sub>Cn</sub>	Reset First Stage	Shift	
Н	Н		Н	Н	X	X	X	X	Н	QAn	QBn	QCn	QCn	Set First Stage		
Н	Н		Н	L	X	X	X	X	QAn	QAn	QBn	QCn	QCn.	Toggle First Stage		

H = high level (steady state) L = low level (steady state)

X = don't care

= transition from low to high level a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively. Q<sub>AO</sub>= the level of Q<sub>A</sub> before the indicated steady-state input conditions were established.

Q<sub>An</sub>, Q<sub>Bn</sub>, Q<sub>Cn</sub>= the level of Q<sub>A</sub>, Q<sub>B</sub>, or Q<sub>C</sub>, respectively, before the most-recent ✓ transition of the clock

circuitry to guard against damage due to high static voltages or electric fields. However, precautions must

## MAXIMUM RATINGS\*

		ACCUSE AND INVESTIGATION AND INC.	147 1414
Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	oC lose, Any

MC54/74HC195

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
Vcc	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Refere	enced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Type	es	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V	0	1000 500	ns
	0 25°C to 5°08'z 5°C	V <sub>CC</sub> = 6.0 V	0	400	

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	75 TS	0.0	Vcc	Gua	aranteed Li	imit	
Symbol	Parameter	Test Conditions		25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	Vin=VIH or VIL  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
	80 100 120 18 20 24	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
	17 20	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	± 1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	Vin = VCC or GND Iout = 0 µA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	repullov sligte right of sub.  V d.1 = 20V or 8.1 =	-	V	25°C to -55°C	≤85°C	≤125°C	Unit
fmax	Maximum Clock Frequency (50% Duty Cycle)		2.0	6.0	4.8	4.0	MHz
	(Figures 1 and 5)		4.5	30	24	20	
	official of antistics		6.0	35	28	24	
tPLH,	Maximum Propagation Delay, Clock to any Q or QD		2.0	145	180	220	ns
1 -1 1	(Figures 1 and 5)		4.5	29	36	44	
	150 Year Win Cargo GND SVI Votes	1910 pines	6.0	25	31	38	
tPLH,	Maximum Propagation Delay, Reset to any Q or QD	Tagaaati (	2.0	150	190	225	ns
tPHL	(Figures 2 and 5)		4.5	30	38	45	
gauno -	DQV so OND vadne . p.84	Seconds	6.0	26	33	38	
tTLH,	Maximum Output Transition Time, Any Output	( Pumoget	2.0	75	95	110	ns
†THL	(Figures 1 and 5)	ramic SIPS	4.5	15	19	22	
	augra-apper anialsh arth of ass			13	16	19	Salirola e
Cin	Maximum Input Capacitance	O liebuacom	000 <del>2</del> 19	10	10	10	pF

## NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	MODER
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	95	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	QC Supply Voltage (Baterapped a	noV.

## TIMING REQUIREMENTS (Input $t_f = t_f = 6$ ns)

	av 1000 0 100 Av 1000		Gua	15 15		
Symbol	Parameter CON CONTROL OF THE PARAMETER CONTROL	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, A, B, C, D, J, or K to Clock	2.0	100	125	150	ns
	(Figure 3)	4.5	20	25	30	BLEC
		6.0	17	21	26	
t <sub>su</sub>	Minimum Setup Time, Serial Shift/Parallel Load to Clock	2.0	100	125	150	ns
	(Figure 4)	4.5	20	25	30	10000
	0.98	6.0	17	21	26	
th	Minimum Hold Time, Clock to A, B, C, D, J, or K	2.0	3	3	3	ns
	(Figure 3)	4.5	3	3	3	10
	6.0 4.2 4.2 6.2	6.0	3	3	3	
th Mi	Minimum Hold Time, Clock to Serial Shift/Parallel Load	2.0	3	3	3	ns
	(Figure 4)	4.5	3	3	3	
	5.0 1.2 1.2 1.2	6.0	3	3	3	
trec	Minimum Recovery Time, Reset Inactive to Clock	2.0	5	5	5	ns
100	(Figure 2)	4.5	5	5	5	
	60 6.0 6.0 5.0	6.0	5	5	5	13.50
tw	Minimum Pulse Width, Clock	2.0	80	100	120	ns
	(Figure 1)	4.5	16	20	24	
	1.0 1.0 0.1 0.1 0.1 0.1	6.0	14	17	20	30V
tw	Minimum Pulse Width, Reset	2.0	80	100	120	ns
	(Figure 2)	4.5	16	20	24	
	1 of Vit (1 of V	6.0	14	17	20	
tr, tf	Maximum Input Rise and Fall Times	2.0	1000	1000	1000	ns
Au	(Figure 1) 0.12 4.82 8.8	4.5	500	500	500	
	A31 00 B AA 0000 mm	6.0	400	400	400	

## **DATA INPUTS**

A, B, C, D (PINS 4, 5, 6, 7) - Parallel data inputs.

## **OUTPUTS**

 $\mathbf{Q_A},\mathbf{Q_B},\mathbf{Q_C},\mathbf{Q_D},\overline{\mathbf{Q}_D}$  (PINS 15, 14, 13, 12, 11) — Parallel data outputs.

## **CONTROL INPUTS**

**CLOCK (PIN 10)** — Clock input. The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

SERIAL SHIFT/PARALLEL LOAD (PIN 9) — Shift or load control. A low level applied to this pin allows data to be loaded from the parallel inputs. Data is loaded with the positive transition of the Clock input. A high level allows data to be shifted in the manner dictated by the J and  $\overline{K}$  control inputs.

RESET (PIN 1) — A low level applied to this pin resets all stages and forces all outputs low.

J,  $\overline{K}$  (PINS 2, 3) — Shift Control. With Serial Shift/Parallel Load high, J and  $\overline{K}$  control the mode of operation, as illustrated in the Function Table.

J = L,  $\overline{K} = H$  — With a positive transition of the Clock input, each bit is shifted to the right (in the direction  $Q_A$  toward  $Q_D$ ) one stage and stage A maintains its previous state.

J=H,  $\overline{K}=L$  — With a positive transition of the Clock input, each bit is shifted right (in the direction of  $Q_A$  toward  $Q_D$ ) one stage and the  $Q_A$  output is inverted.

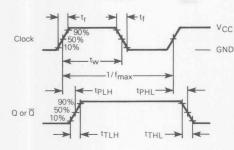
 $J = \overline{K} = L$  — With a positive transition of the Clock input, each bit is shifted right (in the direction  $\Omega_A$  toward  $\Omega_D$ ) one stage and a low is loaded into stage A.

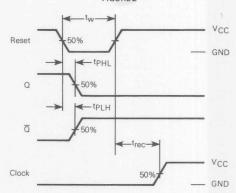
 $J = \overline{K} = H$  — With a positive transition of the Clock input, each bit is shifted right (in the direction  $Q_A$  toward  $Q_D$ ) one stage and a high is loaded into stage A.

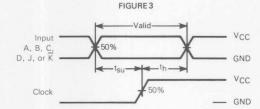
## SWITCHING WAVEFORMS

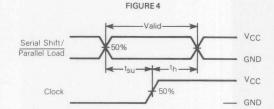
FIGURE 1

FIGURE 2

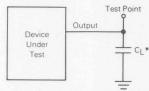




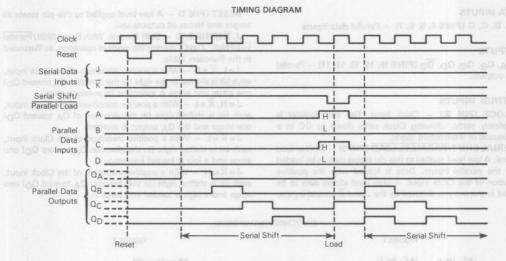




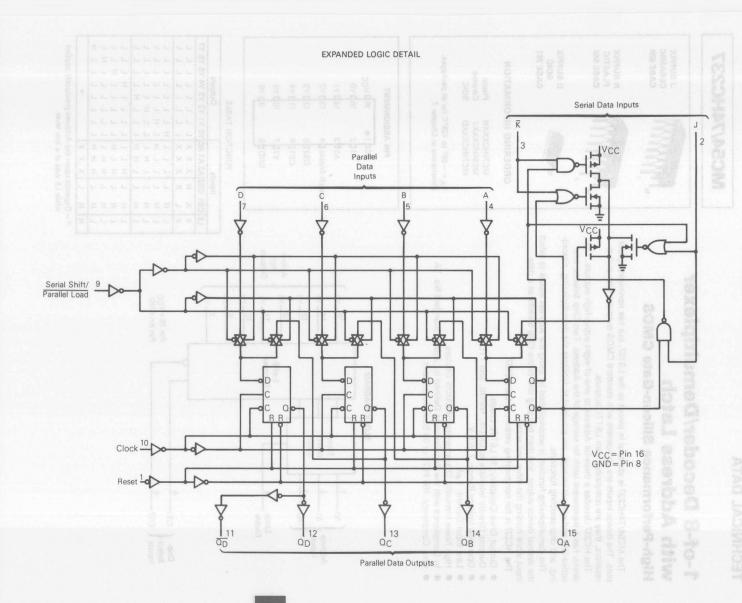
## FIGURE 5 - TEST CIRCUIT



\* Includes all probe and jig capacitance.



5-213



## 1-of-8 Decoder/Demultiplexer with Address Latch High-Performance Silicon-Gate CMOS

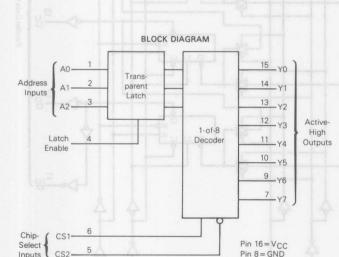
The MC54/74HC237 is identical in pinout to the LS137, but has noninverting outputs. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC237 decodes a three-bit Address to one-of-eight active-high outputs. The device has a transparent latch for storage of the Address. Two Chip Selects, one active-low and one active-high, are provided to facilitate the demultiplexing, cascading, and chip-selecting functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the other one active.

The HC237 is the noninverting version of the HC137.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 156 FETs or 39 Equivalent Gates



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

## ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

## PIN ASSIGNMENT

A0	1 •	16 V <sub>CC</sub>
A10	2	15 Y0
A2 🛚	3	14 1 Y1
Latch Enable	4	13 Y2
CS2	5	12 73
CS1	6	11 <b>1</b> Y4
Y7 🖸	7	10 Y5
GND	8	9 <b>1</b> Y6

## **FUNCTION TABLE**

		Inpu	ts					(	Out	put	S		
LE	CS1	CS2	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Х	X	Н	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	Н	L	L	L	L	Н	L	L	L	L	L	L	L
L	Н	L	L	L	Н	L	Н	L	L	L	L	L	L
L	Н	L	L	Н	L	L	L	H	L	L	L	L	L
L	Н	L	L	Н	Н	L	L	L	Н	L	L	L	L
L	Н	L	Н	L	L	L	L	L	L	Н	L	L	L
L	Н	L	Н	L	Н	L	L	L	L	L	Н	L	L
L	Н	L	Н	H	L	L	L	L	L	L	L	Н	L
L	Н	L	Н	Н	Н	L	L	L	L	L	L	L	Н
Н	Н	L	X	X	X				- 1	4			

<sup>\* =</sup> Depends upon the Address previously applied while LE was at a low level.

## 5

## **MAXIMUM RATINGS\***

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Paramet	er	Min	Max	Unit
VCC	DC Supply Voltage (Referenced	to GND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage	C Input Voltage, Output Voltage (Referenced to GND)			
TA	Operating Temperature, All Pack	- 55	+ 125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 2)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

		named in Citapuer 6.	10 100	Guaranteed Limit			molni . S
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>  ≤20 μA		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	180 180	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	ne <sub>1</sub>
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	61 11 6	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	±1.0	μΑ
ICC	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_f = t_f = 6 \text{ ns}$ )

	This divide contents	Volun Unic				Guaranteed Limit			ice my R	
Symbol	che to high static volcage	Parameter 1997 1997 1997 1997 1997 1997 1997 199		VCC	25°C to -55°C	≤85°C	≤125°C	Unit		
tPLH	Maximum Propagation Delay,	Input A to O	utput Y	or 8.8		2.0	235	295	355	ns
terlan emine	(Figures 1 and 6)					4.5	47	59	71	
crisbagin	voluments to that highli-					6.0	40	50	60	
tPHL	circuit. Fer proper operation					2.0	185	230	280	
	V <sub>ost</sub> should be constrain					4.5	37	46	56	
DOY 2	range GND stivin or Vige	Wens	- 08	5	THIC since	6.0	31	39	48	03
tPLH	Maximum Propagation Delay,	CS2 to Outp	ut Y			2.0	200	250	300	ns
seepall (	(Figures 2 and 6)					4.5	40	50	60	
	ago shall ad stome standard					6.0	34	43	51	
tPHL	Manager of Secret Building					2.0	145	180	220	
						4.5	29	36	44	
						6.0	25	31	38	
tPLH	Maximum Propagation Delay,	CS1 to Outp	ut Y	O nion	ragio bahawam	2.0	200	250	300	ns
	(Figures 3 and 6)					4.5	40	50	60	
						6.0	34	43	51	
tPHL						2.0	160	200	240	
						4.5	32	40	48	
						6.0	27	34	41	
tPLH	Maximum Propagation Delay,	Latch Enable	to Outp	ut Y		2.0	250	315	375	ns
	(Figures 4 and 6)					4.5	50	63	75	
						6.0	43	54	64	lodmy
tPHL						2.0	190	240	285	
						4.5	38	48	57	Resolveni
						6.0	32	41	48	AT
tTLH,	Maximum Output Transition 7	Time, Any Ou	tput		V D.S = gr.V	2.0	75	95	110	ns
tTHL	(Figures 2 and 6)					4.5	15	19	22	1
			400	6		6.0	13	16	19	-
Cin	Maximum Input Capacitance		STATE OF THE PARTY	75		-	10	10	10	pF

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

  2. Information on typical parametric values can be found in Chapter 4.

 Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	100	pF

## TIMING REQUIREMENTS (Input $t_f = t_f = 6$ ns)

	E.I. E.I E.I 1.9 1.9	V. W	Gua	HOV		
Symbol	Parameter A4.0	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Input A to Latch Enable (Figure 5)	2.0	100 20	125 25	150 30	ns
V.	1.0 0.1 0.1 0.1 0.1 0.1	6.0	17	21	26	
th	Minimum Hold Time, Latch Enable to Input A (Figure 5)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
tw	Minimum Pulse Width, Latch Enable (Figure 4)	2.0	80 16	100	120 24	ns
Au	061 08 8 0.0 (MD:seg	6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 2)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

## PIN DESCRIPTIONS

## **ADDRESS INPUTS**

A0, A1, A2 (PINS 1, 2, 3) — Address inputs. These inputs, when the chip is enabled, determine which of the eight outputs is selected.

## **CONTROL INPUTS**

CS1, CS2 (PINS 6, 5) — Chip select inputs. For CS1 at a high level and CS2 at a low level, the chip is enabled and the outputs follow the data inputs (Latch Enable = L). For any other combination of CS1 and CS2, the outputs are at a low level.

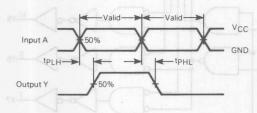
**LATCH ENABLE (PIN 4)** — Latch Enable input. A high level at this input latches the Address. A low level at this input allows the outputs to follow the Address (CS1 = H and CS2 = L).

## **OUTPUTS**

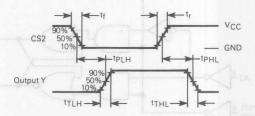
Y0-Y7 (PINS 15, 14, 13, 12, 11, 10, 9, 7) — Active-high outputs. One of these eight outputs is selected when the chip is enabled (CS1=H and CS2=L) and the Address inputs correspond to that particular output. The selected output is at a high level while all others remain at a low level.

## SWITCHING WAVEFORMS

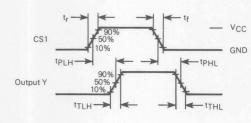
## FIGURE 1



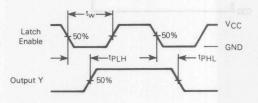
## FIGURE 2



## FIGURE 3



## FIGURE 4



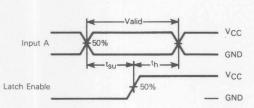


FIGURE 5

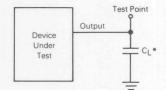
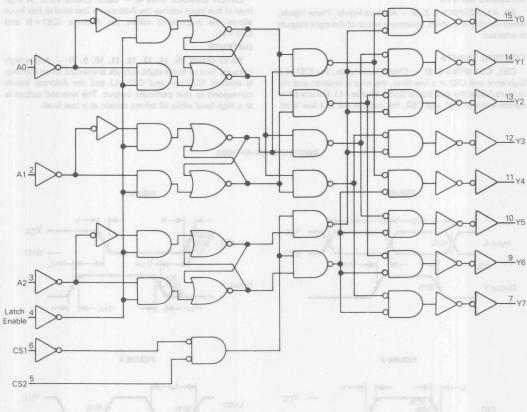


FIGURE 6 - TEST CIRCUIT

\* Includes all probe and jig capacitance.



## Octal 3-State Inverting Buffer/ Line Driver/Line Receiver High-Performance Silicon-Gate CMOS

The MC54/74HC240 is identical in pinout to the LS240. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal inverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has inverting outputs and two active-low output enables.

The HC240 is similar in function to the HC241 and HC244.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 120 FETs or 30 Equivalent Gates

## MC54/74HC240



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



DW SUFFIX SOIC CASE 751D

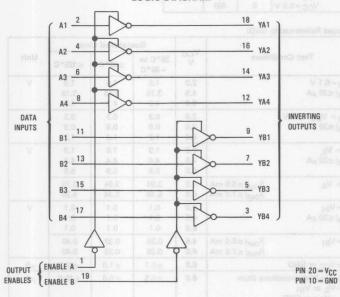
## **ORDERING INFORMATION**

MC74HCXXXN PI MC54HCXXXJ C MC74HCXXXDW S

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

## LOGIC DIAGRAM



## PIN ASSIGNMENT

	71001		
ENABLE A	1 •	20	1 v <sub>CC</sub>
A1 [	2	19	ENABLE E
YB4 [	3	18	] YA1
A2 [	4	17	]B4
YB3 [	5	16	YA2
A3 [	6	15	] B3
YB2	7	14	TYA3
A4 [	8	13	] B2
YB1 [	9	12	YA4
GND [	10	11	]B1
	-	-	

## **FUNCTION TABLE**

Input	YA, YB  H L Z		
Enable A, Enable B	A, B	YA, YB	
L	L	Н	
Mary Land	Н	Lnd	
nera H	X	Z	

J

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GNI	0)	2.0	6.0	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Refe	erenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types			+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> =2.0 V	0	1000	ns
	(Figure 1)	V <sub>CC</sub> =4.5 V	0	500	
	PRINCESS PROTE	V <sub>CC</sub> =6.0 V	0	400	

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	2 2 2 2 2 2	nev 01			Gua	aranteed L	imit	
Symbol	Parameter	Test Con	ditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V  l <sub>out</sub>  ≤20 μA	MY SI	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤20 μA	iar ii ox	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	AV.g STUPAN
Voн	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	587 <sup>7</sup> 782	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
	V <sub>in</sub> = \	V <sub>in</sub> = V <sub>IL</sub>	$ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub>  I <sub>out</sub>  ≤20 μA	yar f	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
IA, VB	Enable E	Vin=VIH	I <sub>out</sub>   ≤6.0 mA  I <sub>out</sub>   ≤7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  Vin = VIL or VIH  Vout = VCC or GND		6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	8	80	160	μΑ

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

			Gua	aranteed Li	imit	
Symbol	Parameter Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns OH 40 elden3
tPZL, tPZH	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	-	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	10 HIS IN	15	15	15	pF

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	32 ATA3	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	TOTAL	

## **SWITCHING WAVEFORMS**

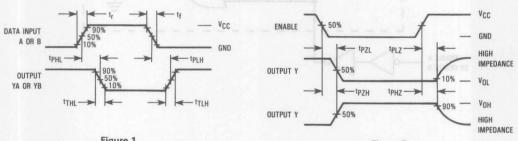


Figure 1

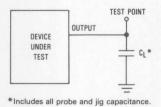
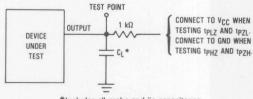


Figure 3. Test Circuit

Figure 2



\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

## **INPUTS**

A1, A2, A3, A4, B1, B2, B3, B4 (Pins 2, 4, 6, 8, 11, 13, 15, 17) — Data input pins. Data on these pins appear in inverted form on the corresponding Y outputs, when the outputs are enabled.

## CONTROLS

Enable A, Enable B (Pins 1, 19) — Output enables (active-low). When a low level is applied to these pins, the outputs

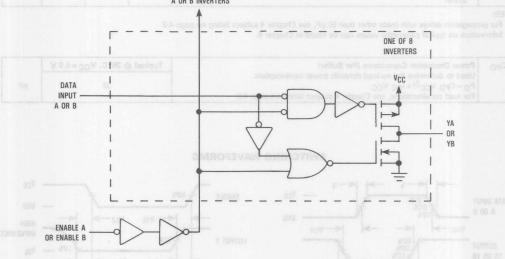
are enabled and the devices function as inverters. When a high level is applied, the outputs assume the high-impedance

## OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (Pins 18, 16, 14, 12, 9, 7, 5, 3) — Device outputs. Depending upon the state of the output-enable pins, these outputs are either inverting outputs or high-impedance outputs.

## LOGIC DETAIL

TO THREE OTHER
A OR B INVERTERS



## Octal 3-State Inverting Buffer/ Line Driver/Line Receiver with **LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS**

The HCT240 is identical in pinout to the LS240. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT240 is an octal inverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has inverting outputs and two active-low output enables.

The HCT240 is the inverting version of the HCT244. See also HCT241.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 110 FETs or 27.5 Equivalent Gates

## MC54/74HCT240



J SUFFIX CERAMIC **CASE 732** 



N SUFFIX PLASTIC **CASE 738** 



DW SUFFIX SOIC CASE 751D

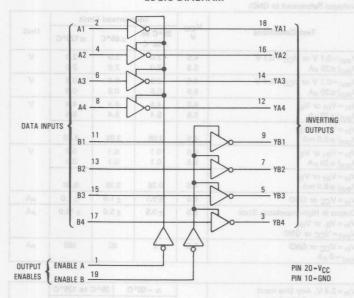
## ORDERING INFORMATION

MC74HCTXXXN MC54HCTXXXJ MC74HCTXXXDW SOIC

Plastic Ceramic

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

## LOGIC DIAGRAM



## PIN ASSIGNMENT

ENABLE A	10	20	□ VCC
A1 🗆	2	19	I ENABLE B
YB4	3	18	YA1
A2 □	4	17	□ B4
YB3 □	5	16	□ YA2
A3 🗆	6	15	□ B3
YB2 🗆	7	14	□ YA3
A4 🗆	8	13	□ B2
YB1 🗆	9	12	TYA4
GND 🗆	10	11	□ B1

## **FUNCTION TABLE**

Input	Outputs	
Enable A, Enable B	А, В	YA, YB
L	L	н
Figure 4	Н	LO
H	X	MZ

Z = High Impedance X = Don't Care

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	٧
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	٧
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL WG WG	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
tr, tf	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	C 81 C DARY	91	.,	Guaranteed Limit			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	٧
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	0.8	0.8 0.8	0.8	٧
VOH	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	٧
	FUNCTION TA	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	BO ATAO
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
gy .	Y S A S eldnes	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0$ mA	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	5.5	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  Vin = VIL or VIH  Vout = VCC or GND	5.5	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 µA	5.5	8	80	160	μΑ

ΔICC	Additional Quiescent Supply	Vin=2.4 V, Any One Input		≥ -55°C	25°C to 125°C	-11
	Current	$V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0 \mu A$	5.5	2.9	2.4	mA

## NOTES:

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

<sup>†</sup>Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

tPHL	(Figures 1 and 3)				
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	30	38	45	ns
tPZL,	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	30	38	45	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
Cin	Maximum Input Capacitance	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

Symbol

2. Information on typical parametric values can be found in Chapter 4.

tpLH, Maximum Propagation Delay, A to YA or B to YB

AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

Parameter

CPD	Power Dissipation Capacitance (Per Enabled Output)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	8 3 18 A 18 A 3 18 A 3	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

## **SWITCHING WAVEFORMS**

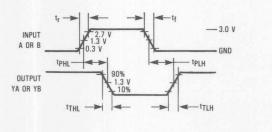
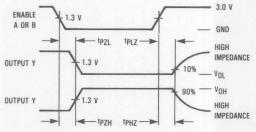


Figure 1



**Guaranteed Limit** 

≤85°C

28

25°C to

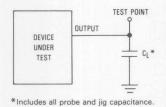
-55°C

22

Unit

≤125°C

Figure 2



TEST POINT CONNECT TO VCC WHEN 1 kΩ OUTPUT TESTING tPLZ AND tPZL.
CONNECT TO GND WHEN
TESTING tPHZ AND tPZH. DEVICE UNDER CL\* TEST

\*Includes all probe and jig capacitance.

Figure 3. Test Circuit

Figure 4. Test Circuit

SUPPORT F 1.3 V 1003 SON WORLDANCE HOOM NAMED AND SON WORLDANCE HOOM NAMED

Figure 1

# Octal 3-State Noninverting Buffer/Line Driver/Line Receiver

## **High-Performance Silicon-Gate CMOS**

The MC54/74HC241 is identical in pinout to the LS241. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has noninverted outputs and two output enables. Enable A is active-low and Enable B is active-high.

The HC241 is similar in function to the HC244 and HC240.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates

## MC54/74HC241



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



DW SUFFIX SOIC CASE 751D

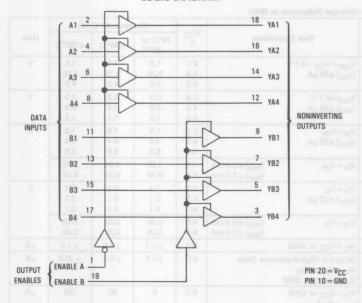
## ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXDW

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

## LOGIC DIAGRAM



## PIN ASSIGNMENT

	710011	3141415	
ENABLE A	1.0	20	1vcc
A1 [	2	19	ENABLE
YB4 [	3	18	YA1
A2 [	4	17	] B4
YB3 [	5	16	YA2
A3 [	6	15	] B3
YB2	7	14	YA3
A4 [	8	13	] B2
YB1 [	9	12	YA4
GND [	10	11	] B10 V

FUNCTION TABLE								
Inputs		ts Output I		s	Output			
Enable A	A	YA	Enable B	В	YB			
L	L	L	Н	L	L			
L	Н	Н	Н	Н	Н			
Н	X	Z	L	X	Z			

Z = high impedance

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq (V_{in}$  or  $V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	CE AND DONE	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	ed to GND)	0	Vcc	٧
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	1			.,	Gua	aranteed L	imit	
Symbol	Parameter	Test Co	nditions	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =V <sub>CC</sub> -0.1 V  I <sub>out</sub>  ≤20 μA	EAY AT	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V  I <sub>out</sub>  ≤20 μA	say S?	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	- V
Voн	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub>  I <sub>out</sub>  ≤20 μA	18Y	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V <sub>in</sub> =V <sub>IH</sub>	I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{\text{in}} = V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	EN -	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
8 "	S AY A oldenii	V <sub>in</sub> = V <sub>IL</sub>	I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	± 1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Imp Vin = VIL or VIH Vout = VCC or GND		6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$		6.0	8	80	160	μΑ

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

			Gu			
Symbol	Parameter stable to the property of the proper	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns DATAO
tPZL, tPZH	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	-	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High-Impedance State)	-	15	15	15	pF

## NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

\*Includes all probe and jig capacitance.

Figure 3. Test Circuit

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC	34	nF
	For load considerations, see Chapter 4 subject listing on page 4-2.		709

## **SWITCHING WAVEFORMS** VCC ENABLE A VCC DATA INPUT GND A OR B GND ← tPHL ENABLE B 50% GND OUTPUT YA OR YB - tpzL tpLZ -> HIGH **IMPEDANCE** OUTPUT Y 10% -tPZH tPHZ → VOH 90% Figure 1 **OUTPUT Y** 50% HIGH IMPEDANCE Figure 2 TEST POINT TEST POINT CONNECT TO VCC WHEN OUTPUT TESTING tPLZ AND tPZL. CONNECT TO GND WHEN OUTPUT DEVICE DEVICE UNDER UNDER TESTING THE AND THE TEST TEST

5

MOTOROLA HIGH-SPEED CMOS LOGIC DATA

\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

A1, A2, A3, A4, B1, B2, B3, B4 (PINS 2, 4, 6, 8, 11, 13, 15, 17) — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs when the outputs are enabled.

## CONTROLS

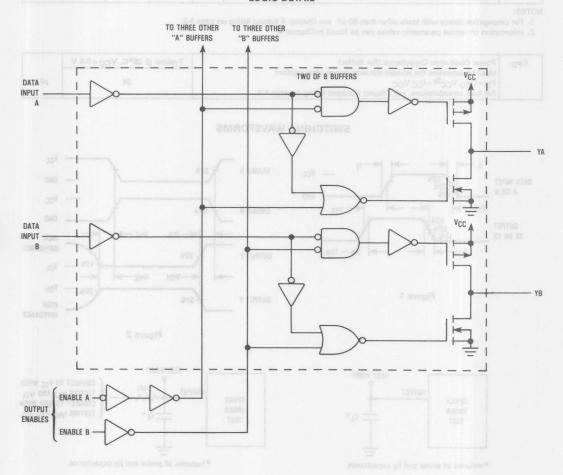
Enable A (PIN 1) — Output enable (active-low). When a low level is applied to this pin, the outputs of the "A" devices are enabled and the devices function as noninverting buffers. When a high level is applied, the outputs assume the high-impedance state.

Enable B (PIN 19) — Output enable (active-high). When a high level is applied to this pin, the outputs of the "B" devices are enabled and the devices function as noninverting buffers. When a low level is applied, the outputs assume the high-impedance state.

## **OUTPUTS**

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (PINS 18, 16, 14, 12, 9, 7, 5, 3) — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high-impedance outputs.

## LOGIC DETAIL



# Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The HCT241 is identical in pinout to the LS241. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT241 is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has non-inverted outputs and two output enables. Enable A is active-low and Enable B is active-high.

The HCT241 is similar in function to the HCT244. See also HCT240.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 118 FETs or 29.5 Equivalent Gates

## MC54/74HCT241



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



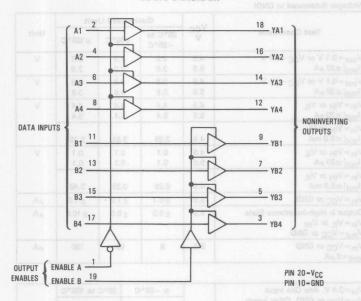
DW SUFFIX SOIC CASE 751D

## ORDERING INFORMATION

MC74HCTXXXN MC54HCTXXXJ MC74HCTXXXDW Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

## LOGIC DIAGRAM



## PIN ASSIGNMENT

ENABLE A	10	20	□. ACC
A1 🗆	2	19	ENABLE B
YB4 □	3	18	YA1
A2 □	4	17	□ B4
YB3 🗆	5	16	YA2
A3 🗆	6	15	□ B3
YB2 🗆	7	14	TYA3
A4 🗆	8	13	□ B2
YB1 □	9	12	TYA4
GND 🗆	10	11	□ B1

## **FUNCTION TABLE**

Inputs		Output
Enable A	Α	YA
L	L	L
L	Н	H
H Tech	X	Z
Inputs		Output
Enable B	В	YB
Calesophi S	L	loo!
111	el Hern	H
(se Hissis a		

Z = high impedance X = don't care

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	±35	mA
lcc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub> 108 W0	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	of order

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \le (V_{in} \text{ or } V_{out}) \le V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
tr, tf	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Her EFINEY	10		Guaranteed Limit			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} = 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	0.8	0.8	0.8	V
VOH	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
3.1	FUNCTION TAE	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	TURN ATA
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	٧
1	J J	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	5.5	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	5.5	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	5.5	8	80	160	μΑ

ΔICC	Additional Quiescent Supply	Vin=2.4 V, Any One Input		≥ -55°C	25°C to 125°C	
	Current	$V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0 \mu A$	5.5	2.9	2.4	mA

## NOTES

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

Symbol		Gua			
	Parameter BAND BENT OT BENT BENT DE	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	25	31	38	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	30	38	45	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	30	38	45	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
Cin	Maximum Input Capacitance	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

## NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Enabled Output)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	1 8	-
	PD = CPD Vcc <sup>2</sup> f+Icc Vcc For load considerations, see Chapter 4 subject listing on page 4-2.	55	рг

## **SWITCHING WAVEFORMS**

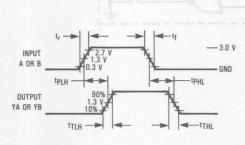


Figure 1

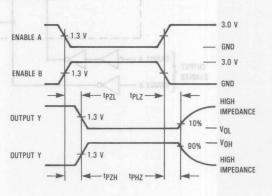


Figure 2

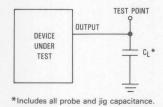
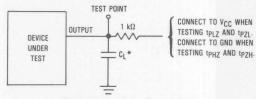


Figure 3. Test Circuit



\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

5

ENABLE A -

ENABLE B

OUTPUT

# Quad 3-State Bus Transceivers High-Performance Silicon-Gate CMOS

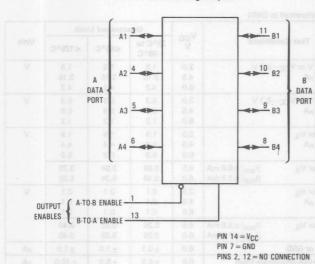
The MC54/74HC242 and MC54/74HC243 are identical in pinout to the LS242 and LS243. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These quad bus transceivers are designed for asynchronous two-way communications between data buses. The states of the Output Enables (A-to-B Enable and B-to-A Enable) determine both the direction of data flow (from A to B or from B to A) and the modes of the Data Ports (input, output, or high-impedance).

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 130 FETs or 32.5 Equivalent Gates (HC242)
   146 FETs or 36.5 Equivalent Gates (HC243)

### LOGIC DIAGRAM

HC242-Inverting Outputs HC243-Noninverting Outputs



# MC54/74HC242 MC54/74HC243



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

### ORDERING INFORMATION

MC74HCXXXN Plastic MC54HCXXXJ Ceramic MC74HCXXXD SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### 

NC = NO CONNECTION

9 B3

8 B4

A4 0 6

GND [ 7

### FUNCTION TABLE

Control Inputs			74HC242	MC54/74HC24		
		Data Port Status		Data Port State		
	B-to-A Enable	А	В	А	В	
Н	Н	ō	1	0	- 1	
L	Н	Z	Z	Z	Z	
Н	L	Z	Z	Z	Z	
L	L	1	ō	1	0	

I = input, O = output,  $\overline{O}$  = inverting output, Z = high impedance

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub>

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject

or Vout)≤VCC.

listing on page 4-2.

### MAXIMUM BATINGS\*

Symbol	Parame	Parameter		Unit
Vcc	DC Supply Voltage (Reference	ed to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced	I to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Reference	ed to GND)	-0.5 to V <sub>CC</sub> +0.5	V
a lin	DC Input Current, per Pin		± 20	mA
lout	DC Output Current, per Pin	THE SPACE SHE	± 35	mA
Icc	DC Supply Current, V <sub>CC</sub> and	GND Pins	± 75	mA
PD	Power Dissipation in Still Air,	Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	(A of 8 mot) so	- 65 to + 150	°C
TL	Lead Temperature, 1 mm from (Plast	n Case for 10 Seconds ic DIP or SOIC Package) (Ceramic DIP)	260 300	spec

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter			Max	Unit
VCC	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Ty	ypes	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0	1000 500 400	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

337.1	P2 0 1 U3.8400 80FA 1			Guaranteed Limit			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
3.16	PUNCTION TA	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
A	8 A siden3 elden3	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	± 1.0	± 1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

### MC54/74HC242 • MC54/74HC243

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

		Vcc	Gua			
Symbol	Parameter		25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, A to B/B to A	2.0	100	125	150	ns
tPHL	(Figures 1 and 3)	4.5	20	25	30	
		6.0	17	21	26	
tPLZ,	Maximum Propagation Delay, Output Enable to Output A or B	2.0	150	190	225	ns
tPHZ	(Figures 2 and 4)	4.5	30	38	45	
	Incommond to the second	6.0	26	33	38	
tPZL,	Maximum Propagation Delay, Output Enable to Output A or B	2.0	150	190	225	ns
tPZH	(Figures 2 and 4)	4.5	30	38	45	
1	11-10   de	6.0	26	33	38	
tTLH,	Maximum Output Transition Time, Any Output	2.0	60	75	90	ns
tTHL	(Figures 1 and 3)	4.5	12	15	18	
		6.0	10	13	15	
Cin	Maximum Input Capacitance	-	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	-	15	15	15	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	Tugte
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	- 10 P- 5H41 31H5H - H	pF

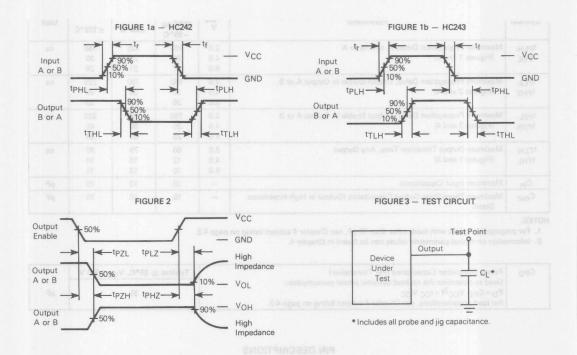
### PIN DESCRIPTIONS

### DATA PORTS

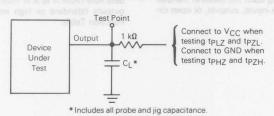
A1, A2, A3, A4 (Pins 3, 4, 5, 6) and B1, B2, B3, B4 (Pins 11, 10, 9, 8) — Data on these pins may be transferred between data buses. Depending upon the states of the Output Enables, these pins may be inputs, outputs, or open circuits (high-impedance).

### CONTROL INPUTS

A-to-B Enable (Pin 1) and B-to-A Enable (Pin 13) — Data on these Output Enables determine both the direction of data flow (from A to B or from B to A) and the states of the outputs (standard or high impedance), according to the Function Table.

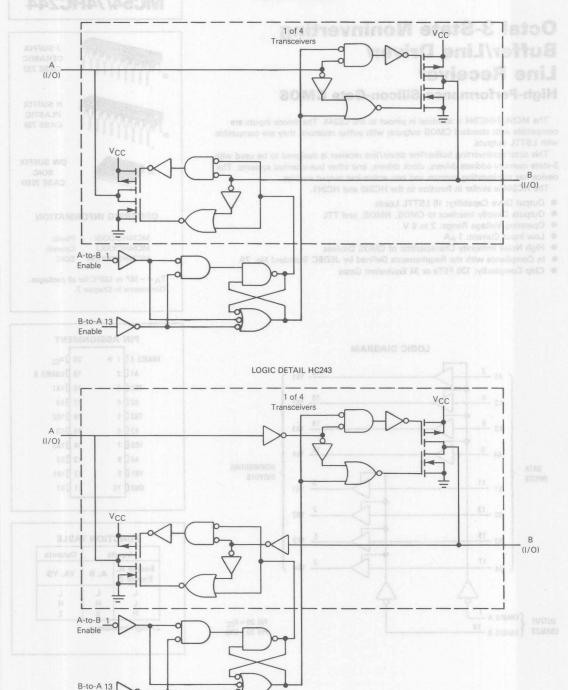


### FIGURE 4 - TEST CIRCUIT



### MC54/74HC242•MC54/74HC243

LOGIC DETAIL HC242



5

MOTOROLA HIGH-SPEED CMOS LOGIC DATA

Enable

# MC54/74HC244

# **Octal 3-State Noninverting Buffer/Line Driver/** Line Receiver

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC244 is identical in pinout to the LS244. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has noninverting outputs and two active-low output enables.

The HC244 is similar in function to the HC240 and HC241.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 136 FETs or 34 Equivalent Gates



CERAMIC **CASE 732** 



N SUFFIX PLASTIC **CASE 738** 



DW SUFFIX SOIC CASE 751D

### ORDERING INFORMATION

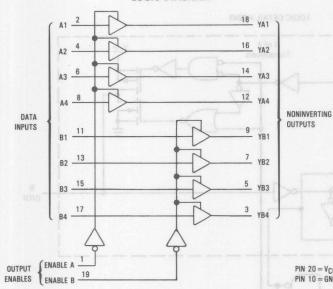
MC74HCXXXN MC54HCXXXJ MC74HCXXXDW

Plastic Ceramic

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

PIN ASSIGNMENT

### LOGIC DIAGRAM



ENABLE A	1 •	20	D v <sub>CC</sub>
A1 [	2	19	ENABLE B
YB4 [	3	18	YA1
A2 [	4	17	] B4
YB3 [	5	16	YA2
A3 [	6	15	] B3
YB2	7	14	] YA3
A4 [	8	13	] B2
YB1	9	12	YA4
GND [	10	11	B1

### FUNCTION TABLE

LOIGO	I I OIY	MULL
Input	s	Outputs
Enable A, Enable B	А, В	YA, YB
L	L	L
L	Н	Н
Н	X	Z

Z = high impedance

PIN 20 = VCC

PIN 10 = GND

Symbol	Simil tonson Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	o AVor A
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C ye.A ,see

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter			Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)			6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage	(Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Packag	je Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> =2.0 V	0	1000	ns
	(Figure 1)	$V_{CC} = 4.5 \text{ V}$	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Vcc	Gua	aranteed L	imit	
Symbol	Parameter	Test Condi	Test Conditions		25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤20 μA	000	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	KO A
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V  I <sub>out</sub>   ≤20 μA	18490	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V PITUS RO AY
VOH	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤20 μA	.071	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$	$ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
иших ээр б	1331 (COURT 1331 ) (COURT 1331 ) (COURT 1331 )	Vin= VIL	$ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	30 ± 1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impeda Vin = VIL or VIH Vout = VCC or GND	nce State	6.0	±0.5	±5.0	± 10.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	- 8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

	Value Unit This divice contains				Guaranteed Limit			
Symbol	clouitry to guard again due to high crade voltages	I didiliotoi		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay	, A to YA or B to YB		2.0	115	145	175	ns
tPHL	(Figures 1 and 3)			4.5 6.0	23 20	29 25	35 30	ni.
t <sub>PLZ</sub> , Maximum Propagation Delay, t <sub>PHZ</sub> (Figures 2 and 4)	, Output Enable to YA or YB		2.0 4.5	150 30	190 38	225 45	ns	
	756 mW range GNB ≤ IV <sub>Sh</sub> or Vou	TSIG sinis	6.0	26	33	38	Q9	
tPZL,	Maximum Propagation Delay (Figures 2 and 4)	, Output Enable to YA or YB		2.0	150 30	190 38	225 45	ns
t, Unused	feigl, either GND ör VOC			6.0	26	33	38	
tTLH, tTHL	Maximum Output Transition (Figures 1 and 3)	Time, Any Output	Processes) samic DIP1	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	was way assus wating Conditions	ege textoo ele semended Opi	500 <del>,-1</del> 8r	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Outpo State)	ut Capacitance (Output in High-I	mpedance	27 <u>m</u> 12 100° to	15	15	15	pF

### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	333
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	underst impage V tumpuO 34 StrV tumet 30	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	Operating Temperature, All Package Type	AT

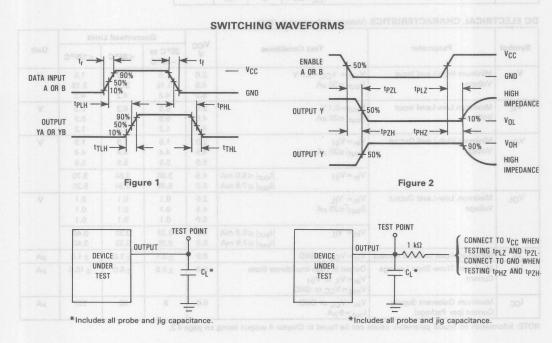


Figure 3. Test Circuit

Figure 4. Test Circuit

### PIN DESCRIPTIONS

### INPUTS

A1, A2, A3, A4, B1, B2, B3, B4 (PINS 2, 4, 6, 8, 11, 13, 15, 17) — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

### CONTROLS

Enable A, Enable B (PINS 1, 19) — Output enables (active-low). When a low level is applied to these pins, the outputs

are enabled and the devices function as noninverting buffers. When a high level is applied, the outputs assume the high-impedance state.

### OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (PINS 18, 16, 14, 12, 9, 7, 5, 3) — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high-impedance outputs.

### LOGIC DETAIL

TO THREE OTHER
A OR B BUFFERS

ONE OF 8
BUFFERS

# **Octal 3-State Noninverting Buffer/Line Driver/Line Receiver** with LSTTL-Compatible Inputs **High-Performance Silicon-Gate CMOS**

The HCT244 is identical in pinout to the LS244. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT244 is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has non-inverted outputs and two active-low output enables. The HCT244 is the noninverting version of the HCT240. See also HCT241.

Output Drive Capability: 15 LSTTL Loads

TTL/NMOS-Compatible Input Levels

Outputs Directly Interface to CMOS, NMOS, and TTL

Operating Voltage Range: 4.5 to 5.5 V

Low Input Current: 1 μA

In Compliance with the Requirements Defined by JEDEC Standard No. 7A

• Chip Complexity: 112 FETs or 28 Equivalent Gates

# MC54/74HCT244



CERAMIC **CASE 732** 



N SUFFIX PLASTIC **CASE 738** 



DW SUFFIX SOIC CASE 751D

### ORDERING INFORMATION

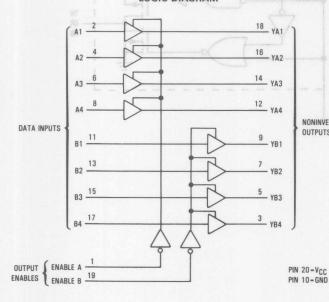
MC74HCTXXXN MC54HCTXXXJ MC74HCTXXXDW

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

**PIN ASSIGNMENT** 

### LOGIC DIAGRAM



NONINVERTING **DUTPUTS** 

ENABLE A	1 .	20	□ VCC
A1 🗆	2	19	ENABLE
YB4	3	18	YA1
A2 🗆	4	17	□ B4
YB3 🗆	5	16	YA2
A3 🗆	6	15	□ B3
YB2 🗆	7	14	TYA3
A4 🗆	8	13	□ B2
YB1 🗆	9	12	TYA4
GND 🗆	10	11	□ B1
			1

### **FUNCTION TABLE**

Input	Outputs	
Enable A, Enable B	A, B	YA, YB
L	L	L
L	Н	Н
Н	X	Z

Z = high impedance X = don't care

### VIOJ4/74110124

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
q <sub>q</sub> T <sub>L</sub> ∃q	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

**MAXIMUM RATINGS\*** 

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	T	A 88 B		Guaranteed Limit			8 H0 A
Symbol	Parameter	Test Conditions	Vcc	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	ay BS At
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	0.8	0.8	0.8	٧
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	
VOL	Maximum Low-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \mu \text{A}$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	5.5	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  Vin = V <sub>IL</sub> or V <sub>IH</sub> Vout = V <sub>CC</sub> or GND	5.5	± 0.5	±5.0	± 10.0	μА
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	5.5	8	80	160	μΑ

ΔICC	Additional Quiescent Supply	Vin = 2.4 V, Any One Input		≥ -55°C	25°C to 125°C	
	Current	Vin=VCC or GND, Other Inputs		receipt of Book as	to or the asked and fi	
	secure and any and it is secured in secure	I <sub>out</sub> =0 μA	5.5	2.9	2.4	m/

### NOTES:

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

	This device contain			Gua	aranteed Li	imit	Symbs
Symbol	circuity to guard egel due to high nortic voltage	Parameter Parameter		25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation De (Figures 1 and 3)	ay, A to YA or B to YB	to GMD)	25	31	38	ns
tPLZ, tPHZ	Maximum Propagation De (Figures 2 and 4)	ay, Output Enable to YA or YB		30	38	45	ns
tPZL, tPZH	Maximum Propagation De (Figures 2 and 4)	ay, Output Enable to YA or YB	side of Continue D	30	38	45	ns
tTLH, tTHL	Maximum Output Transition (Figures 1 and 3)	on Time, Any Output		12	15	18	ns
Cin	Maximum Input Capacitan	ce	COMPAND OF SOME	10	10	10	pF
Cout	Maximum Three-State Out	put Capacitance (Output in High-Imped	dance State)	15	15	15	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Enabled Output)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	Sheri Hara
	Used to determine the no-load dynamic power consumption:  PD = CPD VCc <sup>2</sup> f + ICC VCC	MENDED OP 35 ATTNO CONDITION	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	1 Paggranter	dmid

### **SWITCHING WAVEFORMS**

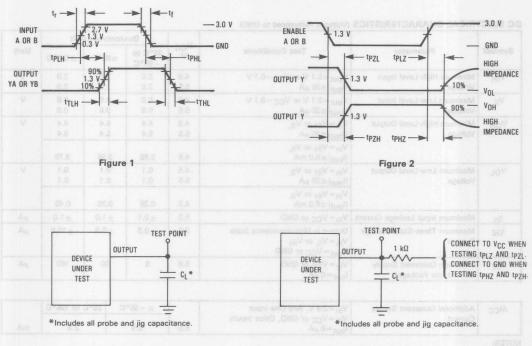
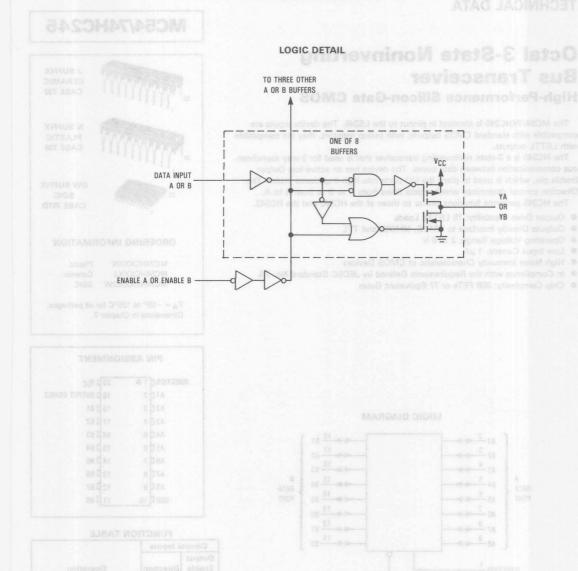


Figure 3. Test Circuit

Figure 4. Test Circuit





# **Octal 3-State Noninverting Bus Transceiver**

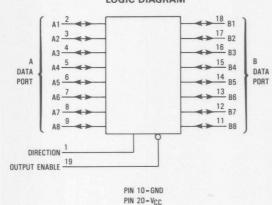
# **High-Performance Silicon-Gate CMOS**

The MC54/74HC245 is identical in pinout to the LS245. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC245 is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A. The HC245 performs functions similar to those of the HC640 and the HC643.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 308 FETs or 77 Equivalent Gates

### LOGIC DIAGRAM



## MC54/74HC245



J SUFFIX CERAMIC **CASE 732** 



N SUFFIX PLASTIC **CASE 738** 



DW SUFFIX SOIC CASE 751D

### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXDW SOIC

Plastic Ceramic

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### PIN ASSIGNMENT

DIRECTION	1 0	20 D VCC
A1 C	2	19 DOUTPUT ENABLE
A2 [	3	18 D B1
A3 C	4	17 D B2
A4 C	5	16 D B3
A5 C	6	15 D B4
A6 C	7	14 D B5
A7 C	8	13 D B6
A8 C	9	12 B7
GND	10	11 D B8

### **FUNCTION TABLE**

Contr	ol Inputs	
Output Enable	Direction	Operation
L	L	Data Transmitted from Bus B to Bus A
L	н	Data Transmitted from Bus A to Bus B
Н	X	Buses Isolated (High-Impedance State)

X = don't care

IMAIIVI	IVI NATIIVOS"		
Symbol	rimil beatre Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	ten V ind
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
VI/O	DC I/O Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	O.V.
lin	DC Input Current, per Pin 1 or 19	±20	mA
1/0	DC I/O Current, per I/O Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL.	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	O You

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to G	(ND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (F	Referenced to GND)	oq 0. p	Vcc	V
TA	Operating Temperature, All Package	Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V	0	1000 500	ns
		V <sub>CC</sub> = 6.0 V	0	400	

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

					Guaranteed Limit			A 90 A
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH ACTOR	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub>  I <sub>out</sub>  ≤20 μA	-0.1 V	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub>  I <sub>out</sub>   ≤20 μA	-0.1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
are 2	Figure 2	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>	$ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
1546 974 9 1545 984 37 1545 984 985	The state of the s	Vin=VIH or VIL	I <sub>out</sub>   ≤6.0 mA  I <sub>out</sub>   ≤7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin si	Maximum Input Leakage Current	Vin = VCC or GND, F	Pin 1 or 19	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Imper Vin = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND,		6.0	±0.5	±5.0	± 10.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	Value Unit: The daylos contains		Guaranteed Limit			Symbol
	Parameter 0.7% of 2.0— segution of sets  V. G. Frynd V of 2.1	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, A to B, B to A	2.0	100	125	150	ns
tPHL	(Figures 1 and 3)	4.5 6.0	20 17	25 21	30 26	mil
tPLZ, tPHZ	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL,	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance (Pin 1 or Pin 19)	loosti si	10	10	10	pF
Cout	Maximum Three-State I/O Capacitance (I/O in High-Impedance State)	St m 45	15	15	15	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	Symbol
	Used to determine the no-load dynamic power consumption:  PD = CPD VCc <sup>2</sup> f + ICC VCC	DC Supely Vol 04 (Referenced to	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	DC Input Voltage, Output Voltage	Vin Vout

### SWITCHING WAVEFORMS

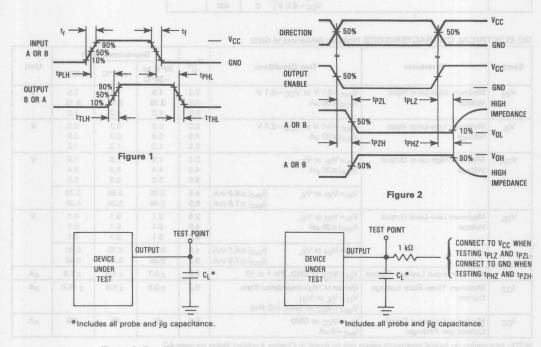


Figure 3. Test Circuit

Figure 4. Test Circuit

B DATA PORT

14 B5

A7 8 12 B7 A8 9 11 B8

OUTPUT ENABLE 19

DATA

PORT

DIRECTION

# Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs

**High-Performance Silicon-Gate CMOS** 

The MC54/74HCT245 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT245 is identical in pinout to the LS245.

The HCT245 is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HCT245 performs functions similar to those of the HCT640 and the HCT643.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 304 FETs or 76 Equivalent Gates

# MC54/74HCT245



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



DW SUFFIX SOIC CASE 751D

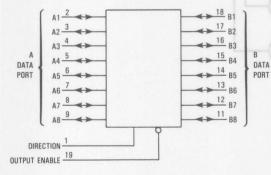
### ORDERING INFORMATION

MC74HCTXXXN MC54HCTXXXJ MC74HCTXXXDW

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM



PIN 10-GND PIN 20-V<sub>CC</sub>

### PIN ASSIGNMENT

DIRECTION	1 •	20 VCC
A1 C	2	19 OUTPUT ENABLE
A2 [	3	18 D B1
A3 C	4	17 B2
A4 C	5	16 B3
A5 [	6	15 D B4
A6 C	7	14 D B5
A7 C	8	13 B6
A8 🗆	9	12 B7
GND C	10	11 B8

### **FUNCTION TABLE**

Contre	ol Inputs	
Output Enable	Direction	Operation
L	L	Data Transmitted from Bus B to Bus A
L	Н	Data Transmitted from Bus A to Bus B
Н	X	Buses Isolated (High-Impedance State)

X = don't care

### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit	
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	V	
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V	
VI/O	DC I/O Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V	
lin	DC Input Current, per Pin 1 or 19	±20	mA	
11/0	DC I/O Current, per I/O Pin	±35	mA	
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 75	mA	
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW	
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C	
RT∟ Rq	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C	

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
tr, tf	Input Rise and Fall Time (Figure 1)	0	500	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	1	C.I. TURYIO	\ \v	Guaranteed Limit			TUSTRIT
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out}$ =0.1 V or $V_{CC}$ -0.1 V $ I_{out}  \le 20 \mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	٧
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	٧
Vон	Voltage Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	٧
IMPEDANC		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	
VOL	Maximum Low-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \mu \text{A}$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	٧
	Wallender Progress	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=Vcc or GND, Pin 1 or 19	5.5	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND, I/O Pins	5.5	±0.5	±5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 µA	5.5	8	80	160	μΑ

ΔICC	Additional Quiescent Supply	V <sub>in</sub> = 2.4 V, Any One Input	annette.	≥ -55°C	25°C to 125°C	
	Current	Vin = VCC or GND, Other Inputs				
		$I_{out} = 0 \mu A$	5.5	2.9	2.4	mA

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

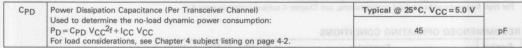
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this highimpedance circuit. For proper operation, Vin and Vout should be constrained to the range GND≤(Vin or Vout)≤VCC.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or VCC). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

	Value Central Pris device contains	Gua	aranteed Li	imit	
Symbol	rege toward of visitation Parameter or 8.0 — ICHS or positive distribution of site digital or each	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, A to B or B to A (Figures 1 and 3)	22	28	33	ns
tPLZ, tPHZ	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	30	38	45	ns
tPZL,	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	30	38	45	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
Cin	Maximum Input Capacitance (Pin 1 or 19)	10	10	10 I	pF
Cout	Maximum Three-State I/O Capacitance (I/O in High-Impedance State)	15	15	15	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.



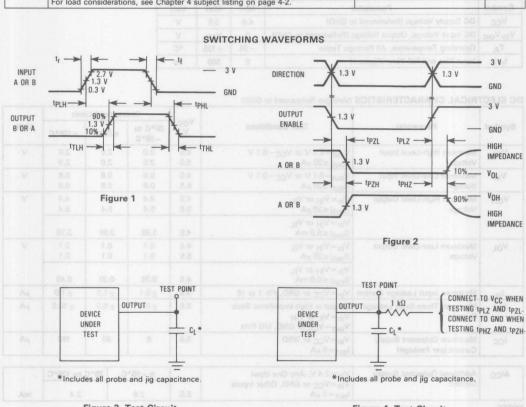
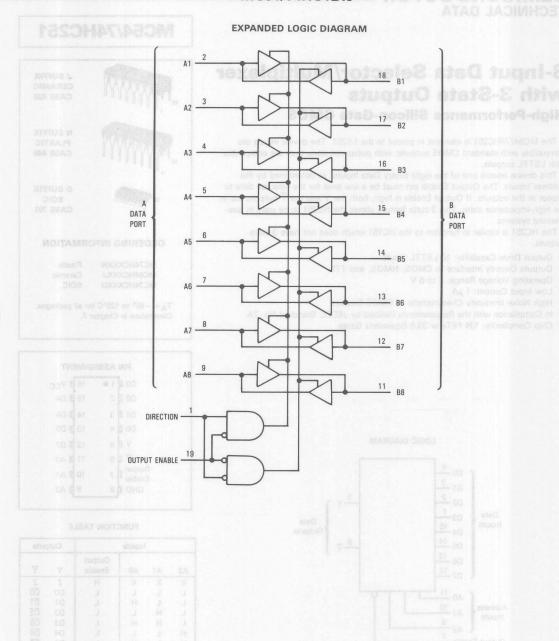


Figure 3. Test Circuit

Figure 4. Test Circuit

### MC54/74HCT245



# 8-Input Data Selector/Multiplexer with 3-State Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC251 is identical in pinout to the LS251. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Output Enable pin must be a low level for the selected data to appear at the outputs. If Output Enable is high, both the Y and the  $\overline{Y}$  outputs are in the high-impedance state. This 3-state feature allows the HC251 to be used in busoriented systems.

The HC251 is similar in function to the HC151 which does not have 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates

# MC54/74HC251



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



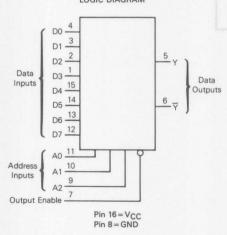
D SUFFIX SOIC CASE 751

### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM



### PIN ASSIGNMENT

D3 [	1 0	16	VCC
D2 [	2	15	D4
D1 [	3	14	D5
D0 [	4	13	D6
Y (	5	12	<b>D</b> 7
₹ [	6	11	1 A0
Output I Enable	7	10	A1
GND I	8	9	A2

### FUNCTION TABLE

	Inputs			Out	puts
A2	A1	A0	Output Enable	Y	₹
X	X	X	Н	Z	Z
L	L	L	L	D0	D0
L	L	Н	L	D1	D1
L	H	L	L	D2	D2
L	Н	Н	L	D3	D3
Н	L	L	L	D4	D4
Н	L	Н	L	D5	D5
Н	Н	L	L	D6	D6
Н	Н	Н	L	D7	D7

Z = high-impedance state

D0, D1. . . D7 = the level of the respective D input

# 5

### MAYIMIIM PATINGS\*

Symbol	Jents baerna Parameter	Value	Unit
VCC	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 25	mA
lout	DC Output Current, per Pin	± 50	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{In}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

SOIC Package: -7 mW/°C from 65° to 125°C

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	SS Parameter 3.5		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	/ <sub>CC</sub> =2.0 V / <sub>CC</sub> =4.5 V / <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns 08 asa

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Typical @ 25°C, Vorg=5.0 V	Test Conditions		Guaranteed Limit			CPD
Symbol	Parameter			25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  l <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	rd V	
	the high impedance state.	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	or be
V <sub>OL</sub> Maximum Low-Level Output Voltage	Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V IA 0
	amot	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	Functi
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Symbol	alreading to good againg thus to high statile veltager	Parameter (1) 4 4 4 4 4 4	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay,	Input D to Output Y or Y	2.0	185	230	280	ns
tPHL	(Figures 1, 2 and 5)		4.5 6.0	37 31	46 39	56 48	
tPLH,	Maximum Propagation Delay, (Figures 3 and 5)	Input A to Output Y or $\overline{Y}$	2.0 4.5	205 41	255 51	310 62	ns
.90V≥1	range GND = (Vita or Vigo		6.0	35	43	53	
tPLZ, tPHZ	Maximum Propagation Delay, (Figures 4 and 6)	Output Enable to Output Y	2.0 4.5 6.0	195 39 33	245 49 42	295 59 50	ns
tPZL, tPZH	Maximum Propagation Delay, (Figures 4 and 6)	Output Enable to Output Y	2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Output $\overline{Y}$ (Figures 4 and 6)		2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
tPZL, tPZH	Maximum Propagation Delay, (Figures 4 and 6)	Output Enable to Output $\overline{Y}$	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 5)		2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	ST THE THE STATE OF THE STATE O		10	10	10	pF
Cout	Maximum Three-State Output State)	Capacitance (Output in High-Impedance	ie Typus	15	15	15	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	36	pF

### PIN DESCRIPTIONS

### **INPUTS**

D0, D1, . . ., D7 (PINS 4, 3, 2, 1, 15, 14, 13, 12) — Data inputs. Data on one of these eight binary inputs may be selected to appear on the output.

### CONTROL INPUTS

A0, A1, A2 (PINS 11, 10, 9) — Address inputs. The data on these pins are the binary address of the selected input (see the Function Table).

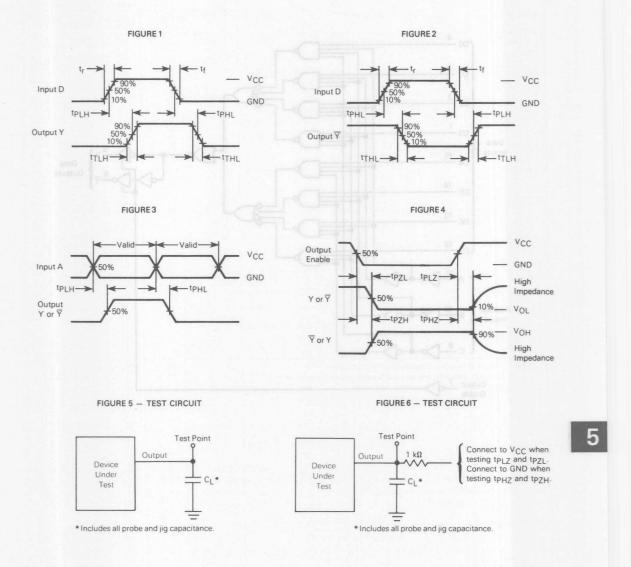
OUTPUT ENABLE (PIN 7) — Output Enable. This input pin must be at a low level for the selected data to appear at the outputs. If the Output Enable pin is high, both the Y and  $\overline{Y}$  outputs are taken to the high-impedance state.

### **OUTPUTS**

Y,  $\overline{Y}$  (PINS 5, 6) — Data outputs. The selected data is presented at these pins in both true (Y output) and complemented ( $\overline{Y}$  output) forms.

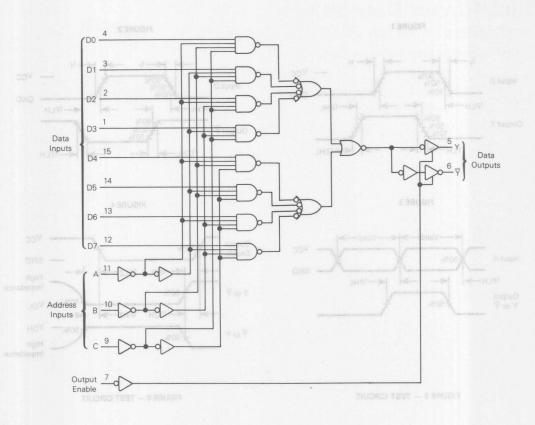
### MC54/74HC251

### SWITCHING WAVEFORMS



### MC54/74HC251

### EXPANDED LOGIC DIAGRAM



# Dual 4-Input Data Selector/ Multiplexer With 3-State Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC253 is identical in pinout to the LS253. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The Address inputs select one of four Data inputs from each multiplexer. Each multiplexer has an active-low Output Enable control and a three-state noninverting output.

The HC253 is similar in function to the HC153 which does not have three-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 108 FETs or 27 Equivalent Gates

### MC54/74HC253



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



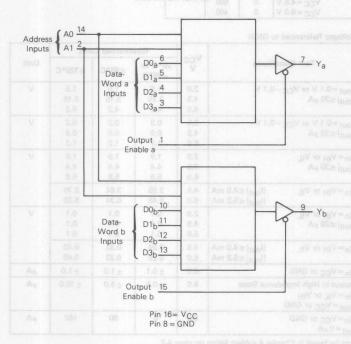
D SUFFIX SOIC CASE 751

### **ORDERING INFORMATION**

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### **BLOCK DIAGRAM**



### PIN ASSIGNMENT

	1 7001	OTATALE	
Output Enable a A1	1 •	16 15	V <sub>CC</sub> Output Enable t
D3 <sub>a</sub> [	3	14	
D2 <sub>a</sub>	4	13	D3 <sub>b</sub>
D1a	5	12	D2 <sub>b</sub>
DO <sub>a</sub> [	6	11	D1 <sub>b</sub>
Ya	7	10	DOp
GND [	8	9	Yb
	-	-	

### **FUNCTION TABLE**

	Inputs		
A1	A0	Output Enable	Y
X	X	esHao.	Z
L	L	L	DO
L	Н	L	D1
Н	L	L	D2
H	Н.	L	D3

D0, D1, D2, and D3= the level of the respective Data Inputs

Z= high impedance

ı	-	all	
L		а.	
Γ	w	91	
	_	_	-

Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	٧
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
lcc	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL Baus a	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	o.C

due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \le (V_{in} \text{ or } V_{out}) \le V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	٧
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	w chro		W	Guaranteed Limit			inputs	
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V or } V_{\text{CC}} = 0.1 \text{ V}$ $ V_{\text{out}}  \le 20 \mu\text{A}$		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V or } V_{\text{CC}} = 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu\text{A}$	V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
VOH	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
	alugot tugisiO		out   ≤4.0 mA out   ≤5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
FQ SQ	7 4 7		out   ≤4.0 mA out   ≤5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  Vin = VIL or VIH  Vout = VCC or GND		6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

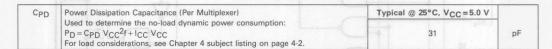
<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

Symbol			Guaranteed Limit			
	Parameter wolesticA — (81 th 81) Blue Country	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Data to Output Y (Figures 1 and 3)	2.0 4.5 6.0	140 28 24	175 35 30	210 42 36	ns
tPLH, tPHL	Maximum Propagation Delay, Address to Output Y (Figures 1 and 3)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance		10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	\ <u>-</u>	15	15	15	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.



### **SWITCHING WAVEFORMS** VCC OUTPUT 50% ENABLE A OR D GND - tPZL GND tPLZ-HIGH tPHL -- tPLH IMPEDANCE 10% VOL -tPZH tpHZ -> tTHL-VOH 50% HIGH IMPEDANCE

Figure 1

Figure 2

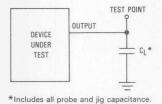


Figure 3. Test Circuit

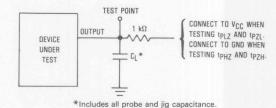


Figure 4. Test Circuit

### PIN DESCRIPTIONS

### DATA INPUTS

 $D0_a$ - $D3_a$ ,  $D0_b$ - $D3_b$  (PINS 3, 4, 5, 6, 10, 11, 12, 13) — Data inputs. When one of these pairs of inputs is selected and the outputs are enabled, the outputs assume the state of the respective inputs.

**OUTPUT ENABLE (PINS 1, 15)** — Active-low three-state Output Enable. When a low level is applied to these inputs, the corresponding outputs are enabled. When a high level is applied, the outputs assume the high-impedance state.

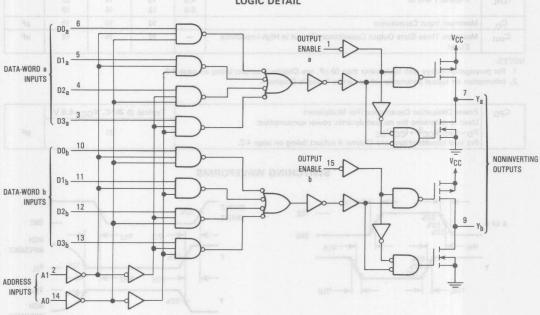
### **CONTROL INPUTS**

A0, A1 (PINS 2, 14) — Address inputs. These inputs select the pair of Data inputs to appear at the corresponding outputs.

### **OUTPUTS**

Ya, Yb (PINS 7, 9) - Noninverting three-state outputs.

### LOGIC DETAIL



# Quad 2-Input Data Selector/ Multiplexer With 3-State Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC257 is identical in pinout to the LS257. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects a (4-bit) nibble from either the A or B inputs as determined by the Select input. The nibble is presented at the outputs in noninverted form when the Output Enable pin is at a low level. A high level on the Output Enable pin switches the outputs into the high-impedance state.

The HC257 is similar in function to the HC157 which do not have 3-state outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 108 FETs or 27 Equivalent Gates

# MC54/74HC257



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



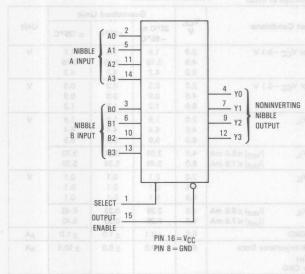
D SUFFIX SOIC CASE 751

### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM



### PIN ASSIGNMENT

SEL	ECT	1 •	16	D v <sub>CC</sub>	
	AO [	2	15	ООТРОТ	ENABLE
	B0 [	3	14	1 A3	
	YOL	4	13	] B3	
	A1 C	5	12	] Y3	
	B1 [	6	11	] A2	
	Y1 [	7	10	] B2	
rgril le	GND [	8	9	] Y2	

### **FUNCTION TABLE**

Inp	Outputs		
Output Enable	Select	Y0-Y3	
Н	X	Z	
L	L	A0-A3	
L	Н	B0-B3	

X = don't care
Z = high-impedance state
A0-A3,B0-B3 = the levels of the respective Nibble Inputs.

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GNI	D)	2.0	6.0	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Refe	erenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	er e line	Parameter Test Conditions	v <sub>CC</sub>	Guaranteed Limit			
	Parameter			25°C to -55°C	≤85°C	≤125°C	Uni
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	) essepti	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 6.0 \text{ mA}$ $ I_{\text{out}}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
6A-8A 88-88		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	6.0	±0.1	±1.0	± 1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

Symbol	Parameter	.,	Guaranteed Limit			
		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Nibble A or B to Output Y (Figures 1 and 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
tPLH, tPHL	Maximum Propagation Delay, Select to Output Y (Figures 2 and 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance		10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	-	15	15	15	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	39	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		p,

# PIN DESCRIPTIONS

### **INPUTS**

A0, A1, A2, A3 (PINS 2, 5, 11, 14) — Nibble A input. The data present on these pins is transferred to the output when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

B0, B1, B2, B3 (PINS 3, 6, 10, 13) — Nibble B input. The logic data present on these pins is transferred to the output when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

### **OUTPUTS**

Y0, Y1, Y2, Y3 (PINS 4, 7, 9, 12) — Nibble output. The selected nibble input is presented at these outputs when the

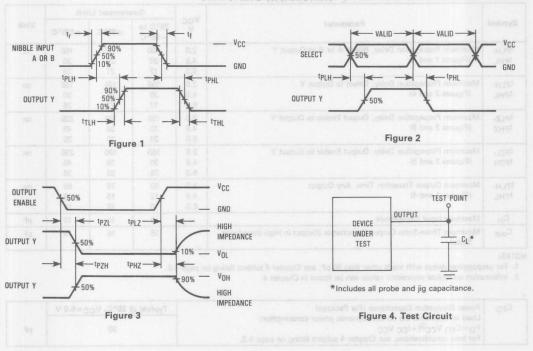
Output Enable input is at a low level. For the Output Enable input at a high level, the outputs are switched to the high impedance state.

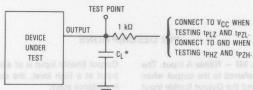
### **CONTROL INPUTS**

**SELECT (PIN 1)** — Nibble select. This input determines the nibble to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

OUTPUT ENABLE (PIN 15) — Output Enable. A low level on this input allows the selected input data to be presented at the outputs. A high level on this input forces the outputs into the high-impedance state.

### SWITCHING WAVEFORMS

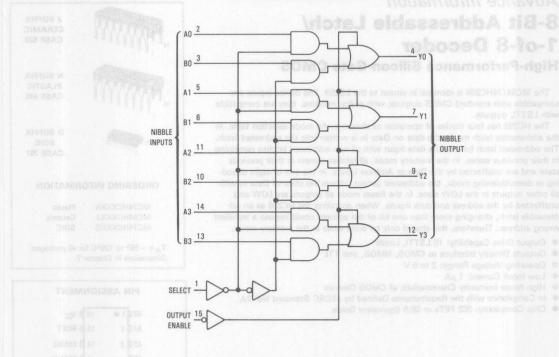




\*Includes all probe and jig capacitance.

Figure 5. Test Circuit

### **EXPANDED LOGIC DIAGRAM**



# Advance Information

# 8-Bit Addressable Latch/ 1-of-8 Decoder

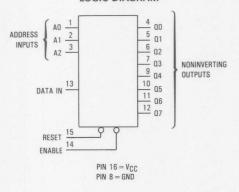
# **High-Performance Silicon-Gate CMOS**

The MC54/74HC259 is identical in pinout to the LS259. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one-of-eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode all outputs are LOW and unaffected by the address and data inputs. When operating the HC259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 202 FETs or 50.5 Equivalent Gates

### LOGIC DIAGRAM



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

# ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### PIN ASSIGNMENT

A0 C	1 .	16	þ	VCC
A1 C	2	15	9	RESET
A2 [	3	14	þ	ENABL
00 [	4	13	þ	DATA
010	5	12	b	07
02	6	11	þ	06
031	7	10	þ	05
GND	8	9	9	04

# MODE SELECTION TABLE

Enable	Reset	Mode
L	Н	Addressable Latch
Н	Н	Memory
L	L	8-Line Demultiplexer
Н	L	Reset

# LATCH SELECTION TABLE

Add	dress In	puts	Latch
С	В	A	Addressed
L	L	L	Q0
L	L	H	Q1
L	Н	L	02
L	Н	H	Q3
Н	L	L	Q4
Н	L	H	Q5
Н	Н	L	Q6
Н	Н	H	Ω7

This document contains information on a new product. Specifications and information herein are subject to change without notice.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any

# **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

MC54/74HC259

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to G	(ND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Parameter	Test Conditions	V <sub>CC</sub>	Guaranteed Limit			
Symbol				25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
	Voltago	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	4.2	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V <sub>OL</sub> Maximum Low-Level Voltage	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
		$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

<sup>†</sup>Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

# AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	This device contains p					Guaranteed Limit			Journal
Symbol	circuitry to guarta against	Parameter			VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay	, Data to Output	at 8.0 —		2.0	185	230	280	ns
†PHL	(Figures 1 and 6)				4.5 6.0	37 31	46 39	56 48	
tPLH, tPHL	Maximum Propagation Delay (Figures 2 and 6)	, Address Select to Outp	ut	1910 plm	2.0 4.5 6.0	215 43 37	270 54 46	325 65 55	ns
tPLH, tPHL	Maximum Propagation Delay (Figures 3 and 6)	, Enable to Output	e n 55	Records	2.0 4.5 6.0	200 40 34	250 50 43	300 60 51	ns
tPHL	Maximum Propagation Delay (Figures 4 and 6)	, Reset to Output		Passage   PRC sees	2.0 4.5 6.0	155 31 26	195 39 33	235 47 40	ns
tTLH, tTHL	Maximum Output Transition (Figures 1 and 6)	Time, Any Output	Э дийжээх	C beliated O C gent	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance			976	01 100	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	DC Input Voltage, Getput Vollage IRs	
	PD = CPD VCC <sup>2</sup> f + ICC VCC	30	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

# TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

	Parameter 1000 or too reals		Guaranteed Limit			
Symbol			25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Address or Data to Enable (Figure 5)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Enable to Address or Data (Figure 5)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t <sub>W</sub>	Minimum Pulse Width, Reset or Enable (Figure 3 or 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

# SWITCHING WAVEFORMS

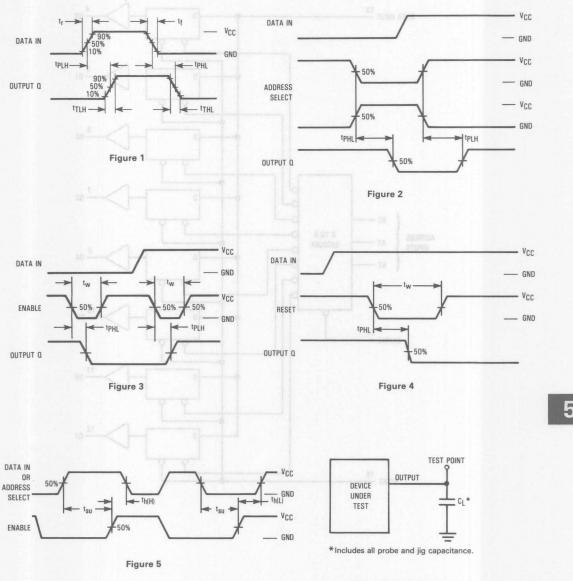
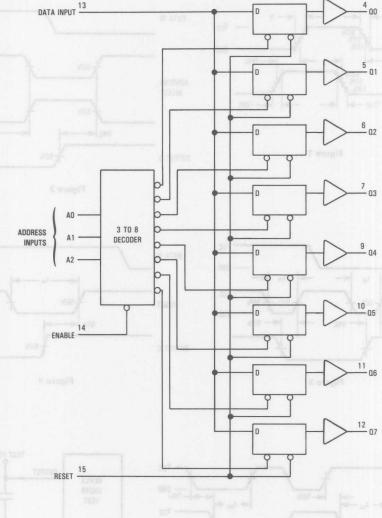


Figure 6. Test Circuit



# Quad 2-Input Exclusive NOR Gate with Open-Drain Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC266 is identical in pinout to the LS266. The HC266 inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC266 output is a high-performance MOS N-Channel FET. Therefore, with suitable output pullup resistors, this gate can be used in wired AND applications. Using the output characteristic curves in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

To comply with JEDEC Standard No. 7A, Motorola's HC266 manufactured after the date code 8547 has open-drain outputs. HC266 prior to the date code 8547 has standard CMOS outputs. (See Figure 4 for date code identifier.)

For applications requiring Standard CMOS outputs, use the HC7266.

- Output Drive Capability: 10 LSTTL Loads with Suitable Pullup Resistor
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 52 FETs or 13 Equivalent Gates

# MC54/74HC266



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

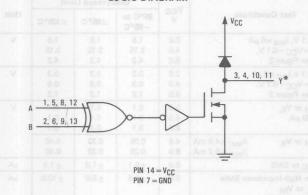
### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# LOGIC DIAGRAM



\*Denotes Open-Drain Outputs

# PIN ASSIGNMENT

	de monetan		1
A1 [	1 •	14	VCC
B1 [	2	13	] B4
Y1 [	3	12	] A4
Y2 [	4	11	] Y4
A2 [	5	10	] Y3
B2 [	6	9	] B3
GND [	7	8	] A3

# **FUNCTION TABLE**

Inp	uts	Output
Α	В	Y
L	L	Z
L	Н	L
Н	ni aLmix	Lat
Н	Н	Z

Z = high impedance

**E** 

# MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND≤(Vin or Vout)≤VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	AV JUA DOED	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referen	ced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Parameter Test Conditions		V	Guaranteed Limit			
Symbol		VCC	25°C to -55°C	≤85°C	≤125°C	Uni	
VIH	Minimum High-Level Input Voltage	$V_{out}$ =0.1 V, $I_{out}$ =0 $\mu$ A or $V_{out}$ = $V_{CC}$ -0.1 V, $R_{pu}$ per Figure 2	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out}$ =0.1 V, $I_{out}$ =0 $\mu$ A or $V_{out}$ = $V_{CC}$ -0.1 V, $R_{pu}$ per Figure 2	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
×		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=V <sub>CC</sub> or GND	6.0	±0.1	± 1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	6.0	±0.5	±5.0	± 10.0	μΑ
ICC	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

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к	ā.	,

Symbol			Gua			
	Parameter GMA G3RIW	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLZ,	Maximum Propagation Delay,	2.0	120	150	180	ns
tPZL	(Figures 1 and 2)	4.5	24	30	36	
	10 <sup>1</sup> A	6.0	20	26	31	
tTHL	t <sub>THI</sub> Maximum Output Transition Time, Any Output	2.0	75	95	110	ns
	(Figures 1 and 2)	4.5	15	19	22	
	MIRWIN S	6.0	13	16	19	
Cin	Maximum Input Capacitance	-	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	-	10	10	10	pF

### NOTES

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	11	pF

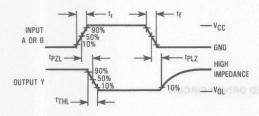
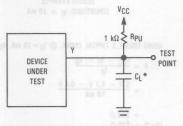
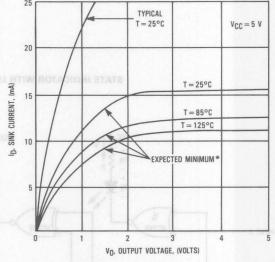


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.



\*The expected minimum curves are not guarantees, but are design aids.

Figure 2. Test Circuit

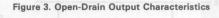
MC74HC266

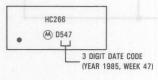
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4 DIGIT DATE CODE
(YEAR 1985, WEEK 47)

4a. DIP

Figure 4. Date Code Identifier





4b. SOIC

# **Octal D Flip-Flop with Common Clock and Reset**

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC273 is identical in pinout to the LS273. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The device consists of eight D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active-low.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 264 FETs or 66 Equivalent Gates

# MC54/74HC273



J SUFFIX CERAMIC **CASE 732** 



N SUFFIX PLASTIC **CASE 738** 



DW SUFFIX SOIC CASE 751D

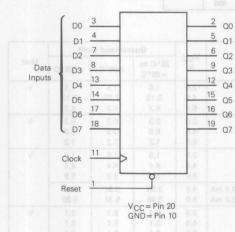
# ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ

Plastic Ceramic MC74HCXXXDW SOIC

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# LOGIC DIAGRAM



Noninverting Outputs

PIN ASSIGNMENT

Reset [	1 •	20	v <sub>CC</sub>
20 0	2	19	07
D0 [	3	18	D7
D1 [	4	17	D6
Q1 C	5	16	Q6
Q2 [	6	15	Q5
D2 [	7	14	D5
D3 C	8	13	D4
Q3 <b>C</b>	9	12	04
GND [	10	11	Clock

# **FUNCTION TABLE**

	Inputs		Output
Reset	Clock	D	Q
L	X	X	L
Н		Н	Н
Н		L	L
Н	L	X	no change
H	~	X	no change

# MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND  $\leq$  (Vin or Vout)  $\leq$  VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	d to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	0184 1700	1 so 2		Guaranteed Limit			1 - 15
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voltage  I <sub>out</sub>   ≤ 2	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V	
	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$		3.98 5.48	3.84 5.34	3.70 5.20		
V <sub>OL</sub> Maximum Low-Level Output Voltage		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40		
lin	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 µA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

# 5

	<u>Carusta</u> Parameter		Gua			
Symbol		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
<sup>t</sup> PHL	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance		10	10	10	pF

### MOTES

For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

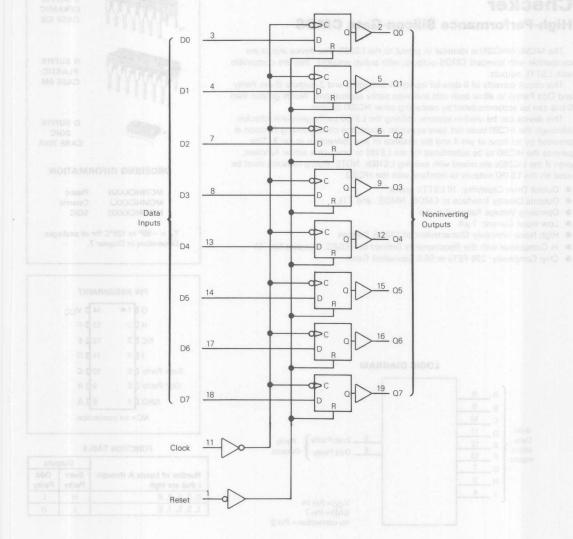
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	A A	
	PD = CPD VCC <sup>2</sup> f + ICC VCC	38	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	http://www.inforces/i	

# TIMING REQUIREMENTS (Input t. = te=6 ns)

	purposeds of pur equid be supriout.		Gua			
Symbol	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Data to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Clock to Data (Figure 3)	2.0 4.5 6.0	25 5 5	30 6 6	40 8 7	ns
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>W</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>W</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.



# 9-Bit Odd/Even Parity Generator/ Checker

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC280 is identical in pinout to the LS280. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This circuit consists of 9 data-bit inputs (A through I) and 2 outputs (Even Parity and Odd Parity) to allow both odd and even parity applications. Words greater than 9-bits can be accommodated by cascading other HC280 devices.

This device can be used in systems utilizing the LS180 parity generator/checker. Although the HC280 does not have expander inputs, the corresponding function is provided by an input at pin 4 and the absence of any connection at pin 3. This permits the HC280 to be substituted for the LS180 to produce a similar function, even if the HC280s are mixed with existing LS180s. NOTE: Pullup resistors must be used on the LS180 outputs to interface with the HC280.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 226 FETs or 56.5 Equivalent Gates

# MC54/74HC280



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



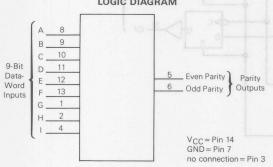
D SUFFIX SOIC CASE 751A

# ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# LOGIC DIAGRAM



# PIN ASSIGNMENT

G	1 •	14	b vcc
н	2	13	J F
NC E	3	12	ΞE
10	4	11	D
Even Parity	5	10	<b>1</b> C
Odd Parity	6	9	В
GND C	7	8	A

NC = no connection

### **FUNCTION TABLE**

	Out	Outputs Even Odd
Number of Inputs A through I that are high	Even Parity	Odd Parity
0, 2, 4, 6, 8	Н	L
1, 3, 5, 7, 9	L	Н

# 5

# **MAXIMUM RATINGS\***

Symbol	simil bonnes Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

SOIC Package: -7 mW/°C from 65° to 125°C

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter			Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)			6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	0	Vcc	٧	
TA	Operating Temperature, All Package Types			+ 125	°C
t <sub>r</sub> , t <sub>f</sub>		V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V	0	1000 500	ns
		$V_{CC} = 4.5 \text{ V}$	0	400	

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Guaranteed Limit			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out}$ =0.1 V or $V_{CC}$ -0.1 V $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH Minimum Hig Voltage	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	* jo eds	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
Voltage	Maximum Low-Level Output Voltage	V <sub>In</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	is all probe and jig carportance.	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Symbol	This daylos contains			v <sub>CC</sub>	Gua	Symbo		
	eleculty to guard egan	Parameter			25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Dela (Figures 1 and 2)	ay, Data Inputs to Parity		2.0 4.5 6.0	205 41 35	255 51 43	310 62 53	ns
tTLH, tTHL	Maximum Output Transitio (Figures 1 and 2)	n Time, Any Output	emic pur	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitano	ce UG	Package	J08	10	10	10	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	Futstiles
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	60 60 60 60 60 60 60 60 60 60 60 60 60 6	pF

# PIN DESCRIPTIONS

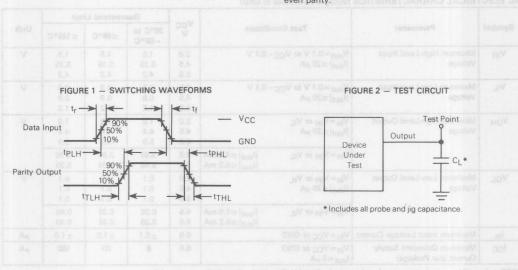
### **INPUTS**

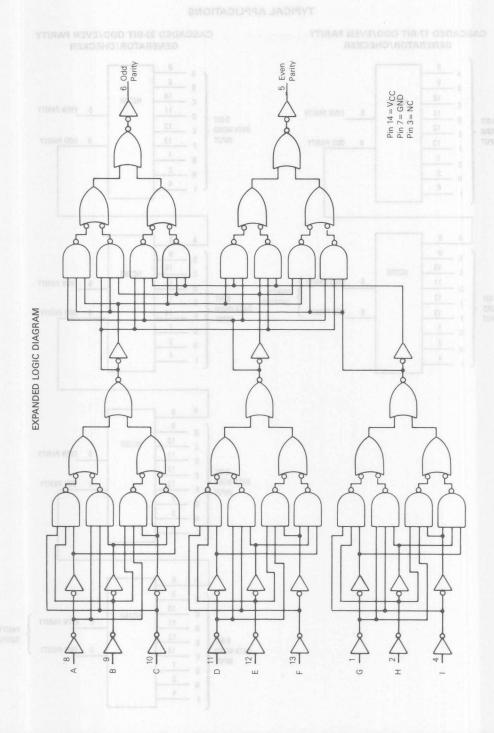
# A, B, C, D, E, F, G, H, I (Pins 8-13, 1, 2, 4) — Nine-bit data-word inputs. The data word placed on these pins is checked for even or odd parity.

### OUTPUTS

**Even Parity (Pin 5)** — Even-parity output. This pin goes high if the data word has even parity and low if the data word has odd parity.

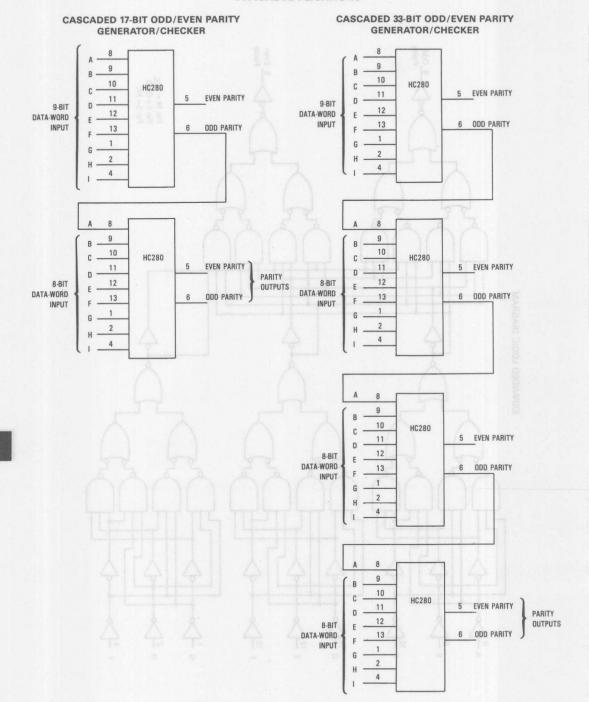
Odd Parity (Pin 6) — Odd-parity output. This pin goes high if the data word has odd parity and low if the data word has even parity.





# MC54/74HC280

# TYPICAL APPLICATIONS



# Product Preview

# 4-Bit Binary Full Adder with Fast Carry

# **High-Performance Silicon-Gate CMOS**

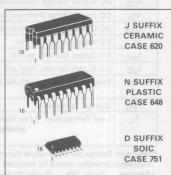
The MC54/74HC283 is identical in pinout to the LS283. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC283 is a high-speed 4-bit binary Full Adder with internal carry lookahead. The device adds two 4-bit words (A and B) plus the Carry-In bit. The binary sum appears at the Sum outputs (S), and any resulting carries appear at the Carry-Out pin.

Because of the symmetry of the binary add function, the HC283 can be used either with all inputs and outputs active-high (positive logic), or with all inputs and outputs active-low (negative logic). With active-high inputs, Carry In must be held low when no carry-in is intended.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 212 FETs or 53 Equivalent Gates

# MC54/74HC283



# ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### 

# FUNCTION TABLE

Inputs			Outputs		
An	Bn	$CIn = CO_{n-1}$	Sn	COn = CI <sub>n+1</sub>	
L	L	L	L	L	
L	CFO	allevo Herback	H	JOY L	
L	Н	F 60019	H	L	
L	Н	Н	L	Н	
Н	L	L	Н	L	
Н	L	Н	L	Н	
Н	Н	L	L	Н	
H	Н	Н	Н	H	

n=0, 1, 2, 3 (A3, B3, and S3 are the most significant bits)

		LOGIC I			
BINARY	$ \begin{cases} A0 \frac{5}{3} \\ A1 \frac{3}{4} \end{cases} $	3.18 4.2 4.2 0.3 0.3	2.6 4.5 8.0 2.0 4.5	4 so	0 - 30V 10
	$\begin{bmatrix} A3 & \frac{12}{2} \\ B0 & \frac{6}{2} \end{bmatrix}$	9.1		13 S2 10 S3	BINARY SUM OUTPUTS
ADDEND B	B1 15 B2 15 B3 11	5.9 5.48 5.48		Am 0.42   (100) Am 1.02   (100)	
CA	ARRY IN 7	1.0	Z,0 4,5 4,0	9 CARRY	OUT
			6 = V <sub>CC</sub> = GND		

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, VCC and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

SOIC Package: -7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
Vcc	DC Supply Voltage (Referenced to GN	2.0	6.0	V	
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Ref	erenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Ty	/pes	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	1 1 1 1 1 1		V	Gua			
Symbol	Parameter	Test Conditions		25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2 0.3 0.9 1.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2		V
Voн	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
==03	An Bn CineCOn-1 B	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	1 J J H	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	± 0.1	±1.0	± 1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 µA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

Punctional operation should be restricted to the Recommended Operating Conditional Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

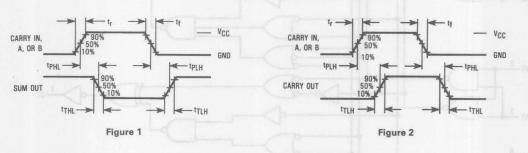
tplH, tplH, tpHL			Pr			
	Parameter	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
	Maximum Propagation Delay, Carry In to Sum Out (Figures 1 and 3)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
	Maximum Propagation Delay, A or B to Sum Out (Figures 1 and 3)	2.0 4.5 6.0	270 54 46	340 68 58	405 81 69	ns
	Maximum Propagation Delay, Carry In to Carry Out (Figures 2 and 3)	2.0 4.5 6.0	195 39 33	245 49 42	295 59 50	ns
tPLH, tPHL	Maximum Propagation Delay, A or B to Carry Out (Figures 2 and 3)	2.0 4.5 6.0	225 45 38	280 56 48	340 68 58	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	I	10	10	10	pF

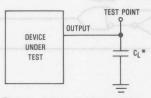
### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
   Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:		
	PD=CPD VCC2f+ICC VCC	130	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

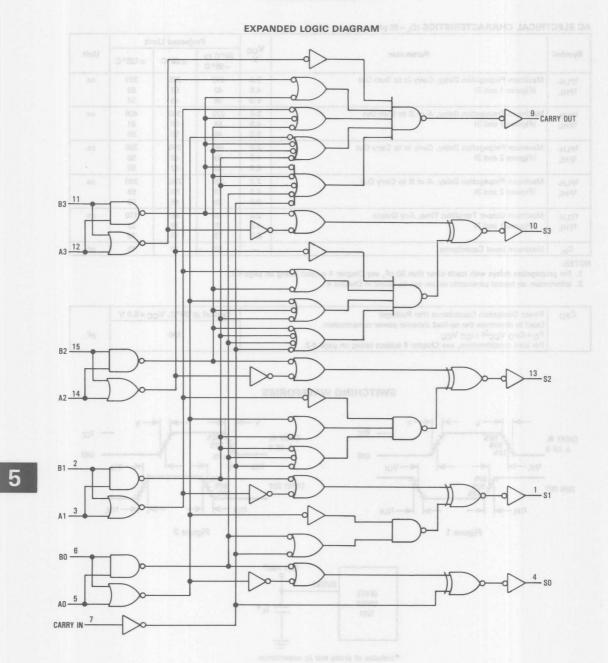
# **SWITCHING WAVEFORMS**





\*Includes all probe and jig capacitance.

Figure 3. Test Circuit



# Advance Information

# 8-Bit Bidirectional Universal Shift Register with Parallel I/O **High-Performance Silicon-Gate CMOS**

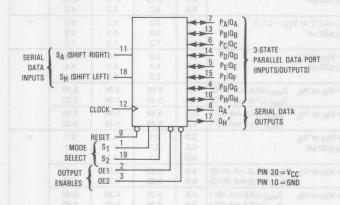
The MC54/74HC299 is identical in pinout to the LS299. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with

The HC299 features a multiplexed parallel input/output data port to achieve full 8-bit handling in a 20 pin package. Due to the large output drive capability and the 3-state feature, this device is ideally suited for interface with bus lines in a bus-ori-

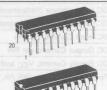
Two Mode-Select inputs and two Output Enable inputs are used to choose the mode of operation as listed in the Function Table. Synchronous parallel loading is accomplished by taking both Mode-Select lines, S1 and S2, high. This places the outputs in the high-impedance state, which permits data applied to the data port to be clocked into the register. Reading out of the register can be accomplished when the outputs are enabled. The active-low asynchronous Reset overrides all other

- Output Drive Capability: 15 LSTTL Loads for Q<sub>A</sub> through Q<sub>H</sub> 10 LSTTL Loads for QA' and QH'
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates

# LOGIC DIAGRAM



# MC54/74HC299



J SUFFIX CERAMIC **CASE 732** 



N SUFFIX PLASTIC **CASE 738** 



DW SUFFIX SOIC CASE 751D

# ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXDW SOIC

Plastic Ceramic

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# PIN ASSIGNMENT

S1 [	1.	20	vcc
OE1	2	19	] S2
0E2 [	3	18	SH
PG/QG [	4	17	ο <sub>H</sub> '
PE/QE [	5	16	PH/QH
PC/QC [	6	15	PF/QF
PA/QA D	7	14	PD/QD
QA' [	8	13	PB/QB
RESET	9	12	CLOCK
GND [	10	11	SA

This document contains information on a new product. Specifications and information herein are subject to change without notice

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or VCC). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject

or  $V_{out}) \leq V_{CC}$ .

listing on page 4-2.

# MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

SOIC Package: -7 mW/°C from 65° to 125°C For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

Functional operation should be restricted to the Recommended Operating Conditions. †Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to	GND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (	Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package	e Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V	0	1000 500	ns
	THE PARTY OF THE P	V <sub>CC</sub> = 6.0 V	0	400	

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	61 2 2 1 130		.,	Gua	aranteed Li	imit	
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
VOH	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	ATAN ATAN
		$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}   I_{\text{out}}  \le 6.0 \text{ mA (P/Q)}$ $ I_{\text{out}}  \le 7.8 \text{ mA (P/Q)}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
		$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}} \qquad  I_{\text{out}}  \le 4.0 \text{ mA } (Q') \\  I_{\text{out}}  \le 5.2 \text{ mA } (Q')$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}   I_{\text{out}}  \le 6.0 \text{ mA (P/Q)}$ $ I_{\text{out}}  \le 7.8 \text{ mA (P/Q)}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
		$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}} \qquad  I_{\text{out}}  \le 4.0 \text{ mA } (Q')$ $ I_{\text{out}}  \le 5.2 \text{ mA } (Q')$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current (Q <sub>A</sub> thru Q <sub>H</sub> )	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Ceramic DIP: -10 mW/°C from 100° to 125°C

# AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

0	Simil beconcioud		Gu			
Symbol	Onlist a Dress of Dre	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0 4.5 6.0	5.0 25 29	4.0 20 24	3.4 17 20	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to Q <sub>A</sub> ' or Q <sub>H</sub> ' (Figures 1 and 5)	2.0 4.5 6.0	170 34 29	215 43 37	255 51 43	ns
tPLH, tPHL	Maximum Propagation Delay, Clock to Q <sub>A</sub> thru Q <sub>H</sub> (Figures 1 and 5)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
<sup>t</sup> PHL	Maximum Propagation Delay, Reset to Q <sub>A</sub> ' or Q <sub>H</sub> ' (Figures 2 and 5)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
<sup>t</sup> PHL	Maximum Propagation Delay, Reset to Q <sub>A</sub> thru Q <sub>H</sub> (Figures 2 and 5)	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
tPLZ, tPHZ	Maximum Propagation Delay, OE1, OE2, S1, or S2 to Q <sub>A</sub> thru Q <sub>H</sub> (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL, tPZH	Maximum Propagation Delay, OE1, OE2, S1, or S2 to Q <sub>A</sub> thru Q <sub>H</sub> (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Q <sub>A</sub> thru Q <sub>H</sub> (Figures 1 and 5)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
tTLH, tTHL	Maximum Output Transition Time, Q <sub>A</sub> ' or Q <sub>H</sub> ' (Figures 1 and 5)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	-	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State), Q <sub>A</sub> thru Q <sub>H</sub>	-	15	15	15	pF

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
   Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package), Outputs Enabled	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:		
	PD = CPD VCC <sup>2</sup> f+ICC VCC For load considerations, see Chapter 4 subject listing on page 4-2.	240	pF

# MC54/74HC299

TIMING REQUIREMENTS (Input  $t_r = t_f = 6$  ns)

	find Lostmannia			Gua			
Symbol	orast≥ oras≥ oras	neter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Mode Select (Figure 4)	S1 or S2 to Clock	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>su</sub>	Minimum Setup Time, Data Inputs S (Figure 4)	A, S <sub>H</sub> , P <sub>A</sub> thru P <sub>H</sub> to Clock	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Clock to Mode (Figure 4)	Select S1 or S2	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
th	Minimum Hold Time, Clock to Data I (Figure 4)	nputs, S <sub>A</sub> , S <sub>H</sub> , P <sub>A</sub> thru P <sub>H</sub>	2.0 4.5 6.0	5 5 5		5 5 5	ns
t <sub>rec</sub>	Minimum Recovery Time, Reset Inac (Figure 2)	tive to Clock	2.0 4.5 6.0	50 10 9	65 13		ns
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	0.5 to Q <sub>A</sub> thru Q <sub>H</sub> 0.5 4.6 4.6 6.0	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>W</sub>	Minimum Pulse Width, Reset (Figure 2)	0.5 HD with QA or 52 to 4.5 4.5 4.5 4.5 4.5 4.5 4.5 4.5 4.5 4.5	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	0.5 6.6 0.8	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

### FUNCTION TABLE

				Inputs					Response					
Mode	Reset		ode lect		tput bles	Clock	DOMESTIC:	rial outs	PA/QA PB/QB PC/QC PD/QD PE/QE PF/QF PG/QG PH/QH	QA'QH				
100		S <sub>2</sub>	S <sub>1</sub>	OE1t	OE2†		DA	DH						
Reset	L L	X L H	L X H	L L X	L L X	X X X	X X X	X X	L L L L L L L L L L L L L L L L L L L	L L L L				
Shift Right	H H H	LLL	HHH	H X L	X H L	111	D D	X X X	Shift Right: $Q_A$ through $Q_H = Z$ ; $D_A \rightarrow F_A$ ; $F_A \rightarrow F_B$ ; etc. Shift Right: $Q_A$ through $Q_H = Z$ ; $D_A \rightarrow F_A$ ; $F_A \rightarrow F_B$ ; etc. Shift Right: $D_A \rightarrow F_A = Q_A$ ; $F_A \rightarrow F_B = Q_B$ ; etc.					
Shift Left	HHH	H	LLL	H X L	X H L	111	X X	D D	Shift Left: $Q_A$ through $Q_H = Z$ ; $D_H \rightarrow F_H$ ; $F_H \rightarrow F_G$ ; etc. Shift Left: $Q_A$ through $Q_H = Z$ ; $D_H \rightarrow F_H$ ; $F_H \rightarrow F_G$ ; etc. Shift Left: $D_H \rightarrow F_H = Q_H$ ; $F_H \rightarrow F_G = Q_G$ ; etc.	Q <sub>B</sub> D Q <sub>B</sub> D				
Parallel Load	Н	Н	Н	X	×	~	X	X	Parallel Load: $P_N \rightarrow F_N$					
Hold	H H	L L	L L	H X L	X H L	X X X	X X X	X X	Hold: $Q_A$ through $Q_H = Z$ ; $F_N = F_N$ Hold: $Q_A$ through $Q_H = Z$ ; $F_N = F_N$ Hold: $Q_N = Q_N$	PA PH PA PH PA PH				

Z = high impedance

# PIN DESCRIPTIONS

### **DATA INPUTS**

SA (PIN 11) — Serial data input (Shift Right). Data on this input is shifted into the shift register on the rising edge of Clock when S2 is low and S1 is high (shift right mode).

 $S_H$  (PIN 18) — Serial data input (Shift Left). Data on this input is shifted into the shift register on the rising edge of Clock when S2 is high and S1 is low (shift left mode).

PA through PH (PINS 7, 13, 6, 14, 5, 15, 4, 16) — Parallel data port inputs. Data on these pins can be parallel loaded into the shift register on the rising edge of Clock when both S1 and S2 are high. For any other combination of S1 and S2, these pins serve as the outputs of the shift register.

### **CONTROL INPUTS**

CLOCK (PIN 12) — Clock input. A low-to-high transition on this pin shifts the data at each stage to the next stage (shift right or left mode) or loads the data at the parallel data inputs into the shift register (parallel load mode).

OE1, OE2 (PINS 2, 3) — Active-low output enables. When both OE1 and OE2 are low, the outputs  $\Omega_A$  through  $\Omega_H$  are enabled. When one or both output enables are high, the outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected.

RESET (PIN 9) — Active-low reset. A low on this pin resets all stages of the register to a low level. The reset operation is asynchronous.

S1, S2 (PINS 1, 19) — Mode select inputs. The levels present at these pins determine the shift register's mode of operation:

S1 = S2 = Low, Hold.

S1 = Low, S2 = High. Shift left.

S1 = High, S2 = Low. Shift right.

S1 = S2 = High. Parallel load.

### **OUTPUTS**

QA', QH' (PINS 8, 17) — Serial data outputs. These are the outputs of the first and last stages of the shift register, respectively. These outputs are not 3-state outputs and have standard drive capabilities.

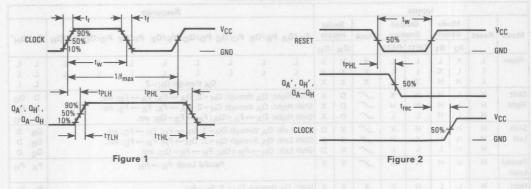
**Q<sub>A</sub> through Q<sub>H</sub> (PINS 7, 13, 6, 14, 5, 15, 4, 16)** — Parallel data port outputs. Shifted data is present at these pins when OE1 and OE2 are low. For all other combinations of OE1 and OE2 these outputs are in the high-impedance state.

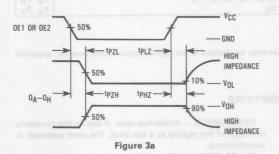
D = data on serial input

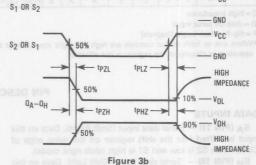
F = flip-flop (see Logic Diagram)

tWhen one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

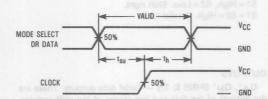
# **SWITCHING WAVEFORMS**







- VCC



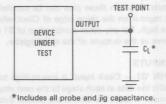


Figure 4

Figure 5. Test Circuit

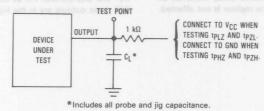
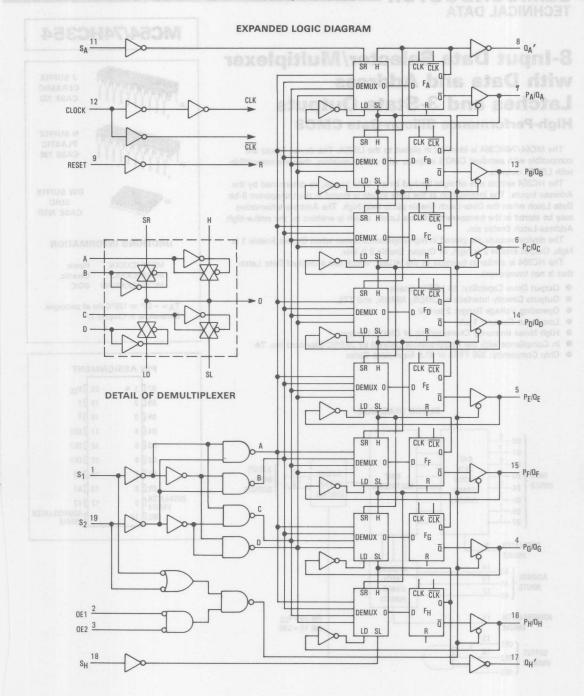


Figure 6. Test Circuit



# 8-Input Data Selector/Multiplexer with Data and Address Latches and 3-State Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC354 is identical in pinout to the LS354. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC354 selects one of eight latched binary Data Inputs, as determined by the Address Inputs. The information at the Data Inputs is stored in the transparent 8-bit Data Latch when the Data-Latch Enable pin is held high. The Address information may be stored in the transparent Address Latch, which is enabled by the active-high Address-Latch Enable pin.

The device outputs are placed in high-impedance states when Output Enable 1 is high, Output Enable 2 is high, or Output Enable 3 is low.

The HC354 is similar in function to the HC356, which has a clocked Data Latch that is not transparent.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 326 FETs or 81.5 Equivalent Gates

# MC54/74HC354



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



DW SUFFIX SOIC CASE 751D

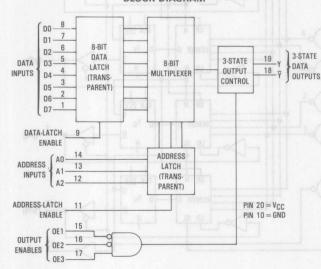
### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXDW

Ceramic

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# BLOCK DIAGRAM



# PIN ASSIGNMENT

1 •	20	vcc
2	19	PΥ
3	18	PΥ
4	17	0E3
5	16	] OE2
6	15	] OE1
7	14	] A0
8	13	] A1
9	12	] A2
10	11	ADDRESS-LATO ENABLE
	1 • 2 3 4 5 6 7 8 9 10	2 19 3 18 4 17 5 16 6 15 7 14 8 13 9 12

M NATINGO	BUT DE STEEL STANFOLD SAN WILL TO		
Parameter Parameter	Value	Unit	
DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V	
DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧	
DC Output Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	A - A - 0	
DC Input Current, per Pin	±20	mA	
DC Output Current, per Pin	± 35	mA	
DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA	
Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW	
Storage Temperature	-65 to +150	°C	
Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C pa.l-sambb	
	Parameter  DC Supply Voltage (Referenced to GND)  DC Input Voltage (Referenced to GND)  DC Output Voltage (Referenced to GND)  DC Input Current, per Pin  DC Output Current, per Pin  DC Supply Current, V <sub>CC</sub> and GND Pins  Power Dissipation in Still Air, Plastic or Ceramic DIPt  SOIC Packagef  Storage Temperature  Lead Temperature, 1 mm from Case for 10 Seconds  (Plastic DIP or SOIC Package)	Parameter         Value           DC Supply Voltage (Referenced to GND)         −0.5 to +7.0           DC Input Voltage (Referenced to GND)         −1.5 to V <sub>CC</sub> +1.5           DC Output Voltage (Referenced to GND)         −0.5 to V <sub>CC</sub> +0.5           DC Input Current, per Pin         ±20           DC Output Current, per Pin         ±35           DC Supply Current, V <sub>CC</sub> and GND Pins         ±75           Power Dissipation in Still Air, Plastic or Ceramic DIPt SOIC Packaget         500           Storage Temperature         −65 to +150           Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)         260	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter 3.6		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	2.0 6.0 V	
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	d to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	al mile,	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0	1000 500 400	ns o 02 nr

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Typical @ 25°C, VCC=5.0 V		V <sub>CC</sub>	Gua	aranteed Li	imit	
Symbol	Parameter	Test Conditions		25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
Voн	Minimum High-Level Output Voltage	Vin=VIH or VIL  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
	Jachus (lugh)	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  l <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	VAZ MOZES VE
	ce states.	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	TAL
lin	Maximum Input Leakage Current	Vin=V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	6.0	±0.5	±5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 µA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

### AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	Value Unit This device outsing p		Gua	aranteed Li	mit	
Symbol	enlage broug of viduolis asperiov otists right of auto	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, D0-D7 to Y or Y	2.0	210	265	315	ns
tPHL	(Figures 2 and 6)	4.5	42	53	63	
Danie III	Am OLL	6.0	36	45	54	
tPLH,	Maximum Propagation Delay, Data-Latch Enable to Y or Y	2.0	260	325	390	ns
tPHL	(Figures 3 and 6)	4.5	52	65	78	
ngVa	Silve of Visa of Cities of Visa of Vis	6.0	44	55	66	
tPLH,	Maximum Propagation Delay, A0-A2 to Y or Y	2.0	270	340	405	ns
tPHL	(Figures 2 and 6)	4.5	54	68	81	
besunU	(pgV ta QVD) tarihe .g.s)	6.0	46	58	69	
tPLH,	Maximum Propagation Delay, Address-Latch Enable to Y or Y	2.0	270	340	405	ns
tPHL	(Figures 3 and 6)	4.5	54	68	81	
	harmon a sharmon a company of the state of t	6.0	46	58	69	
tPLZ,	Maximum Propagation Delay, OE1-OE3 to Y or Y	2.0	160	200	240	ns
tPHZ	(Figures 4 and 7)	4.5	32	40	48	
		6.0	27	34	41 60	
tPZL,	Maximum Propagation Delay, OE1-OE3 to Y or Y	2.0	125	155	190	ns
tPZH	(Figures 4 and 7)	4.5	25	31	38	
		6.0	21	26	32	
tTLH,	Maximum Output Transition Time, Any Output	2.0	60	75	90	ns
tTHL	(Figures 1 and 6)	4.5	12	15	18	
	V 05 05	6.0	10	13	15	20
Cin	Maximum Input Capacitance	to see Talai	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High-Impedance State)	Types -	15	15	15	pF

### NOTES

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC	48	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

# 5

# PIN DESCRIPTIONS

# D0-D7 (PINS 8-1) DATA INPUTS

These eight data bits are stored in a transparent latch when the Data-Latch Enable pin is active (high). Once enabled, changing inputs will not change the contents of the latch.

# A0, A1, A2 (Pins 14, 13, 12) ADDRESS INPUTS

Selects which data bit stored in the Data Latch is routed to the outputs Y and  $\overline{Y}$ .

# DATA-LATCH ENABLE (Pin 9)

The latch is transparent to D0-D7 when enable is inactive (low). The Data-Latch contents are unaffected when enable is held active (high).

# ADDRESS-LATCH ENABLE (Pin 11)

The latch is transparent to A0, A1, and A2 when enable is inactive, (low). The Address-Latch contents are unaffected when enable is held active (high).

# OE1, OE2, OE3 (Pins 15, 16, 17) OUTPUT ENABLES

Any of the output enable pins inactive (OE1= High or OE2= High or OE3= Low) causes the outputs (Y and  $\overline{Y}$ ) to be in high-impedance states.

### Y, Y (Pins 19, 18)

These 3-state outputs (when not 3-stated) represent the data bit in the Data Latch selected by the Address Latch.

TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

				aranteed L	imit		
Symbol	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit	
t <sub>su</sub>	Minimum Setup Time, D0-D7 to Data-Latch Enable (Figure 5)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns	
t <sub>su</sub>	Minimum Setup Time, A0-A2 to Address-Latch Enable (Figure 5)	4.5   10   13   15     10   13   15     10   13   13   15     13   15     10   10   10   10   10   10					
th	Minimum Hold Time, Data-Latch Enable to D0-D7 (Figure 5)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns	
th	Minimum Hold Time, Address-Latch Enable to A0-A2 (Figure 5)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns	
t <sub>W</sub>	Minimum Pulse Width, Data-Latch Enable (Figure 3)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns	
t <sub>w</sub>	Minimum Pulse Width, Address-Latch Enable (Figure 3)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

# **FUNCTION TABLE**

	outs	Outp	5	ts	Inpu		A 11 1 1		
Description			Output Enables			Data- Latch	Address Latch Contents #		
Lancard Parks	Y	Υ	OE3	OE2	0E1	Enable	A0	A1	A2
Outputs in	Z	Z	X	×	Н	X	X	X	X
high-impedance	Z	Z	X	Н	X	X	X	X	X
states	Z	Z	L	×	X	X	X	X	X
Data Latch	<u>D0</u>	D0	Н	L	L	L	L	L	L
is transparent	D1	D1	1	1	1	1	Н	L	L
	D2	D2	33			1	L	Н	L
	D3	D3					Н	Н	L
	D2 D3 D4 D5 D6	D4	- 139			LOTE .	L	L	H
	D5	D5					Н	L	H
	D6	D6				-	L	Н	Н
d enu	D7	D7	*	*	₩	*	Н	H	H
New data is	DO <sub>n</sub>	D0 <sub>n</sub>	Н	L	L	Н	L	L	L
stored in	D1 <sub>n</sub>	D1 <sub>n</sub>		1	1	-1	Н	L	L
Data Latch	D2 <sub>n</sub>	D2 <sub>n</sub>					L	H	L
and is not	D3 <sub>n</sub>	D3 <sub>n</sub>					Н	H	L
alterable	D4 <sub>n</sub>	D4 <sub>n</sub>					L	L	Н
	D5 <sub>n</sub>	D5 <sub>n</sub>	1915 722	110			Н	L	H
	D6 <sub>n</sub>	D6 <sub>n</sub>	1				L	Н	H
	D7 <sub>n</sub>	D7n	*	*	-	*	H	H	Н

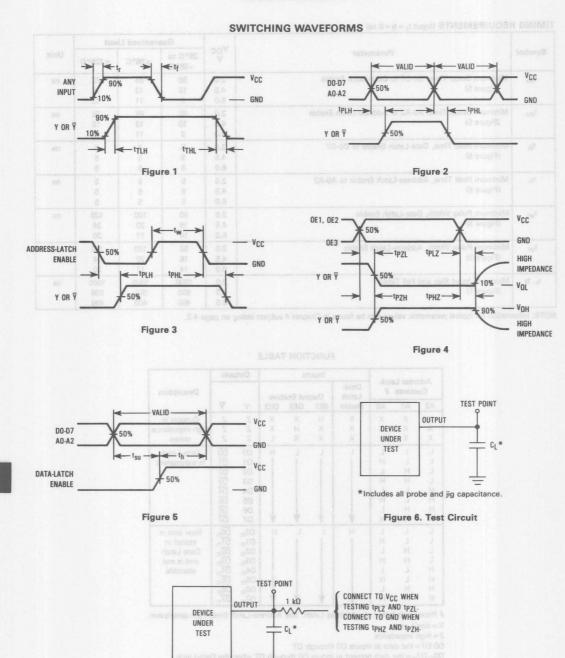
# Represents bits in the Address Latch. See Address-Latch Enable pin description.

X = don't care

Z = high impedance

D0-D7 = the data at inputs D0 through D7

 $\rm DO_{\rm N}\text{-}D7_{\rm N}=$  the data present at inputs D0 through D7 when the Data-Latch Enable pin was taken high.



5

Figure 7. Test Circuit

\*Includes all probe and jig capacitance.

compatible with standard CMDS outsides with bullup

19

3-State

Data Outputs

LE Q A2 -DQ LE Q Address-Latch 11

D2 \_ 6

D5 -

D6 \_\_\_2

D7 -

5

A1-

16

13

Output

Address

Inputs

Data

Inputs

Enable 8 D0 -D LE O D1 -D

LE Q

D LE Q

D

D Q

D DLE Q LE Q

LE Q D LE Q

LE Q Data-Latch 9 Enable

D

# 8-Input Data Selector/Multiplexer with Data and Address Latches and 3-State Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC356 is identical in pinout to the LS356. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC356 selects one of eight latched binary Data Inputs, as determined by the Address Inputs. The information at the Data Inputs is latched into the Data Latch with the rising edge of the Data-Latch Clock. The Address information may be stored in the transparent Address Latch, which is enabled by the active-high Address-Latch Enable pin.

The device outputs are placed in high-impedance states when Output Enable 1 is high, Output Enable 2 is high, or Output Enable 3 is low.

The HC356 is similar in function to the HC354, which has a transparent Data Latch.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 342 FETs or 85.5 Equivalent Gates

## MC54/74HC356



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



DW SUFFIX SOIC CASE 751D

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXDW

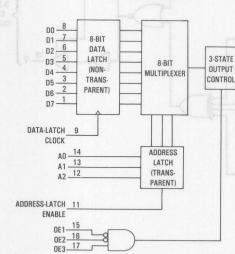
Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

DIN ACCIONMENT

PIN	A331	SINIVIENI
D7 [	1 •	20 V <sub>CC</sub>
D6 [	2	19 JY
D5 [	3	18 🛛 🔻
D4 [	4	17 DE3
D3 [	5	16 0E2
D2 [	6	15 OE1
D1 [	7	14 A0
D0 [	8	13 A1
DATA-LATCH C	9	12 A2
GND [	10	11 ADDRESS-LATCH

#### **BLOCK DIAGRAM**



19

#### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds		°C
BOL	(Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	

MC54/74HC356

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions. A 230-130 wild not provide the provided to the Recommended Operating Conditions. \*Maximum Ratings are those values beyond which damage to the device may occur.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	and the same	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)			Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

		est listing on page 4-2.	dus A vig	Gua	ranteed Li	imit	
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	8 a a	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	107
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5	0.1 0.1	0.1 0.1	0.1 0.1	V
en	8 8 8	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤6.0 mA  I <sub>out</sub>  ≤7.8 mA	6.0 4.5 6.0	0.1 0.26 0.26	0.1 0.33 0.33	0.1 0.40 0.40	At.
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  Vin = VIL or VIH  Vout = VCC or GND	6.0	±0.5	±5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	Value Units This device contains		Gua	aranteed Li	mit	ledinyi
Symbol	Parameter 2.3 at 2.0	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Data-Latch Clock to Y or $\overline{Y}$ (Figures 1 and 7)	2.0 4.5 6.0	240 48 41	300 60 51	360 72 61	ns
tpLH, tpHL	Maximum Propagation Delay, A0-A2 to Y or $\overline{Y}$ (Figures 2 and 7)	2.0 4.5 6.0	270 54 46	340 68 58	405 81 69	ns
tPLH, tPHL	Maximum Propagation Delay, Address-Latch Enable to Y or $\overline{Y}$ (Figures 3 and 7)	2.0 4.5 6.0	270 54 46	340 68 58	405 81 69	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, OE1-OE3 to Y or $\overline{Y}$ (Figures 4 and 8)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
tPZL, tPZH	Maximum Propagation Delay, OE1-OE3 to Y or \( \overline{Y} \)		125 25 21	155 31 26	190 38 32	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 7)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	Samuel	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)		15	15 (8) speriov	15	pF

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:		
	PD = CPD VCC2f + ICC VCC	48	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

#### TIMING REQUIREMENTS (Input t-=t4=6 ps)

	87 87 87 95 VID-00VIOVS 87.5 87.5 87.5 8.5 VID-00VIOVS	200	Guaranteed Limit			HILA
Symbol	Sh Sh Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, D0-D7 to Data-Latch Clock (Figure 5)	2.0 4.5	50 10	65 13	75 15	ns
V	THE REPORT OF THE PARTY OF THE	6.0	9	. 11	13	1743
t <sub>su</sub>	Minimum Setup Time, A0-A2 to Address-Latch Enable (Figure 6)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
th	Minimum Hold Time, Data-Latch Clock to D0-D7	2.0	5	5	5	ns
	(Figure 5)	4.5 6.0	5 5	5 5	5	
th	Minimum Hold Time, Address-Latch Enable to A0-A2 (Figure 6)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
tw	Minimum Pulse Width, Data-Latch Clock (Figure 1)	2.0 4.5	80 16	100 20	120 24	ns
	High-Impedence State 8.0 ±0.5 ±5.0 ±10.0	6.0	14	17	20	
tw	Minimum Pulse Width, Address-Latch Enable (Figure 3)	2.0 4.5	80 16	100 20	120 24	ns
An.	001 09 8 0.8 GHD 10-5	6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

W.T.			Inputs				Out	puts	HE LONDON
	dress L Content		Data-Latch Clock	Out OE1	put Ena	obles OE3	Y	7	Description
×××	×××	× × ×	X X X	H X X	X H X	X	Z Z Z	Z Z Z	Outputs in high-impedance states
	L H H L L H	LHLHLHLH	THE TEN	L .	L	H	D0 <sub>n</sub> D1 <sub>n</sub> D2 <sub>n</sub> D3 <sub>n</sub> D4 <sub>n</sub> D5 <sub>n</sub> D6 <sub>n</sub> D7 <sub>n</sub>	D0n D1n D2n D3n D4n D5n D6n D7n	New data is clocked into Data Latch
L L L H H H	L H H L H	L H L H L H L	H, L, or <b>\</b>	L	L	H	D0 <sub>p</sub> D1 <sub>p</sub> D2 <sub>p</sub> D3 <sub>p</sub> D4 <sub>p</sub> D5 <sub>p</sub> D6 <sub>p</sub> D7 <sub>p</sub>	D0p D1p D2p D3p D4p D5p D6p D7p	Outputs do not change states. Data Latch contents are not alterable.

<sup>\*</sup> Represents bits in the Address Latch. See Address-Latch Enable pin description.

#### PIN DESCRIPTIONS

#### D0-D7 (PINS 8-1) - DATA INPUTS

The information at the data inputs is latched into the data latch on the rising edge of the Data-Latch Clock. Changing the data inputs will not change the contents of the latch except on the rising edge of the clock.

#### A0, A1, A2 (PINS 14, 13, 12) - ADDRESS INPUTS

Selects which data bit stored in the data latch is routed to the outputs Y and  $\overline{Y}$ .

#### DATA-LATCH CLOCK (PIN 9)

The rising edge of the Data-Latch Clock latches the data (D0-D7) into the data latch.

#### ADDRESS-LATCH ENABLE (PIN 11)

The latch is transparent to inputs A0, A1, and A2 when Enable is inactive (low). The latch contents are unaffected when the Enable is held active (high)

#### OE1, OE2, OE3 (PINS 15, 16, 17) OUTPUT ENABLES

Any of the output enable pins being inactive (OE1= high or OE2= high or OE3= low) causes the outputs Y and  $\overline{Y}$  to be in high-impedance states.

#### Y, Y (PINS 19, 18)

These 3-state outputs, when not 3-stated, represent the data bit in the data latch selected by the address latch.



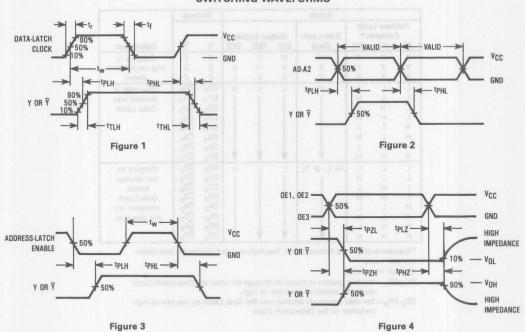
X = don't care

Z = high impedance

 $D0_{n}$ - $D7_{n}$ = the data present at inputs D0 through D7 when the Data-Latch Clock made the transition from low to high.

D0p-D7p = the data previously latched into the Data Latch by the low-to-high transition of the Data-Latch Clock

#### SWITCHING WAVEFORMS



DO-D7 VALID VCC

50%

SOND

VCC

VCC

VCC

Figure 5

CLOCK

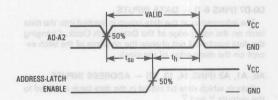


Figure 6 10 20013 HOYAL ATAG

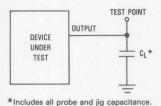
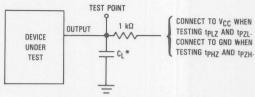


Figure 7. Test Circuit

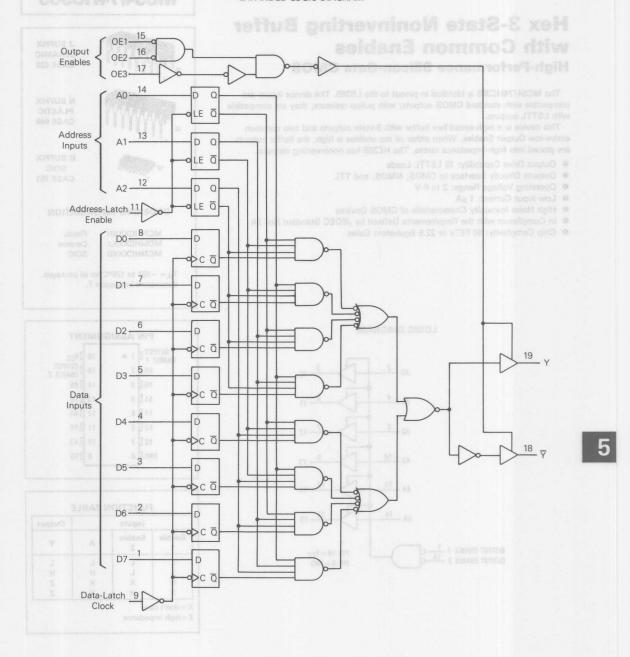


\*Includes all probe and jig capacitance.

Figure 8. Test Circuit

- GND

EXPANDED LOGIC DIAGRAM



## Hex 3-State Noninverting Buffer with Common Enables

**High-Performance Silicon-Gate CMOS** 

The MC54/74HC365 is identical in pinout to the LS365. The device inputs are

compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is a high-speed bey buffer with 3-state outputs and two common

This device is a high-speed hex buffer with 3-state outputs and two common active-low Output Enables. When either of the enables is high, the buffer outputs are placed into high-impedance states. The HC365 has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 90 FETs or 22.5 Equivalent Gates

## MC54/74HC365



J SUFFIX CERAMIC CASE 620



N SUFFIX PLÄSTIC CASE 648



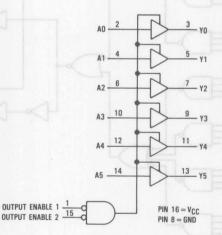
D SUFFIX SOIC CASE 751

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT

D <sub>VCC</sub>	16	1.0	OUTPUT C
OUTDUT	15	2	ENABLE 1 4
A5			YOU
] Y5	13	4	A1 C
] A4	12	5	Y1 [
] Y4	11	6	A2 [
] A3	10	7	Y2 [
] Y3	9	8	GND [

#### **FUNCTION TABLE**

1	Inputs		Output
Enable 1	Enable 2	A	Y
L		L	L
L	L	Н	Н
Н	X	X	Z
X	H	X	Z

X = don't care Z = high impedance

#### **MAXIMUM RATINGS\***

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)			Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	A AREA SHEET TOTAL		.,	Guaranteed Limit			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH -	Minimum High-Level Input Voltage	V <sub>out</sub> =V <sub>CC</sub> -0.1 V  l <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	$V_{in} = V_{IH}$	$V_{in} = V_{IH}$ $ I_{out}  \le 6.0$ $ I_{out}  \le 7.8$		3.98 5.48	3.84 5.34	3.70 5.20	
Vol.			2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
ggi ORA 136 Heri ORB OT Lea OVE TO	ORA SIG BRITEST & WASHINGTON	$V_{in} = V_{IL}$ $ I_{out}  \le 6.0$ $ I_{out}  \le 7.8$		0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	6.0	±0.1	±1.0	±1.0	μА
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	6.0	±0.5	±5.0	±10.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 µA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input  $t_f = t_f = 6 \text{ ns}$ )

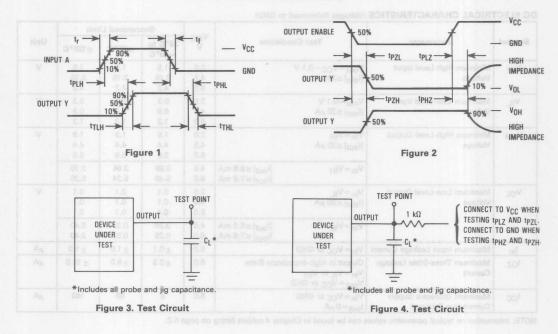
	This device contains	suleV suleV				ranteed Li	lodniyl	
Symbol	espation of are dead of each			VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, (Figures 1 and 3)	Input A to Output Y		2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
tPLZ, tPHZ	Maximum Propagation Delay, (Figures 2 and 4)	Output Enable to Output Y	1910 sins	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
tPZL, tPZH	Maximum Propagation Delay, (Figures 2 and 4)	Output Enable to Output Y	Packagel	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
tTLH, tTHL	Maximum Output Transition 7 (Figures 1 and 3)	Time, Any Output	Packagel amic DRN amic DRN	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	making Conditions	mended Op	noo <del>oli</del> on	10	10	10	pF
Cout	Maximum Three-State Output State)	Capacitance (Output in High-In	npedance	or 2001	15	15	15	pF

#### NOTES

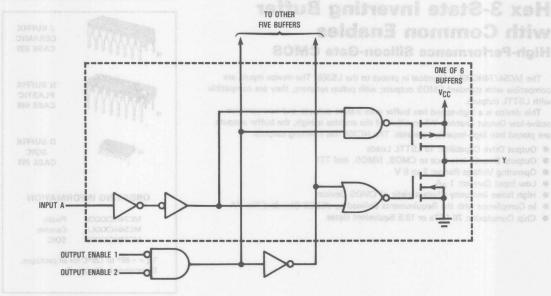
- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	DC Input Voltage Dutgest Voltage (Refere	moYe
	For load considerations, see Chapter 4 subject listing on page 4-2.	Operating Temperatum, All Parking Types	pr

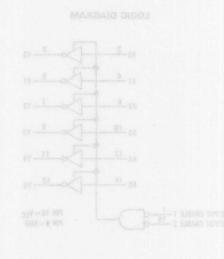
#### **SWITCHING WAVEFORMS**



LOGIC DETAIL



	0 1 1 10910



## Hex 3-State Inverting Buffer with Common Enables

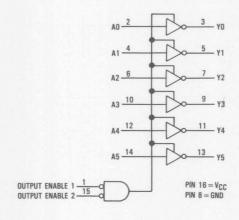
**High-Performance Silicon-Gate CMOS** 

The MC54/74HC366 is identical in pinout to the LS366. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is a high-speed hex buffer with 3-state outputs and two common active-low Output Enables. When either of the enables is high, the buffer outputs are placed into high-impedance states. The HC366 has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 78 FETs or 19.5 Equivalent Gates

#### LOGIC DIAGRAM



## MC54/74HC366



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

#### **ORDERING INFORMATION**

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT

10	16	] v <sub>CC</sub>
2	15	OUTPU
3	14	] A5
4	13	] Y5
5	12	] A4
6	11	] Y4
7	10	] A3
8	9	] Y3
	3 4 5 6 7	2 15 3 14 4 13 5 12 6 11 7 10

#### **FUNCTION TABLE**

	Inputs	Inputs		
Enable 1	Enable 2	A	Y	
L	L	L	Н	
L	L	Н	L	
Н	X	X	Z	
X	Н	X	Z	

X = don't care

Z = high impedance

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ . Unused inputs must always be tied

to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Ref	ferenced to GND)	0	Vcc	٧
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter Test Conditions		V	Guaranteed Limit				
				VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V  l <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voltage   Iou	V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V	
	V <sub>in</sub> =V <sub>IL</sub>	$ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20		
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
TO V <sub>CC</sub> . WAS NO AND 163	PUT THE GONNECT	V <sub>in</sub> =V <sub>IH</sub>	I <sub>out</sub>   ≤6.0 mA  I <sub>out</sub>   ≤7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND		6.0	±0.5	±5.0	±10.0	μА
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

			Guaranteed Limit			Symbol
Symbol	mbol segs bridge of visitable Parameter 0.1 of 3.5 only of 3.5 onl	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 4.5 6.0	95 19 16	120 24 20	145 29 25	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	No. of Secret	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High-Impedance State)	8° +0 138 108° 10	15	m 015 m	15	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	Yer
	Used to determine the no-load dynamic power consumption:  PD = CPD Vcc <sup>2</sup> f + Icc Vcc	180 Input Volt 04 Outnot Voltage Unifere	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	Operating Temperature, All Pediage Type	AT

#### **SWITCHING WAVEFORMS**

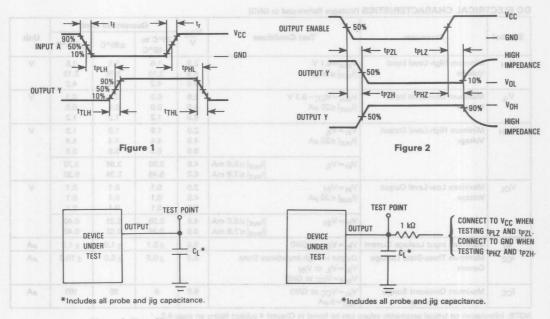
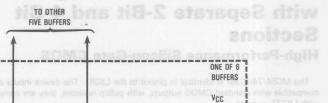


Figure 3. Test Circuit

Figure 4. Test Circuit



CASE 783

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AD 2 16 DOTTOT 70 0 14 JAS AD 4 12 JYS 11 0 5 12 DA4 AD 6 11 JY4

INPUT A -

a gona z gzz

OUTPUT SHABLE 1 10 = VEG

OUTPUT ENABLE 2 15 0

# Hex 3-State Noninverting Buffer with Separate 2-Bit and 4-Bit Sections

## **High-Performance Silicon-Gate CMOS**

The MC54/74HC367 is identical in pinout to the LS367. The device inputs are compatible with standard CMOS outputs, with pullup resistors, they are compatible with LSTTL outputs.

This device is arranged into 2-bit and 4-bit sections, each having its own active-low Output Enable. When either of the enables is high, the affected buffer outputs are placed into high-impedance states. The HC367 has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 92 FETs or 23 Equivalent Gates

## MC54/74HC367



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



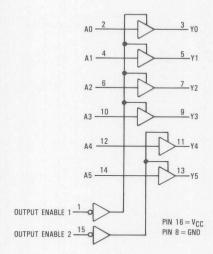
D SUFFIX SOIC CASE 751

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT

OUTPUT C	1 •	16 V <sub>CC</sub>	
A0 [	2	15 OUTPUT ENABLE	2
Y0 [	3	14 A5	
A1 [	4	13 75	
Y1 [	5	12 A4	
A2 [	6	11 Y4	
Y2 [	7	10 A3	
GND [	8	9 73	

#### **FUNCTION TABLE**

Input	Inputs	
Enable 1, Enable 2	A	Y
L	L	L
L	Н	Н
Н	X	Z

X = don't care Z = high-impedance

MC54/74HC367

#### **MAXIMUM RATINGS\***

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Packaget	500	na haus
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

SOIC Package: -7 mW/°C from 65° to 125°C

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referen	ced to GND)	0	Vcc	٧
TA	Operating Temperature, All Package Types	200 00	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	₹ 200 € 310003 T97760			Guaranteed Limit				
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V  I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Vон	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	V <sub>in</sub> =V <sub>IH</sub>	I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20		
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
MAN TO A STATE OF THE PARTY OF	# BETTEST   Did 1	V <sub>in</sub> =V <sub>IL</sub>	I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current			6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND		6.0	±0.5	±5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	Value Unit This device opnizing			Gua	Tourny B		
Symbol	Parameter 0.7.1 of 3.0-		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)		2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	1910 olms	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	Pschagel	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	(septace) (PR) pine	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	i O Sistemani	no marco	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High-Im State)	pedance	or foot	15	15	15	pF

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

5.0 V	Typical @ 25°C, V <sub>CC</sub> =5.0	PD Power Dissipation Capacitance (Per Buffer)
al DO	Here Maleston August Maleston Like	Used to determine the no-load dynamic power consumption:
pF	40	PD = CPD VCC2f+ICC VCC
	40	PD = CPD VCC <sup>2</sup> f+ICC VCC For load considerations, see Chapter 4 subject listing on page 4-2.

#### **SWITCHING WAVEFORMS**

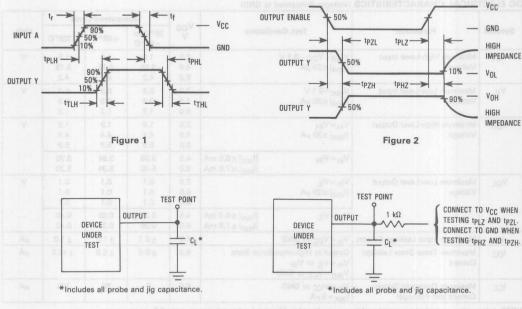
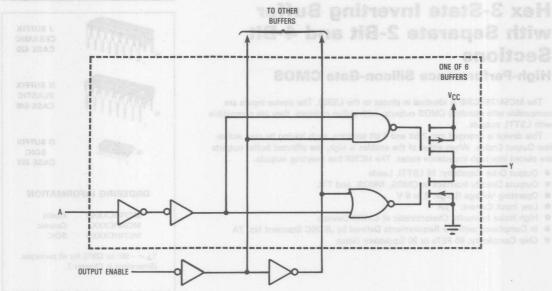


Figure 3. Test Circuit

Figure 4. Test Circuit

LOGIC DETAIL







# Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections

### **High-Performance Silicon-Gate CMOS**

The MC54/74HC368 is identical in pinout to the LS368. The device inputs are compatible with standard CMOS outputs, with pullup resistors, they are compatible with LSTTL outputs.

This device is arranged into 2-bit and 4-bit sections, each having its own active-low Output Enable. When either of the enables is high, the affected buffer outputs are placed into high-impedance states. The HC368 has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 80 FETs or 20 Equivalent Gates

## MC54/74HC368



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



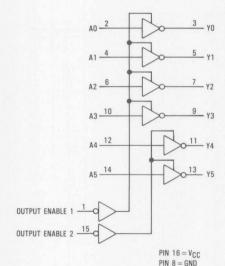
D SUFFIX SOIC CASE 751

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT

OUTPUT C	1 •	16	v <sub>cc</sub>
AO [	2	15	OUTPUT ENABLE 2
Y0 [	3	14	A5
A1 [	4	13	Y5
Y1 [	5	12	1 A4
A2 [	6	11	] Y4
Y2 [	7	10	] A3
GND [	8	9	] Y3

#### **FUNCTION TABLE**

Input	S	Output
Enable 1, Enable 2	А	Y
L	L	Н
L	Н	L
Н	X	Z

X = don't care Z = high-impedance

b

#### **MAXIMUM RATINGS\***

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	or V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	d to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	/ <sub>CC</sub> = 2.0 V / <sub>CC</sub> = 4.5 V / <sub>CC</sub> = 6.0 V	0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	TO I MAKE TURKE			Guaranteed Limit			138	
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	V <sub>IH</sub> Minimum High-Level Input V <sub>out</sub> = Il <sub>out</sub> ! ≤		GEQ SECTION	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =V <sub>CC</sub> -0.1 V  I <sub>out</sub>  ≤20 μA	H/57	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
Voн	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
		V <sub>in</sub> =V <sub>IL</sub>	$ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 20 μA		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
ASHIN GALL I	r touteon f	V <sub>in</sub> = V <sub>IH</sub>	I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  Vin = VIL or VIH  Vout = VCC or GND		6.0	±0.5	±5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

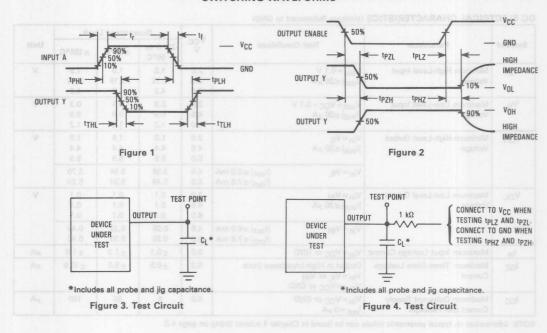
	Value Unit I I'm device consins r			Gua	losmy		
Symbol	Parameter		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)		2.0 4.5 6.0	95 19 16	120 24 20	145 29 25	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	till (NP)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	Pagastorn Stroops	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	Packaga) senic DIPs	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	mendad Opt	e R <del>o</del> cors	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-In State)	pedance	E to poor	15	15 m 01 - :91	15	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	Yee
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	OC Input Voltage, Output Voltage lifetoren	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	eageT gradout NA must sum T gradout	pr

#### **SWITCHING WAVEFORMS**





ONE OF 6 BUFFERS !

VCC

OUTPUT ENABLE -

## Octal 3-State Noninverting Transparent Latch

**High-Performance Silicon-Gate CMOS** 

The MC54/74HC373 is identical in pinout to the LS373. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

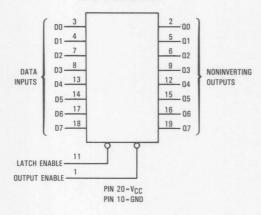
These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HC373 is identical in function to the HC573, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HC533, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 186 FETs or 46.5 Equivalent Gates

#### LOGIC DIAGRAM



### MC54/74HC373



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



DW SUFFIX SOIC CASE 751D

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXDW

Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT

FIIV	ASSIC	HAINIEIAI	
OUTPUT ENABLE	1 •	20 1 V <sub>CC</sub>	
0.00	2	19 07	
000	3	18 07	
D1 [	4	17 D6	
01 [	5	16 1 06	
02 [	6	15 05	
D2 [	7	14 05	
D3 [	8	13 D4	
03 [	9	12 ] 04	
GND [	10	11 LATCH E	NABL

#### **FUNCTION TABLE**

	Inputs			
Output Enable	Latch Enable	D	۵	
L	Н	Н	Н	
L	Н	L	L	
L	L	X	no change	
Н	X	X	Z	

X = don't care

Z = high impedance

## 5

#### **MAXIMUM RATINGS\***

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds		°C
801	(Plastic DIP or SOIC Package)	260 300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	and the Control	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	d to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	CC=2.0 V	0	1000	ns
	(Figure 1)	CC = 4.5 V	0	500	
	\	CC = 6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				VCC	Guaranteed Limit			
Symbol Parameter	Test Condi	Test Conditions		25°C to -55°C	≤85°C	≤125°C	Unit	
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0  l <sub>out</sub>   ≤20 μA	0.1 V	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0  I <sub>out</sub>   ≤20 μA	0.1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
VOH	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	14 17 20	Vin=VIH or VIL	I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	7-4 vil	Vin=VIH or VIL	$ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	(F) 12F(F)
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedar Vin = VIL or VIH Vout = VCC or GND	nce State	6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

#### AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

	Visitors Committee Committee			Guaranteed Limit			
Symbol	Parameter		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)		2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPLH, tPHL	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)		2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	C Packager	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	(C Padkage) seemid (DIP) mode to the	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 5)	convended O 1950 12690	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	2,487	W 200 m	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Im State)	pedance	-	15	15	15	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Latch)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	A-
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	41 17 910991	pF

	DOUBLE DOUBLE OF DOUBLE STORY		Gua	aranteed Li	mit	podwing
Symbol	Parameter VIA-00V is VIA	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Input D to Latch Enable (Figure 4)	2.0 4.5 6.0	25 5 5	30 6 6	40 8 7	ns
t <sub>h</sub>	Minimum Hold Time, Latch Enable to Input D (Figure 4)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t <sub>W</sub>	Minimum Pulse Width, Latch Enable (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### SWITCHING WAVEFORMS

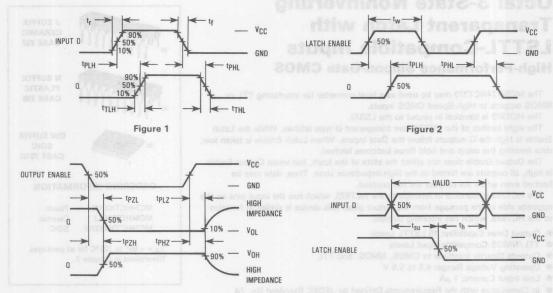
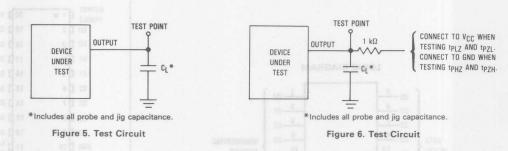
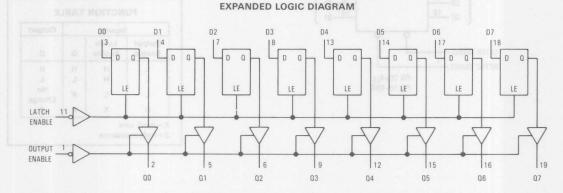


Figure 3

Figure 4





## Octal 3-State Noninverting Transparent Latch with LSTTL-Compatible Inputs

High-Performance Silicon-Gate CMOS

The MC54/74HCT373 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT373 is identical in pinout to the LS373.

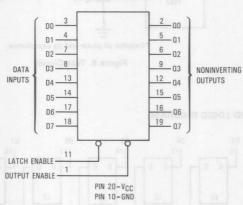
The eight latches of the HCT373 are transparent D-type latches. While the Latch Enable is high the Q outputs follow the Data Inputs. When Latch Enable is taken low, data meeting the setup and hold times becomes latched.

The Output Enable does not affect the state of the latch, but when Output Enable is high, all outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HCT373 is identical in function to the HCT573, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT533, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 186 FETs or 46.5 Equivalent Gates

#### LOGIC DIAGRAM



## MC54/74HCT373



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



DW SUFFIX SOIC CASE 751D

#### ORDERING INFORMATION

MC74HCTXXXN MC54HCTXXXJ MC74HCTXXXDW Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT

OUTPUT	[1 ·	20 VCC
	<b>C</b> 2	19 07
D0	<b>G</b> 3	18 07
D1	<b>C</b> 4	17 D D6
01	<b>C</b> 5	16 0 06
02	<b>G</b> 6	15 🖸 05
D2	7	14 D D5
D3	<b>C</b> 8	13 D D4
03	<b>D</b> 9	12 04
GND	10	11 LATCH ENABLE

#### **FUNCTION TABLE**

Inputs			Output
Output Enable	Latch Enable	D	a
L	Н	Н	Н
L	. н	L	L
L	L	X	No Change
Н	X	X	Z

X = don't care Z = high impedance

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND  $\leq$  (V<sub>in</sub> or V<sub>out</sub>)  $\leq$  V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Gua	-		
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out}$ =0.1 V or $V_{CC}$ -0.1 V $ I_{out}  \le 20 \mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	0.8	0.8 0.8	0.8	V
Vон	VOH Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0$ mA	4.5	3.98	3.84	3.70	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1	٧
	81 X1	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=V <sub>CC</sub> or GND	5.5	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	5.5	±0.5	± 5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0 μA	5.5	8	80	160	μΑ

ΔICC	Additional Quiescent Supply	Vin = 2.4 V, Any One Input		≥ -55°C	25°C to 125°C	
	Current	Vin = VCC or GND, Other Inputs	0.0	\$1		
	100	$I_{out} = 0 \mu A$	5.5	2.9	2.4	

1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

#### MC54/74HCT373

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5.0 V ±10%, C<sub>L</sub>=50 pF, Input t<sub>r</sub>=t<sub>f</sub>=6 ns)

	Parameter V of 2.0 - 10M		Guaranteed Limit		
Symbol			≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	35	44	53	ns
tPLH, tPHL	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	35	44	53	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	35	44	53	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	35	44	53	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 5)	12	15	18	ns
Cin	Maximum Input Capacitance	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High-Impedance Sta	te) 15	15	15	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

  2. Information on typical parametric values can be found in Chapter 4.

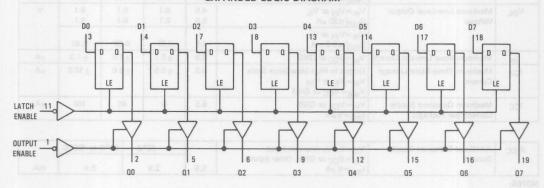
CPD	Power Dissipation Capacitance (Per Latch)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	ANGERO OPERATION COMBUST OFFI	
	PD = CPD VCC2f+ICC VCC	65	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

#### TIMING REQUIREMENTS ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ , Input $t_r = t_f = 6 \text{ ns}$ )

	an   000   0	Gua	Guaranteed Limit			
Symbol	Parameter	25°C to -55°C	≤85°C	≤125°C	Unit	
t <sub>su</sub>	Minimum Setup Time, Input D to Latch Enable (Figure 4)	last augustion (10 Tell	13	15	ns	
th	Minimum Hold Time, Latch Enable to Input D (Figure 4)	10	13	15	ns	
tw	Minimum Pulse Width, Latch Enable (Figure 2)	16	20	24	ns	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### **EXPANDED LOGIC DIAGRAM**



#### SWITCHING WAVEFORMS

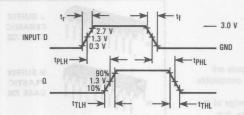


Figure 1

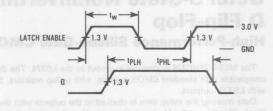


Figure 2

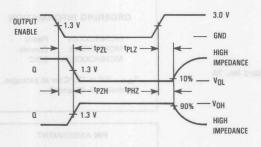


Figure 3

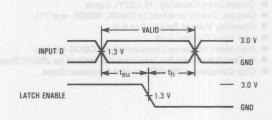
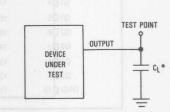


Figure 4



\*Includes all probe and jig capacitance.

TEST POINT CONNECT TO VCC WHEN 1 kΩ OUTPUT TESTING tPLZ AND tPZL. DEVICE CONNECT TO GND WHEN UNDER CL\* TESTING tPHZ AND tPZH. TEST

5

Figure 6. Test Circuit

\*Includes all probe and jig capacitance.

Figure 5. Test Circuit

## Octal 3-State Noninverting D Flip-Flop

### **High-Performance Silicon-Gate CMOS**

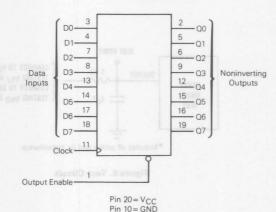
The MC54/74HC374 is identical in pinout to the LS374. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data meeting the setup time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state; thus, data may be stored even when the outputs are not enabled.

The HC374 is identical in function to the HC574, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HC534, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates

#### LOGIC DIAGRAM



## MC54/74HC374



#### ORDERING INFORMATION

MC74HCXXXN Plastic MC54HCXXXJ Ceramic MC74HCXXXDW SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT Output Enable 1 • 20 VCC 19 07 0002 D0 13 18 D7 D104 17 D6 16 06 01 45 15 Q5 02 06 D2 0 7 14 D5 D3 08 13 D4 Q3 [9 12 04 11 Clock GND (10

281 (81	Inputs		Output
Output Enable	Clock	D	a
L		Н	Н
L		L	L
L	L, H, ~	×	no change
Н	X	X	Z

#### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 35	mA
Icc	DC Supply Current, VCC and GND Pins	± 75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	and the state of	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	d to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Guaranteed Limit			I DMI
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V	2.0	1.5	1.5	1.5	V
lan -	Voltage	I <sub>out</sub>   ≤20 μA	4.5 6.0	3.15 4.2	3.15 4.2	3.15 4.2	412
VIL	Maximum Low-Level Input	V <sub>Out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V	2.0	0.3	0.3	0.3	V
en	Voltage	I <sub>out</sub>   ≤20 μA	4.5 6.0	0.9	0.9	0.9	rit <sup>0</sup>
Vон	Minimum High-Level Output	Vin=VIH or VIL	2.0	1.9	1.9	1.9	V
80	Voltage	I <sub>out</sub>   ≤20 μA	4.5 6.0	4.4 5.9	4.4 5.9	4.4 5.9	100
	200 77 30	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0$ mA $ I_{out}  \le 7.8$ mA		3.98 5.48	3.84 5.34	3.70 5.20	1
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0$ mA $ I_{out}  \le 7.8$ mA		0.26 0.26	0.33 0.33	0.40 0.40	GHU L
lin	Maximum Input Leakage Current	Vin=Vcc or GND	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	6.0	±0.5	±5.0	± 10.0	μА
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (C1 = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	Value Unit This device contains		Gua	mit	locimy	
Symbol	Parameter Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
fmax	Maximum Clock Frequency (50% Duty Cycle)	2.0	6.0	4.8	4.0	MHz
perpi me	(Figures 1 and 4)	4.5	30	24	20	- All
northmen.	t-rigin and of separtes	6.0	35	28	24	
tPLH,	Maximum Propagation Delay, Clock to Q	2.0	180	225	270	ns
tPHL	(Figures 1 and 4)	4.5	36	45	54	2001
	DIRE 250 INW SINGS SIVE OF Visit	6.0	31	38	46	0.4
tPLZ,	Maximum Propagation Delay, Output Enable to Q	2.0	150	190	225	ns
tPHZ	(Figures 2 and 5)	4.5	30	38	45	cate 7
	30 to Unite States and an an all all and an an an all all and an	6.0	26	33	38	1
tPZL,	Maximum Propagation Delay, Output Enable to Q	2.0	150	190	225	ns
tPZH	(Figures 2 and 5)	4.5	30	38	45	
-	to the disease rate seems.	6.0	26	33	38	mumin
tTLH,	Maximum Output Transition Time, Any Output	2.0	60	75	90	ns
tTHL	(Figures 1 and 4)	4.5	12	15	18	pailed
		6.0	10	13	15	
Cin	Maximum Input Capacitance	01_260	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	-	15	15	15	pF

#### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	- 83
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	40 (T sup(4)	pF

TIMING REQUIREMENTS (Input  $t_r = t_f = 6$  ns)

Symbol	Office Parameter	VCC	Guaranteed Limit			ladany
			25°C to	≤85°C	≤125°C	Unit
W	1 Y ar Veg - 0.1 V ar	D=dwaV	-55°C	500°€	≤ 125°C	BIV
t <sub>su</sub>	Minimum Setup Time, Data to Clock	2.0	100	125	150	ns
	(Figure 3)	4.5	20	25	30	
	1 V or V oc - 0.1 V or V oc - 0.1 V or V oc - 0.1 V oc V oc -	6.0	17	21	26	JIV
th	Minimum Hold Time, Clock to Data	2.0	25	30	40	ns
	(Figure 3)	4.5	5	6	8	
V	or Vit. 2.0 1.9 1.9 1.0	6.0	5	6	7	RO
tw	Minimum Pulse Width, Clock	2.0	80	100	120	ns
	(Figure 1)	4.5	16	20	24	
	100 Mg (Spurit st 6.0 mA 6.6 3.06 3.06 9.70	6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	2.0	1000	1000	1000	ns
	(Figure 1) 1.0 0.3 0.3 0.3 0.3 0.3 0.3 0.3 0.3 0.3 0	4.5	500	500	500	103
	3 pA 0.1 0.1 0.5	6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### SWITCHING WAVEFORMS

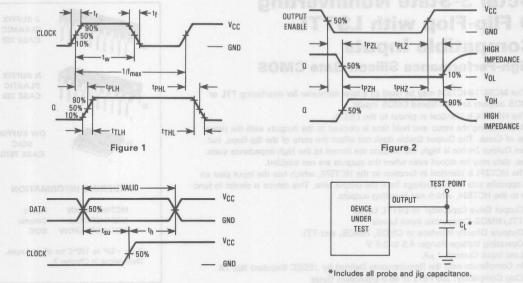


Figure 3

Figure 4. Test Circuit

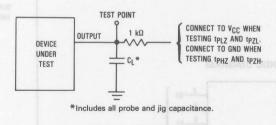
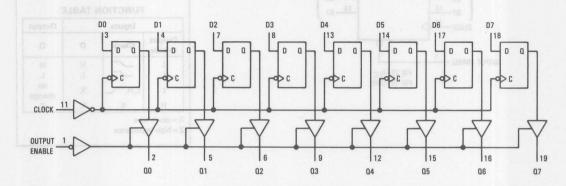


Figure 5. Test Circuit

#### **EXPANDED LOGIC DIAGRAM**



## **Octal 3-State Noninverting** D Flip-Flop with LSTTL-**Compatible Inputs**

**High-Performance Silicon-Gate CMOS** 

The MC54/74HCT374 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT374 is identical in pinout to the LS374.

Data meeting the setup and hold time is clocked to the outputs with the rising edge of Clock. The Output Enable does not affect the state of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HCT374 is identical in function to the HCT574, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT534, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates

## MC54/74HCT374



J SUFFIX CERAMIC **CASE 732** 



N SUFFIX PLASTIC **CASE 738** 



DW SUFFIX SOIC CASE 751D

#### **ORDERING INFORMATION**

MC74HCTXXXN MC54HCTXXXJ MC74HCTXXXDW SOIC

Plastic Ceramic

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

PIN ASSIGNMENT

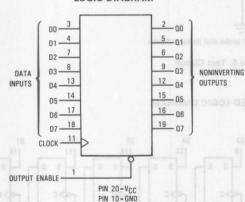
[10	20 VCC
<b>C</b> 2	19 07
<b>Q</b> 3	18 07
<b>d</b> 4	17 D6
<b>C</b> 5	16 06
6	15 05
<b>C</b> 7	14 05
<b>C</b> 8	13 D4
<b>Q</b> 9	12 04
<b>C</b> 10	11 CLOCK
	C 2 C 3 C 4 C 5 C 6 C 7 C 8 C 9

#### **FUNCTION TABLE**

10	Inputs 00		
Output Enable	Clock	D	Q
L	_	Н	Н
L	-	L	L
L	L,H,	X	no change
н	X	X	Z

X = don't care Z = high impedance

#### LOGIC DIAGRAM



#### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	3-82-		-	Guaranteed Limit			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>   ≤20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	٧
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	0.8	0.8	0.8 0.8	٧
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	٧
	age 4-2.	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	٧
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	5.5	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	5.5	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 µA	5.5	8	80	160	μΑ

ΔICC	Additional Quiescent Supply	V <sub>in</sub> =2.4 V, Any One Input		≥ -55°C	25°C to 125°C	
	Current	$V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0 \mu A$	5.5	29	2.4	mA

#### NOTES:

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5.0 V ± 10%, C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	This design contains		Value		Guaranteed Limit		
	egation offets digit of out	Parameter		25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequence (Figures 1 and 4)	y (50% Duty Cycle)	(CIMD of	30	24	20	MHz
tPLH, tPHL	Maximum Propagation Del (Figures 1 and 4)	ay, Clock to Q		35	44	53	ns
tPLZ, tPHZ	Maximum Propagation Del (Figures 2 and 5)	ay, Output Enable to Q	SPIC or Caramir DIPE	35	44	53	ns
tPZL, tPZH	Maximum Propagation Del (Figures 2 and 5)	ay, Output Enable to Q		35	44	53	ns
tTLH, tTHL	Maximum Output Transition (Figures 1 and 4)	n Time, Any Output	IP of SOIC Pactaget	12	15	18	ns
Cin	Maximum Input Capacitan	ce		10	10	10	pF
Cout	Maximum Three-State Out	put Capacitance (Output in High-	mpedance State)	15	15	15	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	MOOR
	Used to determine the no-load dynamic power consumption:	- Parameter 1	Symbo
	PD = CPD Vcc <sup>2</sup> f+Icc Vcc For load considerations, see Chapter 4 subject listing on page 4-2.	100 Supply Villen (Referenced to OMD)	pF

# TIMING REQUIREMENTS (V<sub>CC</sub>=5.0 V $\pm$ 10%, Input t<sub>r</sub>=t<sub>f</sub>=6 ns)

		Gua			
Symbol	Parameter (CMS) or bearmann appeal of	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Data to Clock (Figure 3)	20	25	30	ns
y th	Minimum Hold Time, Clock to Data (Figure 3)	5	5	5	ns
t <sub>W</sub>	Minimum Pulse Width, Clock (Figure 1)	16	20	24	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

# MC54/74HCT374

### SWITCHING WAVEFORMS OUTPUT - 3.0 V ENABLE GND CLOCK ← tpzL tPLZ -HIGH IMPEDANCE 10%\_ - tPLH tPHL -- tPZH tPHZ -> VOH 1.3 V 90% XITIO III 10% HIGH - tTLH **tTHL** IMPEDANCE

Figure 1

Figure 2

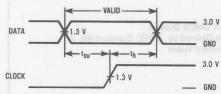


Figure 3

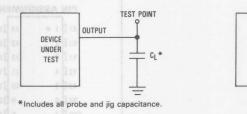


Figure 4. Test Circuit

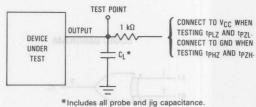
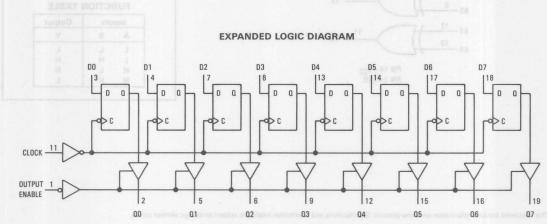


Figure 5. Test Circuit





MOTOROLA HIGH-SPEED CMOS LOGIC DATA

# Advance Information

# **Quad 2-Input Exclusive OR Gate High-Performance Silicon-Gate CMOS**

The MC54/74HC386 is identical in pinout to the LS386. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs

The HC386 is identical in function to the HC86, but has a different pin assignment.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 µA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 56 FETs or 14 Equivalent Gates

# MC54/74HC386



LSUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC **CASE 646** 



D SUFFIX SOIC CASE 751A

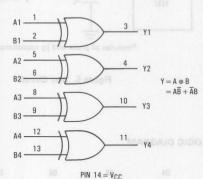
# ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD

Plastic Ceramic SOIC

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# LOGIC DIAGRAM



PIN 7 = GND

# \_\_\_\_

PIN	ASSI	GNM	ENT
A1 [	1 •	14	vcc
B1 [	2	13	] B4
Y1 [	3	12	1 A4
Y2 [	4	11	1 Y4
A2 [	5	10	<b>1</b> Y3
B2 [	6	9	] B3
GND [	7	8	1 A3

# **FUNCTION TABLE**

Inpu	its	Output
А	В	Υ
L	L	L
L	Н	Н
Н	L	Н
H	Н	L

This document contains information on a new product. Specifications and information herein are subject to change without notice

# MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	10 V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	00°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused

outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Ngote 2. Test Circuit			Man	Guaranteed Limit			
Symbol	mbol Parameter Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit		
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -  I <sub>out</sub>   ≤20 μA	-0.1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
VOH Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V	
		Vin=VIH or VIL	I <sub>out</sub>   ≤4.0 mA  I <sub>out</sub>   ≤5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
	Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40		
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

# AC ELECTRICAL CHARACTERISTICS (C1 = 50 pF, Input tr = tf = 6 ns)

Symbol	This device contains				Guaranteed Limit			London & B
	due to high static voltages	Parameter 100 4 of 6.04		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Dela (Figures 1 and 2)	, Input A or B to Output Y		2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
tTLH, tTHL	Maximum Output Transition (Figures 1 and 2)	Time, Any Output	1910 sim	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	008	. Inguae	DIOB	10	10	10	pF

# NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	- Place 199 - 10 million Burn B	
	PD = CPD VCC <sup>2</sup> f+ICC VCC	33	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	man Several Contract of the second Service o	

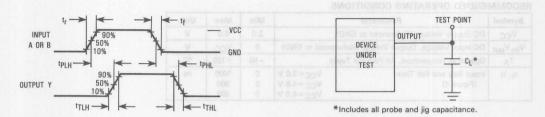
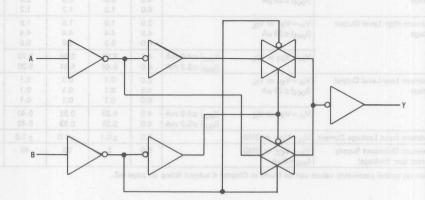


Figure 1. Switching Waveforms

Figure 2. Test Circuit

# EXPANDED LOGIC DIAGRAM (% of the Device Shown)



# Dual 4-Stage Binary Ripple Counter with ÷ 2 and ÷ 5 Sections

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC390 is identical in pinout to the LS390. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five section. The divide-by-two and divide-by-five counters have separate clock inputs, and can be cascaded to implement various combinations of  $\div 2$  and/or  $\div 5$  up to a  $\div 100$  counter.

Flip-flops internal to the counters are triggered by high-to-low transitions of the clock input. A separate, asynchronous reset is provided for each 4-bit counter. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or strobes except when gated with the Clock of the HC390.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 244 FETs or 61 Equivalent Gates

# Clock A 1, 15 ÷ 2 Counter 3, 13 QA Clock B 4, 12 ÷ 5 Counter 6, 10 QC Counter 7, 9 QD Pin 16 = V<sub>CC</sub> Pin 8 = GND

# MC54/74HC390



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

# **ORDERING INFORMATION**

MC74HCXXXN MC54HCXXXJ MC74HCXXXD

Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# PIN ASSIGNMENT

Clock Aa	1 •	16	VCC
Reset a	2	15	Clock Ab
Q <sub>Aa</sub> r	3	14	Reset b
Clock Ba	4	13	QAb
Q <sub>Ba</sub> t	5	12	Clock Bb
Q <sub>Ca</sub>	6	11	1 QBb
QDat	7	10	1 QCb
GND	8	9	QDb

# **FUNCTION TABLE**

Clock		
A B	Reset	Action
× ×	H ogsalo	Reset ÷ 2 and ÷ 5
X	L	Increment ÷ 2
X \	L reparded	Increment ÷ 5

# **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND  $\leq$  (V<sub>in</sub> or V<sub>out</sub>)  $\leq$  V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to	GND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (	Referenced to GND)	0	Vcc	٧
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
tr, tf	Input Rise and Fall Time	V <sub>CC</sub> =2.0 V	0	1000	ns
799	(Figure 1)	V <sub>CC</sub> = 4.5 V	0	500	
	PIRI ASSIGNM	$V_{CC} = 6.0 \text{ V}$	0	400	

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Parameter			V	Guaranteed Limit			
Symbol		Test Condi	tions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0  I <sub>out</sub>   ≤20 μA	0.1 V	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V or } V_{\text{CC}} = 0.1$	).1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	60 11.6	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
- Sea A	2560	Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
S == namerani		Vin=VIH or VIL	$ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

Symbol	OUTPUTS		Gua	PUTS		
	AD — 04, 15) — 0, Perameter   0, 0, 0, 0, 11) = 0, 15, 16, 17, 18, 10, 11) = 0, 16, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle)	2.0	5.4	4.4	3.6	MH
	(Figures 1 and 3)	4.5 6.0	27 32	22 26	18 21	a month
tPLH,	Maximum Propagation Delay, Clock A to QA	2.0	120	150	180	ns
tPHL	(Figures 1 and 3)	4.5 6.0	24 20	30 26	36 31	ni Jša
tPLH,	Maximum Propagation Delay, Clock A to QC (QA connected to Clock B)	2.0	290	365	435	ns
<sup>t</sup> PHL		4.5 6.0	58 49	73 62	87 74	
tPLH,	Maximum Propagation Delay, Clock B to QB	2.0	130	165	195	ns
<sup>t</sup> PHL		4.5 6.0	26 22	33	39 33	
tPLH,	Maximum Propagation Delay, Clock B to QC	2.0	185	230	280	ns
tPHL	(Figures 1 and 3)	4.5 6.0	37 31	46 39	56 48	
tPLH,	Maximum Propagation Delay, Clock B to QD	2.0	130	165	195	ns
<sup>t</sup> PHL	(Figures 1 and 3)	4.5 6.0	26 22	33 28	39 33	
tPHL	Maximum Propagation Delay, Reset to any Q	2.0	165	205	250	ns
	(Figures 2 and 3)	4.5 6.0	33 28	41 35	50 43	
tTLH,	Maximum Output Transition Time, Any Output	2.0	75	95	110	ns
tTHL	(Figures 1 and 3)	4.5	15	19	22	
	7 8 70	6.0	13	16	19	
Cin	Maximum Input Capacitance	-	10	10	10	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Counter)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	35	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

### TIMING REQUIREMENTS (Input to = te = 6 ns)

		V <sub>CC</sub>	Gua	mit	1-7	
Symbol	Parameter agreement to the selection also report		25°C to -55°C	≤85°C	≤125°C	Unit
trec	Minimum Recovery Time, Reset Inactive to Clock A or Clock B (Figure 2)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t <sub>W</sub>	Minimum Pulse Width, Clock A, Clock B (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

# PIN DESCRIPTIONS

### **INPUTS**

CLOCK A (PINS 1, 15) and CLOCK B (PINS 4, 15) -Clock A is the clock input to the ÷ 2 counter; Clock B is the clock input to the ÷5 counter. The internal flip-flops are toggled by high-to-low transitions of the clock input.

# **CONTROL INPUTS**

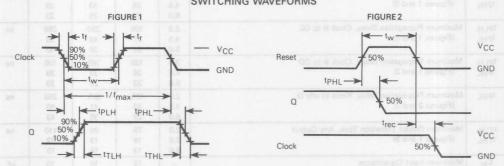
RESET (PINS 2, 14) - Asynchronous reset. A high at the Reset input prevents counting, resets the internal flip-flops, and forces QA through QD low.

# OUTPUTS

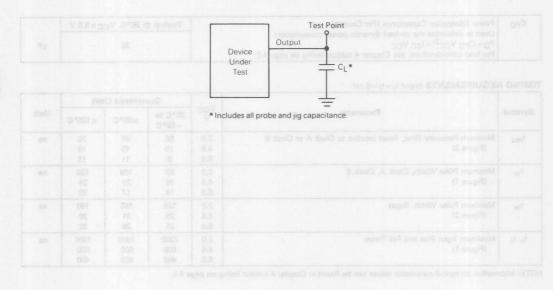
QA (PINS 3, 13) - Output of the ÷ 2 counter.

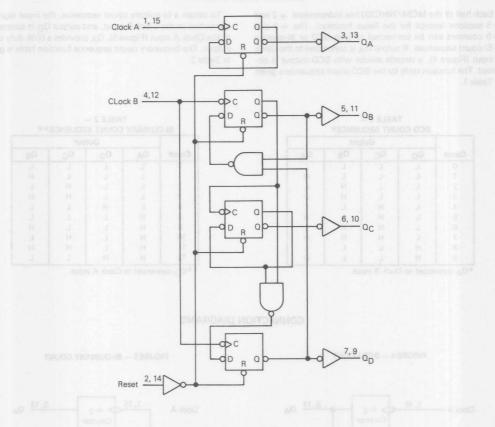
QB, QC, QD (PINS 5, 6, 7, 9, 10, 11) - Outputs of the ÷ 5 counter. Qp is the most significant bit. QA is the least significant bit when the counter is connected for BCD output as in Figure 4. QB is the least significant bit when the counter is operating in the bi-quinary mode as in Figure 5.



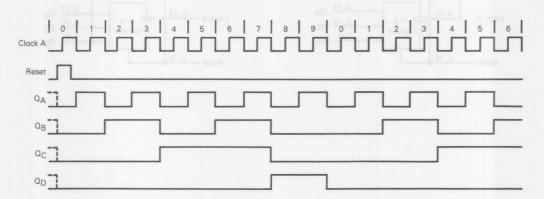


# FIGURE 3 — TEST CIRCUIT





TIMING DIAGRAM (QA Connected to Clock B)



# APPLICATIONS INFORMATION

Each half of the MC54/74HC390 has independent  $\div$  2 and  $\div$  5 sections (except for the Reset function). The  $\div$  2 and  $\div$  5 counters can be connected to give BCD or bi-quinary (2-5) count sequences. If output  $Q_A$  is connected to the Clock B input (Figure 4), a decade divider with BCD output is obtained. The function table for the BCD count sequence is given in Table 1.

To obtain a bi-quinary count sequence, the input signal is connected to the Clock B input, and output Q<sub>D</sub> is connected to the Clock A input (Figure 5). Q<sub>A</sub> provides a 50% duty cycle output. The bi-quinary count sequence function table is given in Table 2.

TABLE 1 — BCD COUNT SEQUENCE\*

	Output					
Count	QD	QC	QB	QA		
0	L	L	L	L		
1	L	L	L	Н		
2	L	L	Н	L		
3	L	L	Н	Н		
4	L	Н	L	L		
5	L	Н	ar L	Н		
6	L	H of	H	L		
7	L	Н	Н	Н		
8	Н	L	L	L		
9	Н	L	L	Н		

<sup>\*</sup>QA connected to Clock B input.

TABLE 2 —
BI-QUINARY COUNT SEQUENCE\*\*

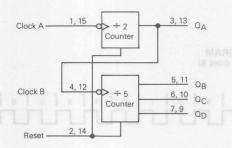
	Output					
Count	QA	QD	QC	QB		
0	L	L	L	L		
1	L	L	L	Н		
2	L	L	Н	L		
3	L	L	Н	Н		
4	L	Н	L	L		
8	Н	L	L	L		
9	H	L	L	H		
10	Н	L	Н	L		
11	Н	L	Н	Н		
12	Н	Н	L	L		

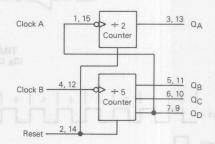
<sup>\*\*</sup>QD connected to Clock A input.

# CONNECTION DIAGRAMS

FIGURE 4 - BCD COUNT

FIGURE 5 - BI-QUINARY COUNT





# Dual 4-Stage Binary Ripple Counter

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC393 is identical in pinout to the LS393. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 4-bit binary ripple counters with parallel outputs from each counter stage. A  $\div$  256 counter can be obtained by cascading the two binary counters.

Internal flip-flops are triggered by high-to-low transitions of the clock input. Reset for the counters is asynchronous and active-high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC393.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 236 FETs or 59 Equivalent Gates

# MC54/74HC393



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

# ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# PIN ASSIGNMENT

# FUNCTION TABLE

Inpu	its	Outnote
Clock	Reset	Outputs
X	Н	L
Н	L	No Change
O lagal syo	throughouse.	No Change
_	- selfing-A	No Change
~	L	Advance to Next State

### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \le (V_{in} \text{ or } V_{out}) \le VCC$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Refe	renced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	21 01, 42 12			Gua	imit	100	
Symbol	Parameter Test Conditions	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
1	H X	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{Out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
March 5 to		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	± 1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 µA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	Parameter		Guaranteed Limit			
Symbol			25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0 4.5 6.0	5.4 27 32	4.4 22 26	3.6 18 21	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to Q1 (Figures 1 and 3)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
tPLH, tPHL	Maximum Propagation Delay, Clock to Q2 (Figures 1 and 3)	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
tPLH, tPHL	Maximum Propagation Delay, Clock to Q3 (Figures 1 and 3)	2.0 4.5 6.0	240 48 41	300 60 51	360 72 61	ns
tPLH, tPHL	Maximum Propagation Delay, Clock to Q4 (Figures 1 and 3)	2.0 4.5 6.0	290 58 49	365 73 62	435 87 74	ns
<sup>t</sup> PHL	Maximum Propagation Delay, Reset to any Q (Figures 2 and 3)	2.0 4.5 6.0	165 33 28	205 41 35	250 50 43	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	-	10	10	10	pF

### NOTES:

For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
 Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Counter)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC	40	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	Trans.	

# TIMING REQUIREMENTS (Input to = 14 = 6 ns)

	Parameter	.,	Gua	mit		
Symbol		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t <sub>W</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>W</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

# PIN DESCRIPTIONS

### INPLITS

CLOCK (PINS 1, 13) — Clock input. The internal flip-flops are toggled and the counter state advances on high-to-low transitions of the clock input.

separate reset is provided for each counter. A high at the Reset input prevents counting and forces all four outputs low.

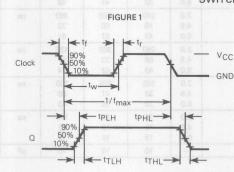
# CONTROL INPUTS

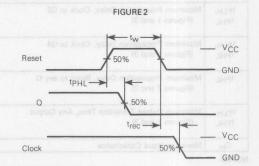
RESET (PINS 2, 12) - Active-high, asynchronous reset. A

# OUTPUTS

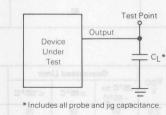
Q1, Q2, Q3, Q4 (PINS 3, 4, 5, 6, 8, 9, 10, 11) - Parallel binary outputs. Q4 is the most significant bit.

# SWITCHING WAVEFORMS

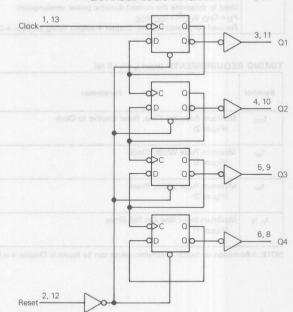




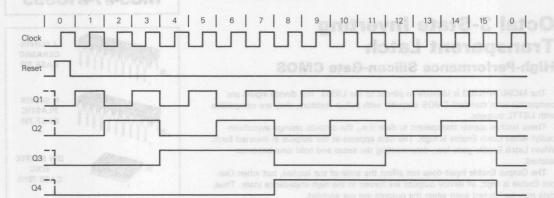
# FIGURE 3 - TEST CIRCUIT



# EXPANDED LOGIC DIAGRAM







# COUNT SEQUENCE

	Outputs					
Count	Q4	Q3	02	01		
0	A[ .01	insignment and	L	YOL		
1	L	L	L	Н		
2	L	L	Н	L		
3	L	L	Н	Н		
4	L	Н	L	L		
5	L	Н	L	Н		
6	L	Н	Н	L		
7	L	Н	Н	Н		
8	Н	L	L	L		
9	Н	L	L	H		
10	Н	L	Н	L		
11	Н	L	H	Н		
12	Н	Н	L	L		
13	Н	Н	L	Н		
14	Н	Н	H	L		
15	Н	Н	Н	H		

# Octal 3-State Inverting Transparent Latch

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC533 is identical in pinout to the LS533. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

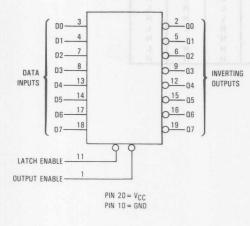
These latches appear transparent to date (i.e., the outputs change asynchronously) when Latch Enable is high. The data appears at the outputs in inverted form. When Latch Enable goes low, data meeting the setup and hold time becomes latched

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

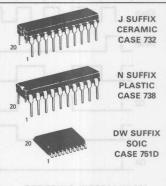
The HC533 is identical in function to the HC563, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HC373, which has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 256 FETs or 64 Equivalent Gates

# LOGIC DIAGRAM



# MC54/74HC533



# ORDERING INFORMATION

MC74HCXXXN Plastic MC54HCXXXJ Ceramic MC74HCXXXDW SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

			1
OUTPUT ENABLE	1 •	20	vcc
00 [	2	19	<b>1</b> 07
D0 [	3	18	D7
D1 [	4	17	D6
01 [	5	16	06
02 [	6	15	05
D2 [	7	14	D5
D3 [	8	13	D4
03 [	9	12	04
GND [	10	11	LATCH ENABLE

Inputs			Output
Output Enable	Latch Enable	D	۵
L	Н	Н	L
L	Н	L	Н
L	L	×	no change
Н	X	X	Z

X = don't care Z = high impedance

# MAXIMUM BATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND≤(Vin or Vout)≤VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)			6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)			Vcc	V
TA	Operating Temperature, All Package Types			+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V	0	1000 500	ns
		$V_{CC} = 6.0 V$	0	400	

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

		Test Conditions		Gua	aranteed L	imit Dall	IN DAM	
Symbol	Parameter			25°C to -55°C	≤85°C	≤125°C	Unit	
VIH	Minimum High-Level Input	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V	2.0	1.5	1.5	1.5	٧	
en	Voltage	l <sub>out</sub>   ≤20 μA	4.5 6.0	3.15 4.2	3.15 4.2	3.15 4.2		
VIL	Maximum Low-Level Input	V <sub>out</sub> =0.1 V or V <sub>CC</sub> - 0.1 V	2.0	0.3	0.3	0.3	V	
90	Voltage	I <sub>out</sub>   ≤20 μA	4.5 6.0	0.9	0.9	0.9		
Vон	Minimum High-Level Output	Vin=VIH or VIL	2.0	1.9	1.9	1.9	V	
en	Voltage	l <sub>out</sub>   ≤20 μA	4.5 6.0	4.4 5.9	4.4 5.9	4.4 5.9		
	17 20	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20		
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V chal cit	
	72-6	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0$ mA $ I_{out}  \le 7.8$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40		
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
loz	Maximum Three-State Leakage Current			±0.5	±5.0	± 10.0	μА	
Icc	Maximum Quiescent Supply Current (per Package)	Vin=VCC or GND Iout=0 µA	6.0	8	80	160	μА	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

	п	

	This davice contains				Guaranteed Limit			todaye
Symbol	circuitry to guerd againt	Parameter 6.7 + m 3.0-		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tpLH, Maximum Propagation Delay, tpHL (Figures 1 and 5)	Input D to Q		2.0	150 30	190 38	225 45	ns	
sambegn	SAMPLE AND SHIP OF SECURIOR			6.0	26	33	38	
tPLH,	Maximum Propagation Delay,	Latch Enable to Q		2.0	175	220	265	ns
tPHL	(Figures 2 and 5)			4.5	35	44	53	
SACC	range GWD ± (Vip or Vous SVCC)	VVm UST	7910 pinns	6.0	30	37	45	09
tPLZ,	PLZ, Maximum Propagation Delay,	Output Enable to Q	Factuager	2.0	150	190	225	ns
tPHZ (Figures 3 and 6)			4.5	30	38	45		
			6.0	26	33	38		
tPZL,	Maximum Propagation Delay,	Output Enable to Q	(egnolos <sup>e</sup> )	2.0	150	190	225	ns
tPZH	(Figures 3 and 6)			4.5	30	38	45	
		device may accur.	eris of som	6.0	26	33	38	reumica
tTLH,	Maximum Output Transition 1	ime, Any Output	O betreen	2.0	60	75	90	ns
<sup>t</sup> THL	(Figures 1 and 5)			4.5	12	15	18	
		2005	6.0	10	113 :91	15		
Cin	Maximum Input Capacitance		D*65	61_583	10	10	10	pF
Cout	Maximum Three-State Output State)	Capacitance (Output in High-Imp	edance	EXAMPLE S	15	15	15	pF

### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

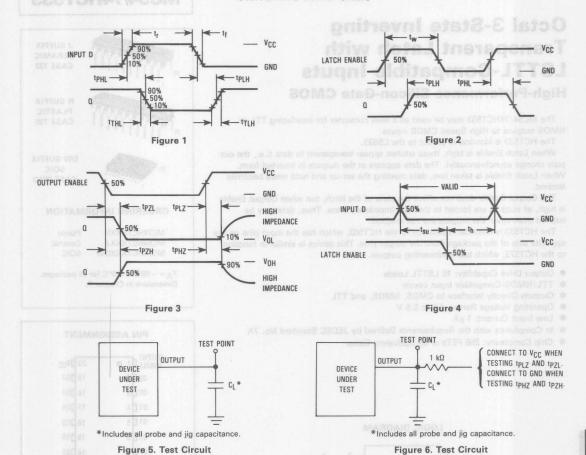
CPD	Power Dissipation Capacitance (Per Latch)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	SISTER BOTH THIS BUILT SHIPE	
	PD=CPD VCC2f+ICC VCC	41	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

# TIMING REQUIREMENTS (Input tr = tf = 6 ns)

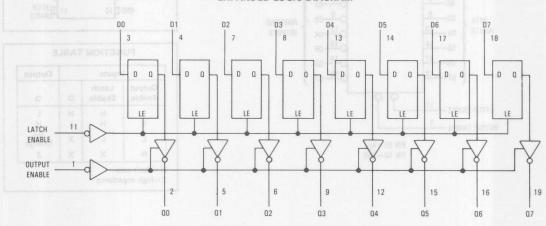
	Test Conditions U 25°C to 485°C 4185°C		Guaranteed Limit			lodmy8
Symbol	Parameter 8.1 8.1 8.1 9.1 9.1 9.1 9.1 9.1 9.1 9.1 9.1 9.1 9	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Input D to Latch Enable (Figure 4)	2.0 4.5	25 5	30 6	40 8	ns
	1 V or Vcc - 0.3 V to - 0.3 V to - 0.3	6.0	5	6	7	
th	Minimum Hold Time, Latch Enable to Input D (Figure 4)	2.0 4.5	50 10	65 13	75 15	ns
	0 Vn 2.0 1.9 1.9 1.9	6.0	9	3 11 10 I	13	
t <sub>w</sub>	Minimum Pulse Width, Latch Enable (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

# SWITCHING WAVEFORMS



# **EXPANDED LOGIC DIAGRAM**



MOTOROLA HIGH-SPEED CMOS LOGIC DATA

# Octal 3-State Inverting Transparent Latch with LSTTL-Compatible Inputs

# **High-Performance Silicon-Gate CMOS**

The MC54/74HCT533 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT533 is identical in pinout to the LS533.

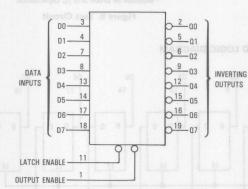
When Latch Enable is high, these latches appear transparent to data (i.e., the outputs change asynchronously). The data appears at the outputs in inverted form. When Latch Enable is taken low, data meeting the set-up and hold times becomes latched.

The Output Enable does not affect the state of the latch, but when Output Enable is high, all outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HCT533 is identical in function to the HCT563, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT373, which has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 256 FETs or 64 Equivalent Gates

# LOGIC DIAGRAM



PIN  $20 = V_{CC}$ PIN 10 = GND

# MC54/74HCT533



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



DW SUFFIX SOIC CASE 751D

# ORDERING INFORMATION

MC74HCTXXXN MC54HCTXXXJ MC74HCTXXXDW

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# PIN ASSIGNMENT

OUTDUT		
OUTPUT ENABLE C	1.	20 VCC
00 🖸	2	19 107
D0 [	3	18 07
D1 C	4	17 006
01	5	16 06
02	6	15 05
D2 [	7	14 005
D3 🖸	8	13 🗆 🗆 🗆
03	9	12 04
GND C	10	11 DLATCH ENABL

# **FUNCTION TABLE**

Inputs		Output	
Output Enable	Latch Enable	D	a
L	Н	Н	L
L	Н	L	Н
L	T.	×	No Change
Н	X	X	Z

X = don't care Z = high impedance

# 5

# **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
<sub>en</sub> T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
tr, tf	Input Rise and Fall Time (Figure 1)	0	500	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	0 0 0	O tus		Guaranteed Limit			39
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	٧
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	0.8	0.8	0.8	٧
VOH	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	
VOL	Maximum Low-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	4.5 5.5	0.1 0.1	0.1	0.1 0.1	V
	passeng passeng p	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0$ mA	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=Vcc or GND	5.5	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	5.5	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 µA	5.5	8	80	160	μА

ΔICC	Additional Quiescent Supply	Vin=2.4 V, Any One Input	9 1	≥ -55°C	25°C to 125°C	
	Current	Vin = VCC or GND, Other Inputs	100			
		I <sub>out</sub> =0 μA	5.5	2.9	2.4	m

### NOTES:

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

# MC54/74HCT533

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5.0 V ±10%, C<sub>L</sub>=50 pF, Input t<sub>f</sub>=t<sub>f</sub>=6 ns)

i pamaqi	Value Unit This device contain		Guaranteed Limit			dmyä
Symbol	Parameter of 3.0	(GMS) of	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	(CMD) or	35	44	53	ns
tPLH, tPHL	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)		35	44	53	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	Ushic or Ceramio DIPT	35	44	53	ns
tPZL,	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	TSEATH DICK	35	44	53	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 5)	Jame for 10 Seconds 31P or 801C Perkings)	12	15	18	ns
Cin	Maximum Input Capacitance	True services	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High	n-Impedance State)	15	15	15	pF

### NOTES

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

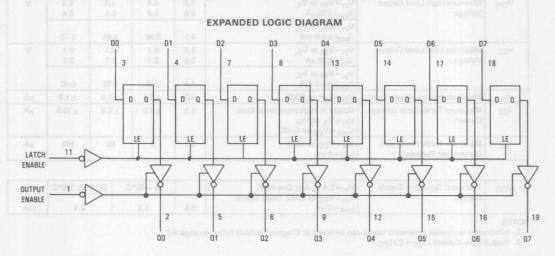
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Latch)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	IOITIC MOD BINITARIAGO DECIMENM	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	of Paramage	flyeni

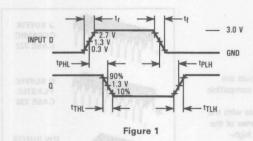
TIMING REQUIREMENTS ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ , Input  $t_r = t_f = 6 \text{ ns}$ )

Symbol	0 1 00 00 000	Gu	Guaranteed Limit		181
	Parameter	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Input D to Latch Enable (Figure 4)	20	25	30	ns
th	Minimum Hold Time, Latch Enable to Input D (Figure 4)	5	6	8	ns
tw	Minimum Pulse Width, Latch Enable (Figure 2)	16 may 1	20	24	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.



# SWITCHING WAVEFORMS



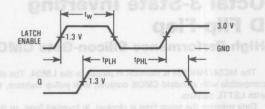
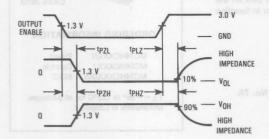


Figure 2



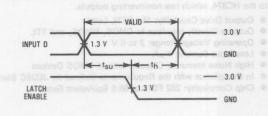
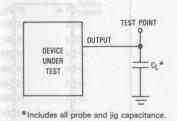


Figure 3

Figure 4



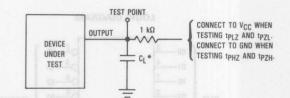


Figure 5. Test Circuit

\* Includes all probe and jig capacitance.



# Octal 3-State Inverting D Flip-Flop

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC534 is identical in pinout to the LS534. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data meeting the setup time is clocked, in inverted form, to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC534 is identical in function to the HC564, which has the input pins on the opposite side of the package from the output pins. The device is similar in function to the HC374, which has noninverting outputs.

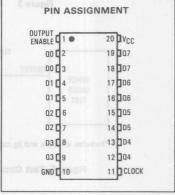
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 282 FETs or 68.5 Equivalent Gates

### LOGIC DIAGRAM D0-**D1** -01 -02 D2--03 DATA D3 INVERTING 012 04 13 INPUTS OUTPUTS D4-05 05 14 17 016 06 D6-18 <u>19</u> 07 D7-11 CLOCK OUTPUT ENABLE -PIN 20 = VCC PIN 10 = GND

# MC54/74HC534



 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.



	Inputs		Output
Output Enable	Clock	D	Q
L		Н	L
L	_	L	Н
L	L,H,~	X	No Change
Н	X	X	Z

# MC54/74HC534

# **MAXIMUM RATINGS\***

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C fugle0 A

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{In}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	est exclutors 8	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	ed to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Parameter		V <sub>CC</sub>	Guaranteed Limit			- amount
Symbol				25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V or V}_{\text{CC}} - 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
an	74 17 26 7000 1000 1000	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	7g, 1g
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V H :BTO
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	± 1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	6.0	±0.5	±5.0	± 10.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

U	E	
1	ŀ	0]

	Value   Link   This device consein		Guaranteed Limit			Sauta B
Symbol	Parameter T G G B B	VCC V	25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	180 36 31	225 45 38	270 54 46	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	45.F et 1/8 <u>0</u> mo	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High-Impedance State)		15	15	15	pF

# NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

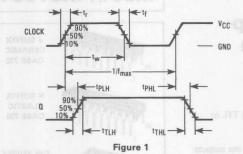
CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	A
	Used to determine the no-load dynamic power consumption:	April me visite uges religion	H M
	PD = CPD Vcc <sup>2</sup> f+Icc Vcc For load considerations, see Chapter 4 subject listing on page 4-2.	40	pF

# TIMING REQUIREMENTS (Input tr=te=6 ns)

	Table 0°382 of 0°48 Parameter Parameter		Guaranteed Limit			Symbol	
Symbol		VCC	25°C to -55°C	≤85°C	≤125°C	Unit	
t <sub>su</sub>	Minimum Setup Time, Data to		2.0	100	125	150	ns
	(Figure 3)		4.5	20	25	30	
	En 1 60 1 60		6.0	17	21	26	
th	Minimum Hold Time, Clock to	Data	2.0	25	30	40	ns
	(Figure 3)		4.5	5	6	8	
8.6	02 02 1 05		6.0	5	6	7	
t <sub>w</sub>	Minimum Pulse Width, Clock	8.4. Au-051	2.0	80	100	120	ns
	(Figure 1)		4.5	16	20	24	
	NC P 56 C 1 28 C		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall 1		2.0	1000	1000	1000	ns
V	(Figure 1)		4.5	500	500	500	
			6.0	400	400	400	

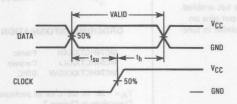
NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

# SWITCHING WAVEFORMS



OUTPUT ENABLE GND tPZL tPLZ-HIGH IMPEDANCE 50% 0 10% **←**tpZH tPHZ -> VOH 50% 0 HIGH IMPEDANCE

Figure 2



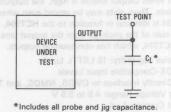


Figure 3

Figure 4. Test Circuit

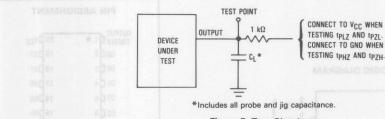
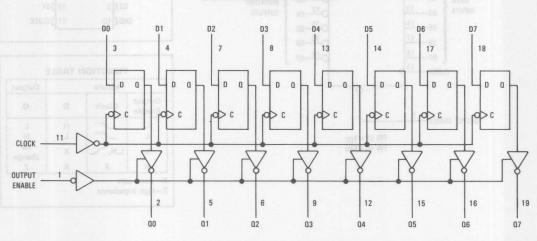


Figure 5. Test Circuit

# **EXPANDED LOGIC DIAGRAM**



# Octal 3-State Inverting D Flip-Flop with LSTTL-Compatible Inputs

# **High-Performance Silicon-Gate CMOS**

The MC54/74HCT534 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT534 is identical in pinout to the LS534.

Data meeting the setup and hold time is clocked, in inverted form, to the outputs with the rising edge of Clock. The Output Enable does not affect the state of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HCT534 is identical in function to the HCT564, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT374, which has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 229 FETs or 57 Equivalent Gates

# MC54/74HCT534



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



DW SUFFIX SOIC CASE 751D

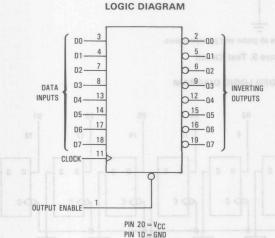
# ORDERING INFORMATION

MC74HCTXXXN MC54HCTXXXJ MC74HCTXXXDW

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### Well-man Shirt course



# PIN ASSIGNMENT

OUTPUT C	1 •	20 DV <sub>CC</sub>
0.0	2	19 07
00	3	18 <b>D</b> D7
010	4	17 <b>D</b> D6
01	5	16 106
02	6	15 05
D2 C	7	14 DD5
D3 <b>C</b>	8	13 D4
03 🖸	9	12 04
GND C	10	11 CLOC
D3 C	8	13 D4 12 D4

### FUNCTION TADI

	FUNCTION	I IABL	.E	
4 - 8	Inputs			
Output Enable	Clock	D	Q	
L	5	H	L H	
L	L,H,	X	no change	
Н	×	X	Z	

X = don't care Z = high impedance

# MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
ICC	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	٧
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Parameter		Man	Guaranteed Limit			- UES
Symbol		Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	0.8	0.8	0.8	V
Vон	Minimum High-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V Malai esti
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	
V <sub>OL</sub> Maximum Low-Level Voltage	Maximum Low-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \mu \text{A}$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	٧
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	5.5	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  Vin = VIL or VIH  Vout = VCC or GND	5.5	±0.5	±5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 µA	5.5	8	80	160	μΑ

ΔICC	Additional Quiescent Supply	V <sub>in</sub> =2.4 V, Any One Input		≥ -55°C	25°C to 125°C	
	Current	Vin=VCC or GND, Other Inputs				
		$I_{out} = 0 \mu A$	5.5	2.9	2.4	mA

### NOTES:

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5.0 V ±10%, C<sub>L</sub>=50 pF, Input t<sub>f</sub>=t<sub>f</sub>=6 ns)

	This sleving compine			Gua	ranteed L	imit	
Symbol	due to high static voltages	Parameter - WANG-	GND)	25°C to -55°C	≤85°C	≤125°C	Unit
fmax	Maximum Clock Frequency (Figures 1 and 4)	(50% Duty Cycle)	(OMO)	25	31	38	MHz
tPLH, tPHL	Maximum Propagation Dela (Figures 1 and 4)	y, Clock to Q		35	44	53	ns
tPLZ, tPHZ	Maximum Propagation Dela (Figures 2 and 5)	y, Output Enable to Q	1919 ammin DIP1	35	44	53	ns
tPZL, tPZH	Maximum Propagation Dela (Figures 2 and 5)	y, Output Enable to Q		35	44	53	ns
tTLH, tTHL	Maximum Output Transition (Figures 1 and 4)	Time, Any Output	ea for 111 Seronds P or SDIC Package)	12	15	18	ns
Cin	Maximum Input Capacitance	Landa de la companya	Tind omidated	10	10	10	pF
Cout	Maximum Three-State Outp	ut Capacitance (Output in High-In	npedance State)	15	15	15	pF

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

   Information on typical parametric values can be found in Chapter 4.

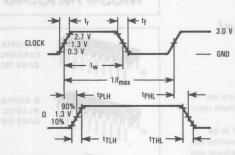
CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	сомп
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC	attempted 65	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	UC Supply Verlage Likelyeneed to GN	nov

TIMING REQUIREMENTS ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ , Input  $t_r = t_f = 6 \text{ ns}$ )

Symbol		Gu	Guaranteed Limit		4
	Parameter 40M2 or business	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Data to Clock (Figure 3)	10	13	15	ns
th	Minimum Hold Time, Clock to Data (Figure 3)	5	5	5	ns
tw	Minimum Pulse Width, Clock (Figure 1)	A-(05)=1004 16	20	24	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	Au os a moli 500	500	500	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.





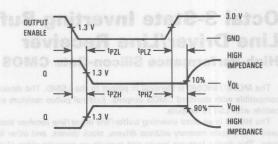
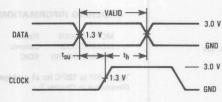


Figure 1

Figure 2



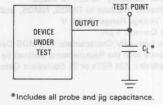


Figure 3

Figure 4. Test Circuit

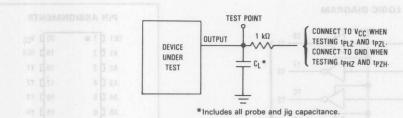
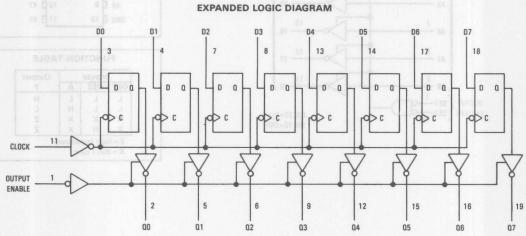


Figure 5. Test Circuit



# **Octal 3-State Inverting Buffer/** Line Driver/Line Receiver

**High-Performance Silicon-Gate CMOS** 

The MC54/74HC540 is identical in pinout to the LS540. The device inputs are compatible with standard CMOS outputs. External pullup resistors make them compatible with LSTTL outputs.

The HC540 is an octal inverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

The HC540 is similar in function to the HC541, which has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 124 FETs or 31 Equivalent Gates

# MC54/74HC540



J SUFFIX CERAMIC **CASE 732** 



N SUFFIX PLASTIC **CASE 738** 



DW SUFFIX SOIC CASE 751D

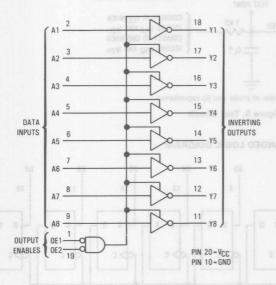
# ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ

Ceramic MC74HCXXXDW SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# LOGIC DIAGRAM



# **PIN ASSIGNMENTS**

[10	20 VCC
2	19 D OE2
<b>Q</b> 3	18 Y1
<b>d</b> 4	17 Y2
<b>C</b> 5	16 73
6	15 Y4
7	14 75
8	13 76
<b>Q</b> 9	12 Y7
<b>C</b> 10	11 Y8
	1 • 2 2 3 4 4 5 5 6 6 7 7 8 8 9 0 110

# **FUNCTION TABLE**

	Inputs		Output
OE1	OE2	Α	Y
L	L	L	Н
L	L	Н	L
HS	X	X	Z
X	Н	X	Z

Z = high impedance X = don't care

Symbol	Mimild bestrone Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter			Max	Unit
Vcc	DC Supply Voltage (Referenced	to GND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	. V
TA	Operating Temperature, All Package Types			+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

		OE on one 2		, J la	Guaranteed Limit		imit	
Symbol	Parameter	Test Cond	litions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V  I <sub>out</sub>   ≤20 μA	HMI THE	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =V <sub>CC</sub> -0.1 V  I <sub>out</sub>  ≤20 μA	KETS-	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH Minimum High-Level Output Voltage		$V_{in} = V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V <sub>in</sub> = V <sub>IL</sub>	$ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
ON GOV OF	THE THE COMMEC	Vin=VIH	$ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
d <sub>in</sub>	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  Vin = VIL or VIH  Vout = VCC or GND		6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

# AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

	This device contains				Gua	aranteed L	imit	depyth
Symbol	circuitry to guero agail	Parameter 1.1 + ca 8.0 -		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, (Figures 1 and 3)	Input A to Output Y or A (IIII		2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tPLZ, tPHZ	Maximum Propagation Delay, (Figures 2 and 4)	Output Enable to Output Y	1 PSIO bimine	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPZL, tPZH	Maximum Propagation Delay, (Figures 2 and 4)	Output Enable to Output Y	Tauston C	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tTLH, tTHL	Maximum Output Transition (Figures 1 and 3)	Time, Any Output	C Package) araquic DIP)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	anothbroContinue	aO bebooning	boll-belt	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Outpu State)	t Capacitance (Output in High-	Impedance	169°-10 1	15	n 01 15 910	15	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD Vcc <sup>2</sup> f+Icc Vcc	OC Input Volate Dutput Volume IRefe	ρF
	For load considerations, see Chapter 4 subject listing on page 4-2.	Operant of Temperature, All Facilings Tyr	AT

# SWITCHING WAVEFORMS

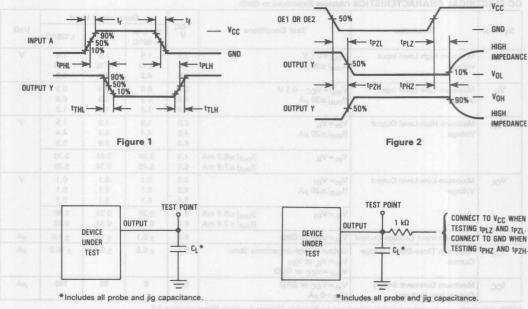


Figure 3. Test Circuit

Figure 4. Test Circuit

# **PIN DESCRIPTIONS**

# **INPUTS**

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9) — Data input pins. Data on these pins appear in inverted form on the corresponding Y outputs, when the outputs are enabled.

# CONTROLS

OE1, OE2 (PINS 1, 19) — Output enables (active-low). When a low voltage is applied to both of these pins, the outputs

are enabled and the device functions as an inverter. When a high voltage is applied to either input, the outputs assume the high impedance state.

### OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) — Device outputs. Depending upon the state of the output enable pins, these outputs are either inverting outputs or high-impedance outputs.

# LOGIC DETAIL

TO SEVEN OTHER INVERTERS

NOTAMINOTAL DATE OF EIGHT INVERTERS

ONE OF EIGHT INVERTERS

ONE OF EIGHT INVERTERS

OUTPUT

TO SEVEN OTHER INVERTER

## Octal 3-State Inverting Buffer/ Line Driver/Line Receiver with LSTTL-Compatible Inputs

**High-Performance Silicon-Gate CMOS** 

The MC54/74HCT540 is identical in pinout to the LS540. This device may be used as a level converter for interfacing TTL or NMOS to High-Speed CMOS inputs.

The HCT540 is an octal inverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

The HCT540 is similar in function to the HCT541, which has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 164 FETs or 41 Equivalent Gates

## MC54/74HCT540



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



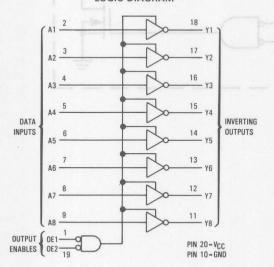
DW SUFFIX SOIC CASE 751D

#### ORDERING INFORMATION

MC74HCTXXXN MC54HCTXXXJ MC74HCTXXXDW Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENTS

10	20 V <sub>C</sub>	C
2	19 0	2
<b>Q</b> 3	18 Y1	
<b>Q</b> 4	17 Y2	
<b>C</b> 5	16 Y3	}
6	15 Y4	
7	14 75	i
<b>D</b> 8	13 Y6	
<b>d</b> 9	12 Y7	
D 10	11 Y8	
	☐ 1 • ☐ 2 ☐ 3 ☐ 4 ☐ 5 ☐ 6 ☐ 7 ☐ 8 ☐ 9 ☐ 10 ☐ 10	C 2 19 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

#### **FUNCTION TABLE**

	Inputs		Output
OE1	OE2	Α	Υ
L	L	L	Н
L	L	Н	L
Н	X	X	Z
X	Н	X	Z

Z = high impedance X = don't care

## 5

#### MAXIMUM RATINGS\*

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	٧
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

		projection X-350		Guaranteed Limit			a Tropie
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out}$ =0.1 V or $V_{CC}$ -0.1 V $ I_{out}  \le 20 \mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	0.8	0.8	0.8	٧
Vон	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	٧
Gifter gold to cost OMA ex	YOURSES SET DOS	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	5.5	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or $V_{IH}$ $V_{out} = V_{CC}$ or GND	5.5	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	5.5	8	80	160	μΑ

ΔICC	Additional Quiescent Supply	V <sub>in</sub> =2.4 V, Any One Input		≥ -55°C	25°C to 125°C	
	Current	Vin = VCC or GND, Other Inputs				
		I <sub>out</sub> =0 μA	5.5	2.9	2.4	mA

#### NOTES:

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

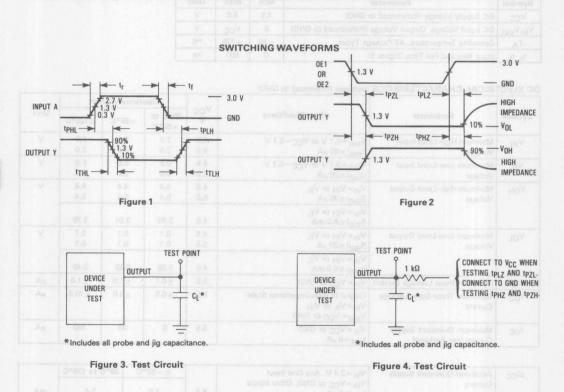
Functional operation should be restricted to the Recommended Operating Conditions.

	entermo entreta entitivada entre entreta entre		Gua	Indime		
Symbol			25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	GND)	30	38	45	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)		35	44	53	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	) Place No de Cecarnio Di	45	56	68	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	lessed thros	12	15	18	ns
Cin	Maximum Input Capacitance	se for 10 Second	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High-Imped	ance State)	15	15	15	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	High son
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC	50	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	MENDED OPERATING CONDITIONS	MMOORE



#### PIN DESCRIPTIONS

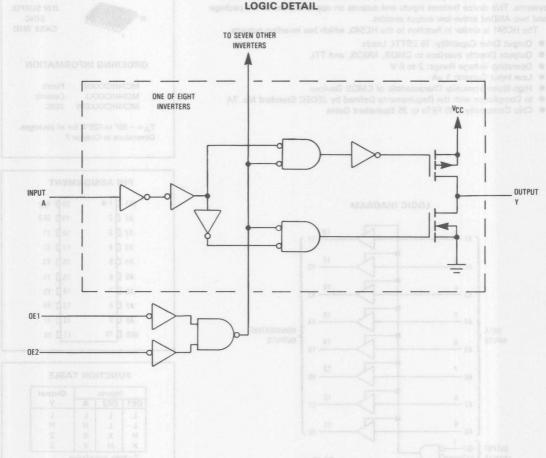
A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9) - Data input pins. Data on these pins appear in inverted form on the corresponding Y outputs, when the outputs are enabled.

#### CONTROLS

OE1, OE2 (PINS 1, 19) — Output enables (active low). When a low level is applied to both of these pins, the outputs are enabled and the device functions as an inverter. When a high level is applied to either input, the outputs assume the high impedance state.

#### **OUTPUTS**

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) - Device outputs. Depending upon the state of the output-enable pins, these outputs are either inverting outputs or high impedance outputs.



## Octal 3-State Noninverting Buffer/Line Driver/Line Receiver High-Performance Silicon-Gate CMOS

The MC54/74HC541 is identical in pinout to the LS541. The device inputs are compatible with standard CMOS outputs. External pullup resistors make them compatible with LSTTL outputs.

The HC541 is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

The HC541 is similar in function to the HC540, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 140 FETs or 35 Equivalent Gates

## LOGIC DIAGRAM 18 17 16 15 NONINVERTING DATA 14 13 Y6 12 11 OUTPUT | OE1-ENABLES 0E2-PIN 20 - VCC PIN 10-GND

## MC54/74HC541

20

J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



DW SUFFIX SOIC CASE 751D

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXDW

Plastic Ceramic

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT

OE1		1 •	20	þ	VCC	
A1		2	19	þ	OE2	
A2		3	18	þ	Y1	
АЗ		4	17	þ	Y2	
A4		5	16	þ	Y3	
A5	q	6	15	þ	Y4	
A6	9	7	14	b	Y5	
A7	q	8	13	Ь	Y6	
A8	d	9	12		Y7	
GND	d	10	11		Y8	

#### **FUNCTION TABLE**

	Inputs	Output	
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	Н
Н	X	X	Z
X	Н	X	Z

Z = high impedance X = don't care

## 5

#### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	A V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package1	750 500	mW
T <sub>stq</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds		°C
an:	(Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{In}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referen	ced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	C.5 on	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

			v. 0	Guaranteed Limit				
Symbol	Parameter	Test Condit	Test Conditions		25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =V <sub>CC</sub> -0.1 V  l <sub>out</sub>  ≤20 μA	(H)	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V  I <sub>out</sub>  ≤20 μA	Jeff	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH Minimum High-Level Output Voltage		V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	Figure 2	V <sub>in</sub> =V <sub>IH</sub>	I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VoL	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
nggi disa sila Baya disa di	V <sub>in</sub> =V <sub>IL</sub>		$ I_{\text{out}}  \le 6.0 \text{ mA}$ $ I_{\text{out}}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedar Vin = VIL or VIH Vout = VCC or GND	nce State	6.0	±0.5	±5.0	± 10.0	μА
lcc	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

			Gua	opmys		
Symbol	Parameter Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, Input A to Output Y	2.0	125	155	190	ns
tPHL	(Figures 1 and 3)	4.5 6.0	25 21	31 26	38 32	
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPZL,	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	noeE.ed	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High-Impedance State)	01 - 01 - 10 02 - 70 07 03 - 000	15	15	15	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	DC Input Voltage, Output Voltage (B.	uoV-oil
	PD = CPD VCc <sup>2</sup> f+ICC VCC For load considerations, see Chapter 4 subject listing on page 4-2.	School BA James Starte Co.	pF

#### **SWITCHING WAVEFORMS**

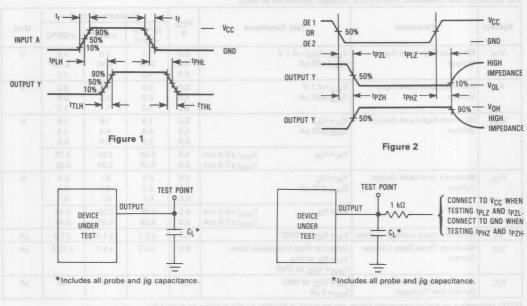


Figure 3. Test Circuit

Figure 4. Test Circuit

#### INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9) — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

#### CONTROLS

OE1, OE2 (PINS 1, 19) — Output enables (active-low). When a low level is applied to both of these pins, the outputs

are enabled and the device functions as a noninverting buffer. When a high level is applied to either input, the outputs assume the high impedance state.

#### OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high impedance outputs.

#### LOGIC DETAIL

# Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT541 is identical in pinout to the LS541. The device may be used as a level converter for interfacing TTL or NMOS to High-Speed CMOS inputs.

The HCT541 is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

The HCT541 is similar in function to the HCT540, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 180 FETs or 45 Equivalent Gates

## MC54/74HCT541



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



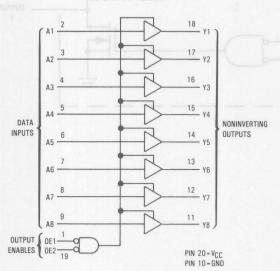
DW SUFFIX SOIC CASE 751D

#### ORDERING INFORMATION

MC74HCTXXXN MC54HCTXXXJ MC74HCTXXXDW Plastic Ceramic

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENTS

OE1	d	1 •	20	þ	VCC
A1	d	2	19	þ	OE2
A2	d	3	18	þ	Y1
А3	d	4	17	þ	Y2
A4	d	5	16	þ	Y3
A5	d	6	15	þ	Y4
A6	d	7	14	þ	Y5
A7	d	8	13	þ	Y6
A8	d	9	12		Y7
GND	d	10	11	þ	Y8

#### **FUNCTION TABLE**

-	Inputs		Output
OE1	OE2	Α	Υ
L	L	L	1
L	L	Н	1 1 3 1 -
H	X	X	Z
X	Н	X	Z

Z = high impedance X = don't care

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
ag <sup>T</sup> L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{\text{In}}$  and  $V_{\text{out}}$  should be constrained to the range GND  $\leq$  ( $V_{\text{in}}$  or  $V_{\text{out}}$ )  $\leq$   $V_{\text{CC}}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### **RECOMMENDED OPERATING CONDITIONS**

**MAXIMUM RATINGS\*** 

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	٧
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Guaranteed Limit			
Symbol	Parameter Test Conditions	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out}$ =0.1 V or $V_{CC}$ -0.1 V $ I_{out}  \le 20 \mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	0.8	0.8	0.8 0.8	V
VOH Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	٧	
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	٧
TWD4. T697		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND	5.5	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	5.5	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	5.5	8	80	160	μΑ

ΔICC	Additional Quiescent Supply	V <sub>in</sub> =2.4 V, Any One Input		≥ -55°C	25°C to 125°C	
	Current	Vin = Vcc or GND, Other Inputs	3331573	STATES OF STATES		
		$I_{out} = 0 \mu A$	5.5	2.9	2.4	mA

#### NOTES:

1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2,

2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

	Velue Unit This device contain		Gua	aranteed Li	mit	
Symbol	Show shall spid of subs	to GND)	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	to GND)	30	38	45	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	10.00	35	44	53	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	1510 signato so size	45	56	68	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)		12	15	18	ns
Cin	Maximum Input Capacitance	stranged of 10 least	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High	-Impedance State)	15	15	15	pF

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC	MENDED DISCLATING CONDITION	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

#### SWITCHING WAVEFORMS

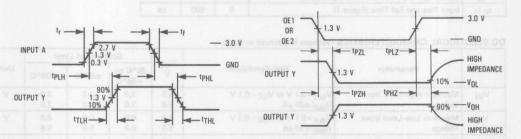
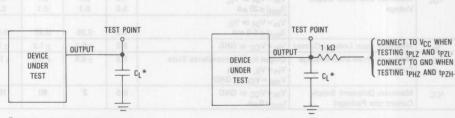


Figure 1

Figure 2



\*Includes all probe and jig capacitance.

\*Includes all probe and jig capacitance.

Figure 3. Test Circuit

Figure 4. Test Circuit

#### PIN DESCRIPTIONS

#### INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9) - Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

#### CONTROLS

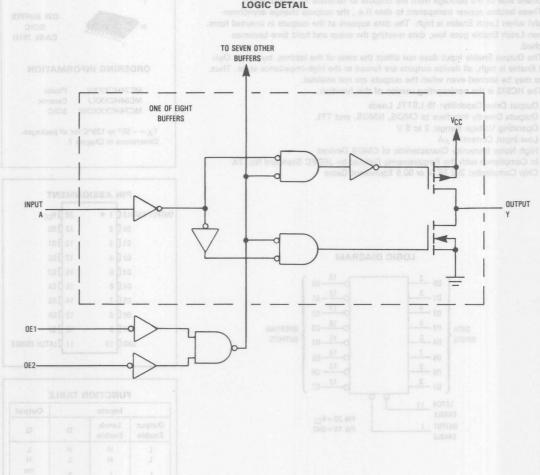
OE1, OE2 (PINS 1, 19) - Output enables (active low). When a low level is applied to both of these pins, the outputs

are enabled and the device functions as a noninverting buffer. When a high level is applied to either input, the outputs assume the high impedance state.

#### **OUTPUTS**

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) - Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high impedance outputs.

#### LOGIC DETAIL



## Octal 3-State Inverting Transparent Latch

**High-Performance Silicon-Gate CMOS** 

The MC54/74HC563 is identical in pinout to the LS563. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is identical in function to the HC533 but has the Data Inputs on the opposite side of the package from the outputs to facilitate PC board layout.

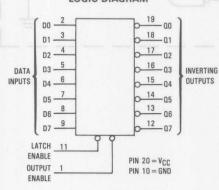
These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. The data appears at the outputs in inverted form. When Latch Enable goes low, data meeting the setup and hold time becomes

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HC573 is the noninverting version of this function.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 202 FETs or 50.5 Equivalent Gates

#### LOGIC DIAGRAM



## MC54/74HC563



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



DW SUFFIX SOIC CASE 751D

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXDW Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT

PIN	ASSI	GNMENT
OUTPUT ENABLE	1 •	20 D VCC
0 00	2	19 00
D1 [	3	18 01
D2 [	4	17 02
D3 [	5	16 03
D4 [	6	15 04
D5 [	7	14 05
D6 [	8	13 1 06
D7 [	9	12 07
GND [	10	11 LATCH ENABLE
	-	

#### **FUNCTION TABLE**

	Inputs		Output
Output Enable	Latch Enable	D	Q
L	Н	Н	L
L	н	L	Н
L	L	X	no change
Н	X	X	Z

X = don't care
Z = high impedance

#### **MAXIMUM RATINGS\***

	III III III III III III III III III II	an district rail June 11 and 12 and 1	
Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD,	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Refer	enced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V	0	1000 500	ns
		V <sub>CC</sub> = 6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

			tan	Gua	Guaranteed Limit		
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V	2.0	1.5	1.5	1.5	V
	Voltage	I <sub>out</sub>   ≤20 μA	4.5 6.0	3.15 4.2	3.15 4.2	3.15 4.2	
VIL	Maximum Low-Level Input	V <sub>Out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V	2.0	0.3	0.3	0.3	V
en	Voltage	I <sub>out</sub>   ≤20 μA	4.5 6.0	0.9	0.9	0.9 1.2	
Vон	Minimum High-Level Output	Vin=VIH or VIL	2.0	1.9	1.9	1.9	V
	Voltage	I <sub>out</sub>   ≤20 μA	4.5 6.0	4.4 5.9	4.4 5.9	4.4 5.9	
	14 17 20	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$		3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	W. Carrie
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	± 10.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	Vin=VCC or GND Iout=0 µA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

	Value Unit Tris device contains pr	.,	Guaranteed Limit			Locient
Symbol	Parameter QXY on 8.0 -	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLH, tPHL	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	7 ST OF 75	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	900	15	15	15	pF

#### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Latch)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	37 (Fadged)	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	3/	

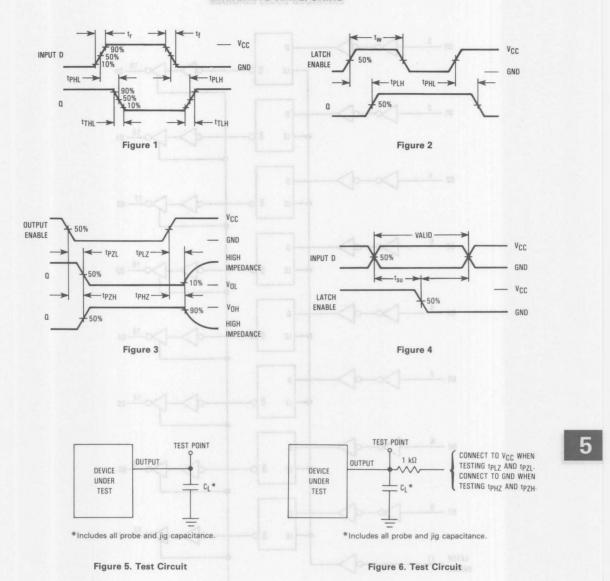
#### TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

	Test Dondillons y 25°C to e8°C < 125°C		Gua	aranteed Li	mit	
Symbol	Parameter 8.1 Parameter 9.1 Pa	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Input D to Latch Enable (Figure 4)	2.0	75 15	95 19	110 22	ns
	Ver Vcc - 0.1 V 2.0 0.3 0.3 0.3	6.0	13	16	19	
th	Minimum Hold Time, Latch Enable to Input D (Figure 4)	2.0 4.5	5 5	5 5	5 5	ns
	et et et 0.5 m/ to	6.0	5 110	5	5	
t <sub>W</sub>	Minimum Pulse Width, Latch Enable (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	2.0	1000	1000	1000	ns
	(Figure 1) 1.0 1.0 0.3 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0	4.5 6.0	500 400	500 400	500 400	

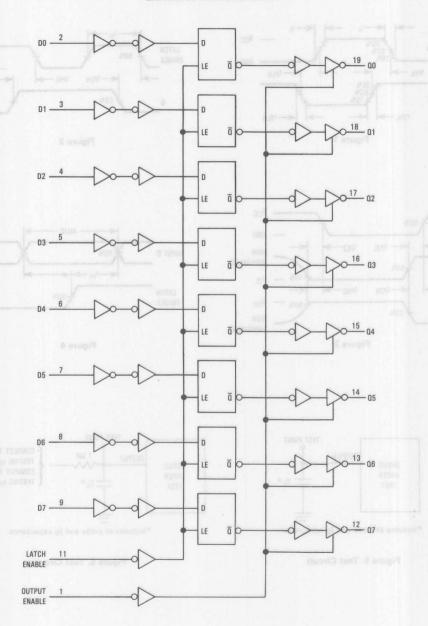
NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### MC54/74HC563

#### **SWITCHING WAVEFORMS**



#### **EXPANDED LOGIC DIAGRAM**



## Octal 3-State Inverting D Flip-Flop High-Performance Silicon-Gate CMOS

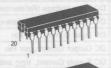
The MC54/74HC564 is identical in pinout to the LS564. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is identical in function to the HC534 but has the flip-flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

Data meeting the setup time is clocked, in inverted form, to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled. The HC564 is the inverting version of the HC574.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 282 FETs or 70.5 Equivalent Gates

## MC54/74HC564



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



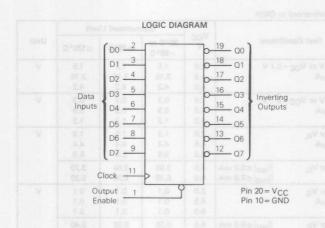
DW SUFFIX SOIC CASE 751D

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXDW

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.



#### PIN ASSIGNMENT

Output Enable	1 •	20 ]	VCC
D0 <b>C</b>	2	19	Q0
D1 <b>C</b>	3	18	Q1
D2 <b>[</b>	4	17 🕽	Q2
D3 [	5	16	Q3
D4 <b>C</b>	6	15	Q4
D5 C	7	14 🕽	Q5
D6 🖸	8	13	Q6
D7 C	9	12	Q7
GND [	10	110	Clock

#### FUNCTION TABLE

	Inputs		Output
Output Enable	Clock	D	Q
L	5	Н	L
L	5	L	Н
y Pass	L,H,~	X	no change
H	X	X	Z

X = don't care Z = high impedance

в	200
L	
К	-

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	٧
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	AT	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GN	ID)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Re	ferenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter		Vcc	Guaranteed Limit			7.5
		Test Conditions		25°C to -55°C	≤85°C	≤125°C	Uni
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
Voн	Minimum High-Level Output Voltage	V <sub>In</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	A PT MOTOWN IN	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
0	Enable Clock D	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	6.0	±0.5	±5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Symbol		Vcc	Gua			
	Parameter		25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	-	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	-	15	15	15	pF

#### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

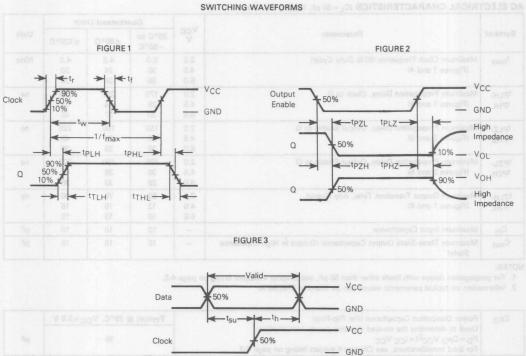
CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	38	pF

TIMING REQUIREMENTS (Input  $t_r = t_f = 6$  ns)

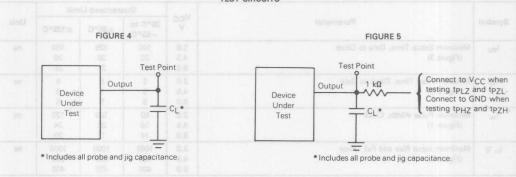
Symbol	Parameter		Gua	imit		
			25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Data to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
nedw Oxi	Minimum Hold Time, Clock to Data (Figure 3)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t <sub>W</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1) The Company of the State	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

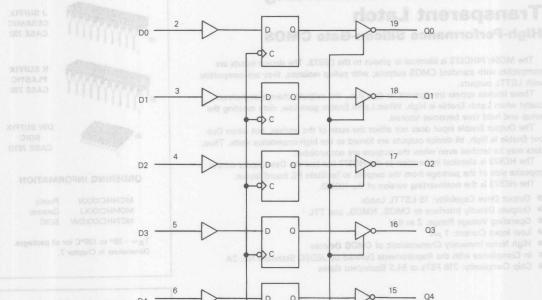


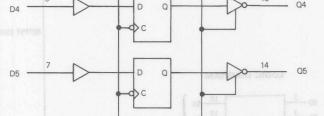


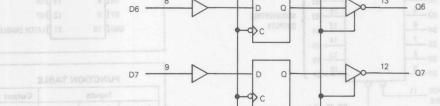
#### TEST CIRCUITS



13







Clock 11
Output 1
Enable

## **Octal 3-State Noninverting Transparent Latch**

### **High-Performance Silicon-Gate CMOS**

The MC54/74HC573 is identical in pinout to the LS573. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

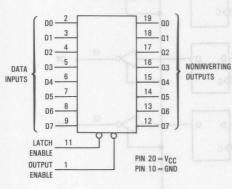
The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HC573 is identical in function to the HC373 but has the Data Inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HC573 is the noninverting version of the HC563.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 218 FETs or 54.5 Equivalent Gates





J SUFFIX CERAMIC **CASE 732** 



N SUFFIX PLASTIC **CASE 738** 



DW SUFFIX SOIC CASE 751D

Ceramic

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXDW SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT OUTPUT ENABLE [ 1 • 20 D VCC 19 00 DO [ 18 0 01 17 02 D2 [ 16 0 03 D3 [ 15 04 D5 [ 14 0 05 13 1 06 D6 D 8 12 07 D7 0 9 11 LATCH ENABLE GND 1 10

### **FUNCTION TABLE**

	Inputs		Output
Output Enable	Latch Enable	D	a
L	н	Н	Н
L	н	L	L
Linde	L	Х	no change
Н	X	X	Z

X = don't care Z = high impedance

#### MAXIMUM RATINGS\*

IAAIIVIO	MI HATINGS"	医女生经历。1300年1000年	原产 法是汇票
Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	of V high
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{In}$  and  $V_{Out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{Out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	and the state of	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types	Operating Temperature, All Package Types		+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V	0	1000 500	ns
		V <sub>CC</sub> = 6.0 V	0	400	100 A 10

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

		Test Conditions		Guaranteed Limit			R DW
Symbol	Parameter		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤20 μA	2.0 4.5	1.5 3.15	1.5 3.15	1.5 3.15	٧
	26 95 570	able 2.9	6.0	4.2	4.2	4.2	
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5	0.3 0.9	0.3 0.9	0.3 0.9	٧
90	8 8 8	0.00	6.0	1.2	1.2	1.2	10
VOH	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0	1.9 4.4	1.9 4.4	1.9 4.4	V
	16 20 24 14 17 20	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	6.0 4.5 6.0	5.9 3.98 5.48	5.9 3.84 5.34	5.9 3.70 5.20	
VoL	Maximum Low-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
	5-6	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	notal :
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	Value Unit Unit device contains		W	Guaranteed Limit			ledary2
Symbol	Parameter 0.5 + cd d.0 -		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, Input D to Q		2.0	175	220	265	ns
tPHL	(Figures 1 and 5)		4.5 6.0	35 30	44 37	53 45	εψ
tPLH, tPHL	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)		2.0 4.5	175 35	220 44	265 53	ns
	780 mW range GVD stVin of Vote	1980 ohs	6.0	30	37	45	109
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)		2.0 4.5	150 30	190 38	225 45	ns
1112	35V to tixto renta , g.al		6.0	26	33	38	
tPZL,	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	(egs/hafi MiG ako	2.0 4.5	150 30	190 38	225 45	ns
	tuppy year ea	ivalb arit or ea	6.0	26	33	38	mumbes
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 5)		2.0	60 12	75 15	90 18	ns
			6.0	10	13	15	
Cin	Maximum Input Capacitance	Unit	67,48	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High- State)	Impedance	01000	15	15	15	pF

#### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

PD	Power Dissipation Capacitance (Per Latch)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	37 (I mugil)	pF
	PD=CPD VCC <sup>2</sup> †+ICC VCC For load considerations, see Chapter 4 subject listing on page 4-2.	3/	

TIMING REQUIREMENTS (Input t<sub>r</sub>=t<sub>f</sub>=6 ns)

Symbol	3°80 ≥ 3°80 ≥ 3°80 Parameter V1.0-55V to V I	V <sub>CC</sub>	Guaranteed Limit			
			25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Input D to Latch Enable	2.0	75	95	110	ns
	(Figure 4)	4.5 6.0	15 13	19 16	22 19	
t <sub>h</sub>	Minimum Hold Time, Latch Enable to Input D (Figure 4)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t <sub>W</sub>	Minimum Pulse Width, Latch Enable (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

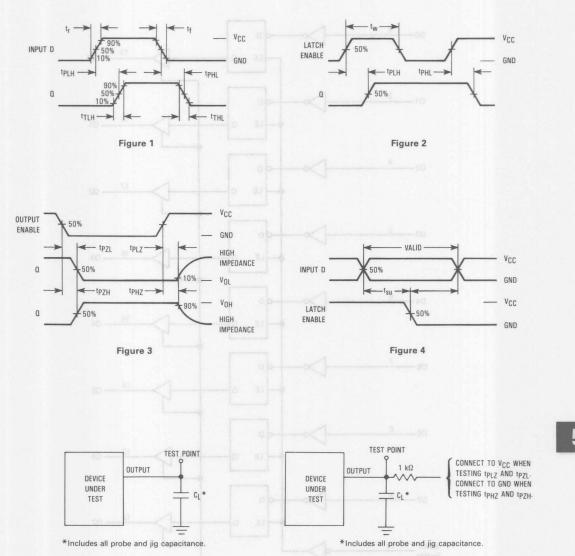
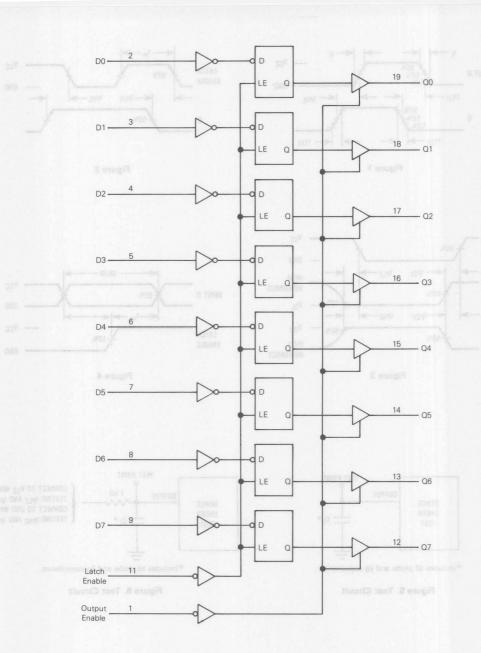


Figure 6. Test Circuit

Figure 5. Test Circuit



## Octal 3-State Noninverting D Flip-Flop

### **High-Performance Silicon-Gate CMOS**

The MC54/74HC574 is identical in pinout to the LS574. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data meeting the setup time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC574 is identical in function to the HC374 but has the flip-flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HC574 is the noninverting version of the HC564.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates

## MC54/74HC574

J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



SOIC CASE 751D

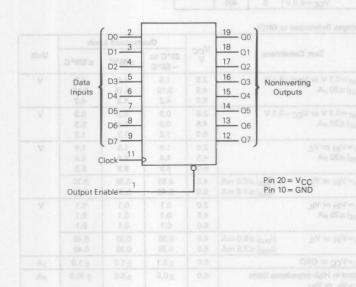
#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXDW

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT

Output Enable 1 1	20 VCC
D0 C 2	19 00
D1 🕻 3	18 🕽 Q1
D2 <b>C</b> 4	17 🖸 Q2
1001 1001 D3 <b>C</b> 5	16 D Q3
D4 <b>C</b> 6	15 Q4
D5 C 7	14 <b>3</b> Q5
D6 C 8	13 🗖 Q6
D7 <b>C</b> 9	12 07
GND [ 10	11 Clock

#### **FUNCTION TABLE**

	Inputs		Output
Output Enable	Clock	D	a
L	5	Н	Н
the great	5	L	nl L
-Side	L,H,~	×	no change
Н	X	X	Z

X = don't care
Z = high impedance

#### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	٧
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	٧
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND≤(Vin or Vout)≤VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	٧
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	/ <sub>CC</sub> =2.0 V / <sub>CC</sub> =4.5 V / <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Car Dick		The state of the s		Gua	aranteed L	imit	
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
ó	Sreble Cinds D	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	6.0	±0.5	±5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

		Vcc	Guaranteed Limit			
Symbol	Parameter		25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL,	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	_	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	-	15	15	15	pF

#### NOTES:

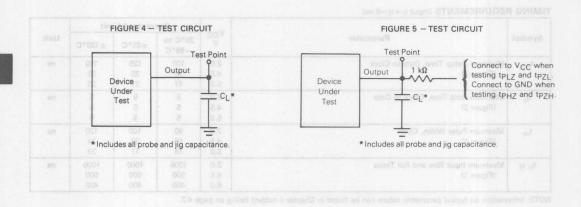
For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
 Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	38	pF

TIMING REQUIREMENTS (Input t -tr-6 ps)

		v. Til	Gua	imit	6	
Symbol	Parameter mod mod	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Data to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Clock to Data (Figure 3)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

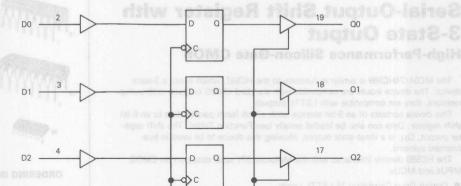
NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.



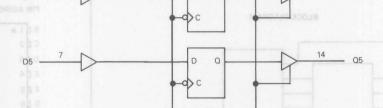
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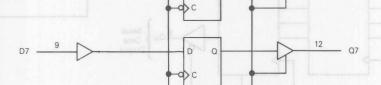




D

Q

Q



D

Clock 11
Output 1
Enable

6

D4 -

D6 -

## 8-Bit Serial- or Parallel-Input/ Serial-Output Shift Register with 3-State Output

## **High-Performance Silicon-Gate CMOS**

The MC54/74HC589 is similar in function to the HC597, which is not a 3-state device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of an 8-bit storage latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table). The shift register output,  $Q_H$ , is a three-state output, allowing this device to be used in busoriented systems.

The HC589 directly interfaces with the Motorola SPI serial data port on CMOS MPUs and MCUs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 526 FETs or 131.5 Equivalent Gates

## MC54/74HC589



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



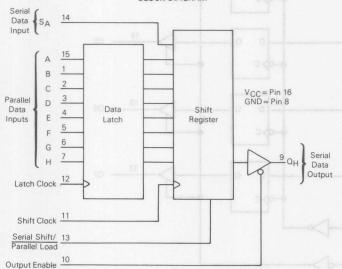
D SUFFIX SOIC CASE 751

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.





#### PIN ASSIGNMENT

В	1 .	16	vcc
C	2	15	<b>A</b>
DI	3	14	SA
E	4	13	Serial Shift/ Parallel Load
F (	5		Latch Clock
G [	6	11	Shift Clock
н	7	10	Output Enable
GND [	8	9	Q <sub>H</sub>

#### MAXIMUM RATINGS\*

AATITO	IN NATINGO"	of A - B - Bracket week	120
Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
81	SOIC Packaget	500	ilan Clack
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter 2.4		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
Vin, Vout	DC Input Voltage, Output Voltage (Reference	ed to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	epolished in	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Typicel (h 28°C, Vgg=5.9 V		(0)	suine9 to	Gua	aranteed Li	imit	
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	VOH Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
		Vin=VIH or VIL	I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
		Vin=VIH or VIL	$ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND		6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

	The second secon		.,	Gua	mit	ladmy		
Symbol				VCC	25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency ( (Figures 2 and 8)	50% Duty Cycle)		2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay (Figures 1 and 8)	, Latch Clock to Q <sub>H</sub>	1910 birts	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
tPLH, tPHL	Maximum Propagation Delay (Figures 2 and 8)	, Shift Clock to QH	Palokagar	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLH, tPHL	Maximum Propagation Delay (Figures 4 and 8)	, Serial Shift/Parallel Load to QH	Racksgall envic (01P)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLZ, tPHZ	Maximum Propagation Delay (Figures 3 and 9)	, Output Enable to Q <sub>H</sub>	mended Op 10 26°C	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
<sup>t</sup> PZL, <sup>t</sup> PZH	Maximum Propagation Delay (Figures 3 and 9)	, Output Enable to Q <sub>H</sub>	SPRC Trapter 4 su	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition (Figures 1 and 8)	Time, Any Output		2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	V Lasy 0 L	CHARLET NO.	marille (i	10	10	10	pF
Cout	Maximum Three-State Outpu State)	t Capacitance (Output in High-Imp	pedance	e Typus	15	15	15	pF

#### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
   Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Used to d	ssipation Cap letermine the VCC <sup>2</sup> f+IC consideration	no-load dy	Typical @ 25°C, V <sub>CC</sub> =5.0 V	loderyd pF		
	2.15 2.15 4.2	3.15 4.2 4.2	0.16 0.16 0.2	6.5	An 052 (100)	Mainten ingerunsel logue. Voltage	FILE
				2:0 4.6 6.0			
		6.83				Current	

TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol			Gu	A I I I		
	Parameter GAGUR LIARASATTRIKS	VCC V	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, A-H to Latch Clock (Figure 5)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>su</sub>	Minimum Setup Time, Serial Data Input S <sub>A</sub> to Shift Clock (Figure 6)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
<sup>t</sup> su	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock (Figure 7)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Latch Clock to A-H (Figure 5)	2.0 4.5 6.0	25 5 5	30 6 6	40 8 7	ns
th	Minimum Hold Time, Shift Clock to Serial Data Input S <sub>A</sub> (Figure 6)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
th	Minimum Hold Time, Shift Clock to Serial Shift/Parallel Load (Figure 7)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t <sub>W</sub>	Minimum Pulse Width, Shift Clock (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>w</sub>	Minimum Pulse Width, Latch Clock (Figure 1)	4.5	80 16 14	100 20 17	120 24 20	ns
t <sub>w</sub> .	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### FUNCTION TABLE

##- bisVateG-#		FU	INCTION	I IABLE		1-4	- Balle V era			
201	Inputs						Resulting Function			
Operation Operation		Serial Shift/ Parallel Load	_	Shift Clock	Serial Input S <sub>A</sub>	Parallel Inputs A-H	Data Latch Contents	Shift Register Contents	Output Q <sub>H</sub>	
Force output into high-impedance state	Н	X	X	X	X	X	X	X	Z	
Load parallel data into data latch	L	Н	_	L, H,~	X	a-h	a-h	U	U	
Transfer latch contents to shift register	L	ExtactD /	L, H,~	X	X	X	U	LRN→SRN	LRH	
Contents of input latch and shift register are unchanged	- L	Н	L, H, ~	L, H, \	X	X	U	U	U	
Load parallel data into data latch and shift register	L	L	1	X	X	a-h	a-h	a-h	h	
Shift serial data into shift register	L	Н	X	1	D	X	*	$SR_A = D;$ $SR_N \rightarrow SR_{N+1}$	SR <sub>G</sub> →SR <sub>H</sub>	
Load parallel data in data latch and shift serial data into shift register	nuda	Н	~	~	D	a-h	a-h	$SR_A = D;$ $SR_N \rightarrow SR_{N+1}$	SR <sub>G</sub> →SR <sub>H</sub>	

LR = latch register contents

SR = shift register contents

a-h = data at parallel data inputs A-H

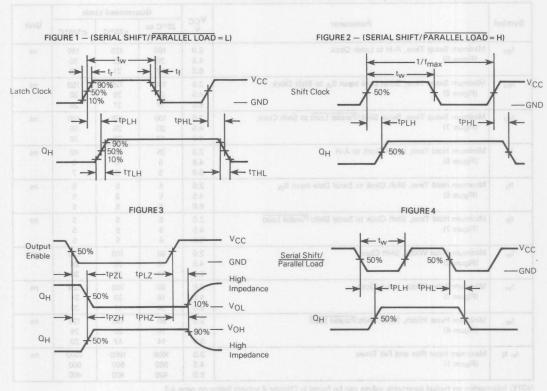
D = data (L, H) at serial data input SA

U = remains unchanged

X = don't care

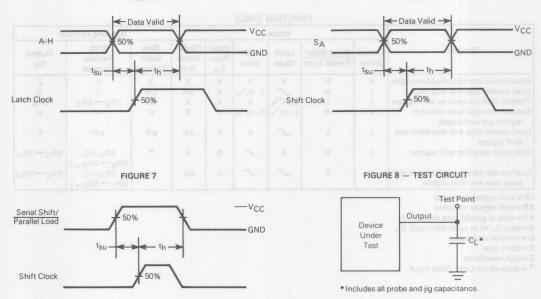
Z = high impedance
\* = depends on Latch Clock input

### SWITCHING WAVEFORMS of the property of the pro



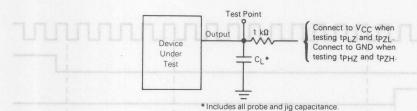
#### FIGURE 5

#### FIGURE 6



J

#### FIGURE 9 - TEST CIRCUIT



#### PIN DESCRIPTIONS

#### DATA INPUTS

A, B, C, D, E, F, G, H (PINS 15, 1, 2, 3, 4, 5, 6, 7) — Parallel data inputs. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.

SA (PIN 14) — Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

#### CONTROL INPUTS

SERIAL SHIFT/PARALLEL LOAD (PIN 13) — Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the data latch.

SHIFT CLOCK (PIN 11) — Serial shift clock. A low-to-high transition on this input shifts data on the serial data input into the shift register and data in stage H is shifted out  $Q_H$ , being replaced by the data previously stored in stage G.

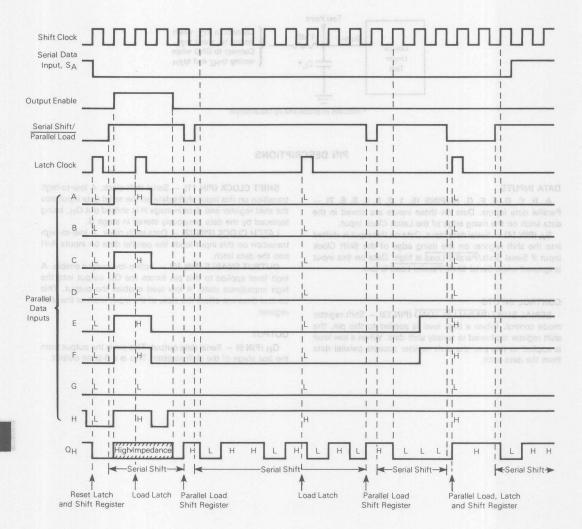
LATCH CLOCK (PIN 12) — Data latch clock. A low-to-high transition on this input loads the parallel data on inputs A-H into the data latch.

OUTPUT ENABLE (PIN 10) — Active-low output enable. A high level applied to this pin forces the Q<sub>H</sub> output into the high impedance state. A low level enables the output. This control does not affect the state of the input latch or the shift register.

#### OUTPUT

 $\rm Q_{H}$  (PIN 9) — Serial data output. This pin is the output from the last stage of the shift register. This is a 3-state output.





5

\*NOTE: Stages C thru G (not shown in detail) are identical to stages A and B above.

# 8-Bit Serial-Input/Serial- or Parallel-Output Shift Register with Latched 3-State Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC595 is identical in pinout to the LS595. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC595 consists of an 8-bit serial shift register and an 8-bit D-type latch with three-state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8-bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

The HC595 directly interfaces with the Motorola SPI serial data port on CMOS MPUs and MCUs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 328 FETs or 82 Equivalent Gates

## MC54/74HC595



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



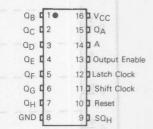
D SUFFIX SOIC CASE 751

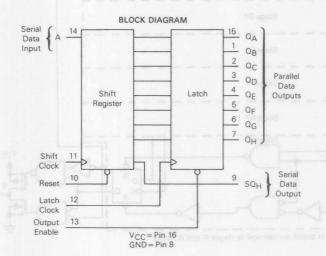
#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT





#### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	٧
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{In}$  and  $V_{Out}$  should be constrained to the range GND  $\leq$  ( $V_{In}$  or  $V_{Out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Ceramic DIP: – 10 mW/°C from 100° to 125°C SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Paramet	er		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced	2.0	6.0	V		
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage	0	Vcc	V		
TA	Operating Temperature, All Paci	Operating Temperature, All Package Types				
tr, tf	Input Rise and Fall Time	4.5	V <sub>CC</sub> =2.0 V	0	1000	ns
	(Figure 1)		V <sub>CC</sub> =4.5 V	0	500	
	230 205 205		V <sub>CC</sub> =6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	25 220 255	2.0	V	Gua	11443		
Symbol	Parameter Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit	
VIH	Minimum High-Level Input Voltage $V_{\text{Out}} = 0.1 \text{ V or V}_{\text{CC}} = 0.1 \text{ V}$ Voltage $ I_{\text{Out}}  \leq 20 \ \mu\text{A}$			1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
V <sub>IL</sub>	Maximum Low-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V or } V_{\text{CC}} = 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu\text{A}$		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	Minimum High-Level Output Voltage, Q <sub>A</sub> -Q <sub>H</sub>	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
87	80 25 80 12 16 18 10 18 16	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	AHIT
V <sub>OL</sub>	Maximum Low-Level Output Voltage, Q <sub>A</sub> -Q <sub>H</sub>	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
Tig II	01 01 50	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	

5

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Symbol	Parameter	Test Conditions		25°C to -55°C	≤85°C	≤125°C	Unit
VOH Minimum High-Level Output Voltage, SQH		Vin=VIH or VIL  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
	vultages to this high-	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ m/}$ $ I_{out}  \le 5.2 \text{ m/}$		3.98 5.48	3.84 5.34	3.70 5.20	-3×81 201
VOL	Maximum Low-Level Output Voltage, SQ <sub>H</sub>	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	(c.g., ether GND or Vgg1, Unuse outputs must be left open.	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 4.0 \text{ m}$ $ I_{\text{out}}  \le 5.2 \text{ m}$		0.26 0.26	0.33 0.33	0.40 0.40	37
lin	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	± 1.0	± 1.0	μΑ
loz	Maximum Three-State Leakage Current, Q <sub>A</sub> -Q <sub>H</sub>	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

	and ken ma	.,	Gu	Danisha		
Symbol	Parameter 0.0 0.5 COMO or become	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay, Shift Clock to SQ <sub>H</sub> (Figures 1 and 7)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
<sup>†</sup> PHL	Maximum Propagation Delay, Reset to SQH (Figures 2 and 7)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLH, tPHL	Maximum Propagation Delay, Latch Clock to QA-QH (Figures 3 and 7)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Q <sub>A</sub> -Q <sub>H</sub> (Figures 4 and 8)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Q <sub>A</sub> -Q <sub>H</sub> (Figures 4 and 8)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Q <sub>A</sub> -Q <sub>H</sub> (Figures 3 and 7)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
tTLH, tTHL	Maximum Output Transition Time, SQ <sub>H</sub> (Figures 1 and 7)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	V Fall	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State), QA-QH	-	15	15	15	pF

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	300	pF

TIMING REQUIREMENTS (Input  $t_r = t_f = 6 \text{ ns}$ )

		V-	Gua			
Symbol	Parameter Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tsu	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>su</sub>	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t <sub>W</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>W</sub>	Minimum Pulse Width, Shift Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
tw	Minimum Pulse Width, Latch Clock (Figure 6)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### **FUNCTION TABLE**

		Page 3		DIVETION	INDEL	(10) Jan 19 19 19 19 19 19 19 19 19 19 19 19 19	er med	Star Fast			
	Inputs					Resulting Function					
Operation	Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Shift Register Contents	Latch Register Contents	Serial Output SQ <sub>H</sub>	Parallel Outputs Q <sub>A</sub> -Q <sub>H</sub>		
Reset shift register	L	X	X	L, H, ~	L	L	U	L	U		
Shift data into shift register	Н	D		L, H, ~	L	D→SRA;	U	SRG→SRH	U		
Shift register remains unchanged	Haer	×	L, H, ~	L, H, ~	L 30	SR <sub>N</sub> →SR <sub>N+1</sub>	U	U	U		
Transfer shift register contents to latch register	Н	X	L, H, ~		r GN	U	SR <sub>N</sub> →LR <sub>N</sub>	U	SRN		
Latch register remains unchanged	X	X	X	L, H, \_	L	*	U	- U.*	U		
Enable parallel outputs	X	X	X	X	Log	*,	* *	*	Enabled		
Force outputs into high- impedance state	X	X	X	X	Н	and a	**	*	Z		

SR = shift register contents LR = latch register contents D = data (L, H) logic level U = remains unchanged

X = don't care Z = high impedance \* = depends on Reset and Shift Clock inputs \* \* = depends on Latch Clock input

#### PIN DESCRIPTIONS

#### **INPUTS**

A (Pin 14) — Serial Data Input. The data on this pin is shifted into the 8-bit serial shift register.

#### CONTROL INPUTS

Shift Clock (Pin 11) — Shift Register Clock Input. A low-to-high transition on this input causes the data at the Serial Input pin to be shifted into the 8-bit shift register.

Reset (Pin 10) — Active-low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8-bit latch is not affected.

Latch Clock (Pin 12) — Storage Latch Clock Input. A low-to-high transition on this input latches the shift register data.

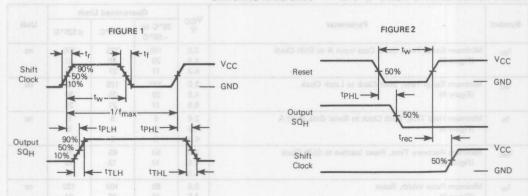
Output Enable (Pin 13) — Active-low Output Enable. A low on this input allows the data from the latches to be presented at the outputs. A high on this input forces the outputs  $(Q_A - Q_H)$  into the high-impedance state. The serial output is not affected by this control input.

#### OUTPUTS

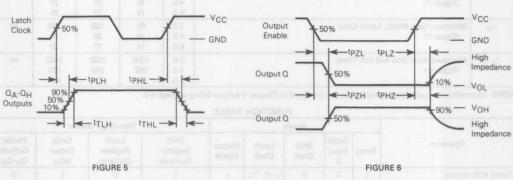
 $Q_{\mbox{\scriptsize A}}\text{-}Q_{\mbox{\scriptsize H}}$  (Pins 15, 1, 2, 3, 4, 5, 6, 7) - Noninverted, 3-state, latch outputs.

SQ<sub>H</sub> (Pin 9) — Noninverted, Serial Data Output. This is the output of the eighth stage of the 8-bit shift register. This output does not have three-state capability.

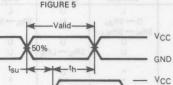


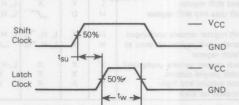


#### FIGURE 3 FIGURE 4



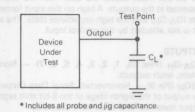
GND



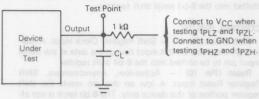


### FIGURE 7 - TEST CIRCUIT

50%



#### FIGURE 8 - TEST CIRCUIT



\* Includes all probe and jig capacitance.

5

Serial

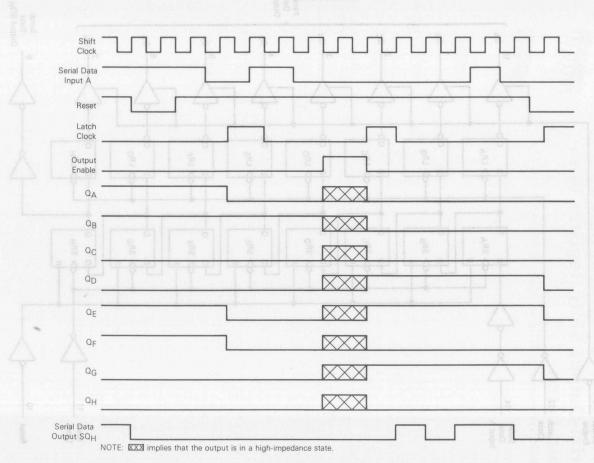
Input A

Shift

Clock

5

#### TIMING DIAGRAM



MOTOROLA HIGH-SPEED CMOS LOGIC DATA

5-424

## 8-Bit Serial- or Parallel-Input/ Serial-Output Shift Register With Input Latch

The MC54/74HC597 is identical in pinout to the LS597. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of an 8-bit input latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table).

The HC597 is similar in function to the HC589, which is a 3-state device.

**High-Performance Silicon-Gate CMOS** 

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 516 FETs or 129 Equivalent Gates

## MC54/74HC597



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



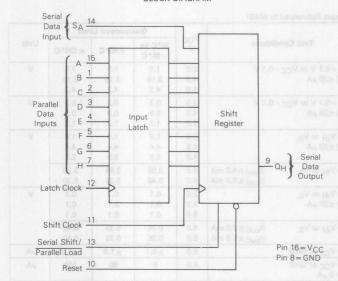
D SUFFIX SOIC CASE 751

#### ORDERING INFORMATION

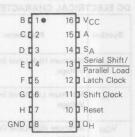
MC74HCXXXN MC54HCXXXJ MC74HCXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### **BLOCK DIAGRAM**



#### PIN ASSIGNMENT



5

#### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	CC = 2.0 V CC = 4.5 V CC = 6.0 V	0 0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	1 2 21 0 1 2 E				Gua	Unit		
Symbol	Parameter Test Conditions		VCC	25°C to -55°C	≤85°C		≤125°C	
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub>  I <sub>out</sub>   ≤20 μA	-0.1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V MG
VOH Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	0	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V	
		Vin=VIH or VIL	I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	L	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	\$ 102
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	± 1.0	± 1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	8	80	160	μА

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

#### AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_f = t_f = 6 \text{ ns}$ )

	Swarantood Limit		Gua			
Symbol	Parameter 2000 Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Uni
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 8)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	МН
tPLH, tPHL	Maximum Propagation Delay, Latch Clock to Q <sub>H</sub> (Figures 1 and 8)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
tPLH, tPHL	Maximum Propagation Delay, Shift Clock to Q <sub>H</sub> (Figures 2 and 8)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPHL	Maximum Propagation Delay, Reset to Q <sub>H</sub> (Figures 3 and 8)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLH, tPHL	Maximum Propagation Delay, Serial Shift/Parallel Load to Ω <sub>H</sub> (Figures 4 and 8)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	bo <del>-</del> ds	10	10	10	pF

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	50	pF

#### PIN DESCRIPTIONS

#### DATA INPUTS

A, B, C, D, E, F, G, H (PINS 15, 1, 2, 3, 4, 5, 6, 7) - Parallel data inputs. Data on these inputs is stored in the input latch on the rising edge of the Latch Clock input.

SA (PIN 14) — Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

#### **CONTROL INPUTS**

SERIAL SHIFT/PARALLEL LOAD (PIN 13) — Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the input latch, and serial shifting is inhibited.

RESET (PIN 10) — Asynchronous, Active-low shift register reset. A low level applied to this input resets the shift register to a low level, but does not change the data in the input latch.

SHIFT CLOCK (PIN 11) — Serial shift register clock. A low-to-high transition on this input shifts data on the Serial Data Input into the shift register and data in stage H is shifted out  $\Omega_H$ , being replaced by the data previously stored in stage G.

LATCH CLOCK (PIN 12) — Latch clock. A low-to-high transition on this input loads the parallel data on inputs A-H into the input latch.

#### OUTPUT

 $\Omega_{\mbox{\scriptsize H}}$  (PIN 9) — Serial data output. This pin is the output from the last stage of the shift register.

,	-95°C ≤95°C ≤125°C	٧	-55°C	≤85°C	≤125°C	Viiit
t <sub>su</sub>	Minimum Setup Time, Parallel Data Inputs A-H to Latch Clock	2.0	100	125	150	ns
ou	(Figure 5)	4.5	20	25	30	
	8.0 36 28 24	6.0	17	21	26	
t <sub>su</sub>	Minimum Setup Time, Serial Data Input SA to Shift Clock	2.0	100	125	150	ns
	(Figure 6)	4.5	20	25	30	THAI
	6.0 38 45 54	6.0	17	21	26	
t <sub>su</sub>	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock	2.0	100	125	150	ns
34	(Figure 7)	4.5	20	25	30	3497
	6,0 30 37 45	6.0	17	21	26	
th	Minimum Hold Time, Latch Clock to Parallel Data Inputs A-H	2.0	25	30	40	ns
	(Figure 5)	4.5	5	6	8	
	69 (6 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5	6.0	5	6	7	
th	Minimum Hold Time, Shift Clock to Serial Data Input SA	2.0	5	5	5	ns
-11	(Figure 6)	4.5	5	5	5	Jeig!
	28 05 0.8	6.0	5	5	5	
trec	Minimum Recovery Time, Reset Inactive to Shift Clock	2.0	100	125	150	·ns
100	(Figure 3)	4.5	20	25	30	JHTZ
	81 81 10	6.0	17	21	26	
tw	Minimum Pulse Width, Latch Clock and Shift Clock	2.0	80	100	120	ns
	(Figures 1 and 2)	4.5	16	20	24	.2910
	9-A space on police! A serious A retour(O em. Po	6.0	14	17	20	Lifet
tw	Minimum Pulse Width, Reset	2.0	80	100	120	ns
	(Figure 3)	4.5	16	20	24	FIG. 1
		6.0	14	17	20	
tw	Minimum Pulse Width, Serial Shift/Parallel Load	2.0	80	100	120	ns
	(Figure 4)	4.5	16	20	24	
		6.0	14	17	20	
tr, tf	Maximum Input Rise and Fall Times	2.0	1000	1000	1000	ns
	(Figure 1)	4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### FUNCTION TABLE

		707	Inputs	S			Resulting Function			
Operation	Reset	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	Serial Input S <sub>A</sub>	Parallel Inputs A-H	Latch Contents	Shift Register Contents	Output Q <sub>H</sub>	
Reset shift register	(199L 983	X X	L, H, \	X	X	X	no U an	to entit polish	ing inglateration	
Reset shift register; load parallel data into data latch	At ho	X Agid	-	X	X	a-h	a-h	stabilank2 — (A	MAN LES	
Load parallel data into data latch	Н	Н	5	L, H~	X	a-h	a-h	U	U	
Transfer latch contents to shift register	Н	proster Exerce-1	L, H~	X	X	X	U	LRN→SRN	LRH	
Contents of data latch and shift register are unchanged	Н	On on this inp	L, H, \_	L, H, ~	X	X	U	UNPUTS	CONTROL	
Load parallel data into data latch and shift register	Н	e inpulgiacoh.	_	X	X	a-h	a-h	AAA a-h	JAITHIE	
Shift serial data into shift register	Н	H Tt	X	1	D	X	visites of	$SR_A = D;$ $SR_N \rightarrow SR_{N+1}$	SRG→SRH	
Load parallel data into data latch and shift serial data into shift register	Н	o agent had es	_	5	D	a-h	a-h	$SR_A = D;$ $SR_N \rightarrow SR_{N+1}$	SR <sub>G</sub> →SR <sub>H</sub>	

LR = latch register contents SR = shift register contents

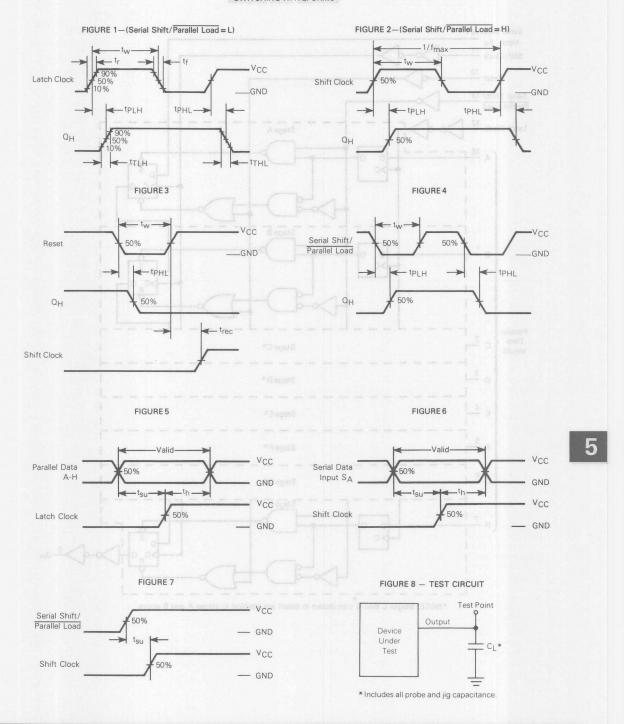
a-h = data at parallel data inputs A-H D = data (L, H) at serial data input S<sub>A</sub> U = remains unchanged

X = don't care

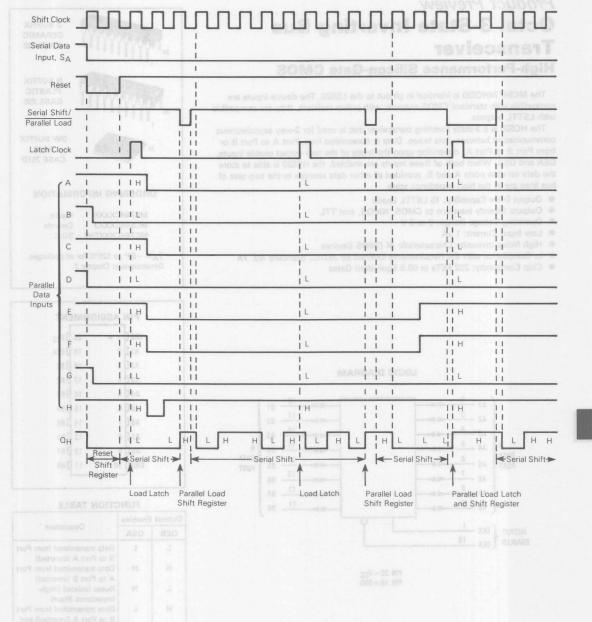
\* = depends on latch clock input

#### MC54/74HC597

#### SWITCHING WAVEFORMS







5

## Product Preview

## Octal 3-State Inverting Bus Transceiver

## **High-Performance Silicon-Gate CMOS**

The MC54/74HC620 is identical in pinout to the LS620. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC620 is a 3-state inverting transceiver that is used for 2-way asynchronous communication between data buses. Data is transmitted from Port A to Port B or from Port B to Port A, depending upon the levels of the two output enable inputs, OEA and OEB. When both of these inputs are enabled, the HC620 is able to store the data on data ports A and B, provided all other data sources to the two sets of bus lines are in the high impedance state.

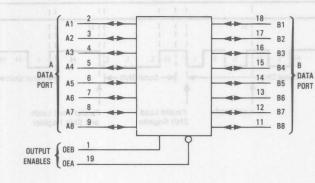
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 202 FETs or 50.5 Equivalent Gates



MC74HCXXXN Plastic
MC54HCXXXJ Ceramic
MC74HCXXXDW SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



 $\begin{array}{l} PIN \ 20 = V_{CC} \\ PIN \ 10 = GND \end{array}$ 

OEB [		- 00	h.,
4 31 6			VCC
A1 [	2	19	DEA
A2 [	3	18	B1
A3 [	4	17	]B2
A4 [	5	16	] B3
A5 [	6	15	] B4
A6 [	7	14	B5
A7 [	8	13	] B6
1 8A	9	12	<b>B</b> 7
GND [	10	11	B8

#### FUNCTION TABLE

Output Enables		
OEB	OEA	Operation
L	L	Data transmitted from Port B to Port A (inverted)
Н	Н	Data transmitted from Port A to Port B (inverted)
L	Н	Buses isolated (High- Impedance State)
Н	L	Data transmitted from Port B to Port A (inverted) and from Port A to Port B (inverted)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

#### **MAXIMUM RATINGS\***

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to V <sub>CC</sub> +1.5	V
VI/0	DC I/O Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin 1 or 19	± 20	mA
11/0	DC I/O Current, per I/O Pin	± 35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260 300	O ymA ,

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$ 

or V<sub>Out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)			6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	٧
TA	Operating Temperature, All Package Types	.94.6	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	*	200 4 830		Gua	aranteed Li	imit	
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	10 V 0
Voн	Minimum High-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
HER HPEGABLE		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0$ mA $ I_{out}  \le 7.8$ mA		0.26 0.26	0.33 0.33	0.40 0.40	
Iin	Maximum Input Leakage Current	Vin=Vcc or GND, Pin 1 or 19	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND, I/O Pins	6.0	±0.5	±5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 µA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

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AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input  $t_f = t_f = 6 \text{ ns}$ )

Symbol				Pr	learny		
	Parameter Parameter		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, A to B, B to A	0-	2.0	100	125	150	ns
<sup>t</sup> PHL	(Figures 1 and 3)		4.5 6.0	20 17	25 21	30 26	
tPLZ, tPHZ	Maximum Propagation Delay, OEA or OEB to A or B (Figures 2 and 4)		2.0 4.5	150 30	190 38	225 45	ns
19,77	750 mily control to the made (SI	TRIO sin	6.0	26	33	38	0.8
tPZL,	Maximum Propagation Delay, OEA or OEB to A or B (Figures 2 and 4)		2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	Package! mid DIP! ge to the device	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	necessi Decest	nspecific	10	10	10	pF
C <sub>out</sub>	Maximum Three-State I/O Capacitance (Output in High-Importance)	pedance	00° to 1	15	15	15	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

 Power Dissipation Capacitance (Per Transceiver Channel)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	201
Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC	agency such C 40 gency from 50	pF
For load considerations, see Chapter 4 subject listing on page 4-2.	Osserting Torrograture, All Pauloga Ty	A.T

#### **SWITCHING WAVEFORMS**

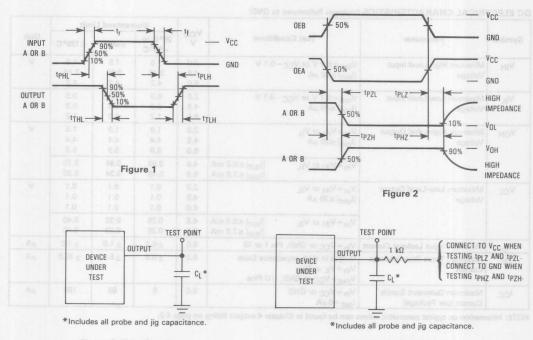


Figure 3. Test Circuit

Figure 4. Test Circuit

A1 -

A3 -

PORT

ENABLES

19

OEA -

A2 3 17 B2 17 B2

A DATA 15 B4

A5 6 B DATA PORT

12

OLITPUT OEB 1

250 = 01 104 250 = 50 104

## Octal 3-State Inverting Bus Transceiver with LSTTLCompatible Inputs

**High-Performance Silicon-Gate CMOS** 

The MC54/74HCT620 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT620 is identical in pinout to the LS620.

The HCT620 is a 3-state inverting transceiver that is used for 2-way asynchronous communication between data buses. Data is transmitted from Port A to Port B or from Port B to Port A, depending upon the levels at the two output enable inputs, OEA and OEB. When both of these inputs are enabled, the HCT620 is able to store the data on data ports A and B, provided all other data sources to the two sets of bus lines are in the high impedance state.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 202 FETs or 50.5 Equivalent Gates

#### LOGIC DIAGRAM 17 B2 16 **B3** 15 B4 DATA DATA 14 PORT B5 13 B6 12 B7 OUTPUT OEB -ENABLES OEA 19

 $\begin{array}{l} \text{PIN 20} = \text{V}_{\text{CC}} \\ \text{PIN 10} = \text{GND} \end{array}$ 

## MC54/74HCT620



#### ORDERING INFORMATION

MC74HCTXXXN Plastic MC54HCTXXXJ Ceramic MC74HCTXXXDW SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT 0EB [ 1 • 20 VCC A1 [ 2 19 0EA A2 [ A3 1 4 A4 [ 5 A5 [ 6 15 DB4 14 1 B5 Дад 13 B6 A7 [ 8 12 B7 A8 🛛 9 11 B8 GND [] 10

#### **FUNCTION TABLE**

Output Enables		0			
OEB	OEA	TUNE Operation			
L ar	L A30	Data transmitted from Port B to Port A (inverted)			
Н	Н	Data transmitted from Port A to Port B (inverted)			
L	Н	Buses isolated (High- Impedance State)			
Н	L	Data transmitted from Port B to Port A (inverted) and from Port A to Port B (inverted)			

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## 5

#### **MAXIMUM RATINGS\***

Symbol	Simil betasio Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	N P
Vin	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to V <sub>CC</sub> +1.5	V
VI/O	DC I/O Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin 1 or 19	±20	mA
1/0	DC I/O Current, per I/O Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
a <sub>o</sub> T <sub>L</sub> 3e	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

or Vout)≤VCC.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin

Unused inputs must always be tied to an appropriate logic level (e.g.,

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	A 800	V <sub>CC</sub>	Guaranteed Limit			
		Test Conditions		25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	0.8	0.8 0.8	0.8	٧
Voн	Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
	Figure 2	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	٧
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=Vcc or GND, Pin 1 or 19	5.5	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND, I/O Pins	5.5	±0.5	± 5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 µA	5.5	8	80	160	μΑ

ΔICC	Additional Quiescent Supply	Vin=2.4 V, Any One Input	Jeonstroeg	≥ -55°C	25°C to 125°C	
	Current	Vin = VCC or GND, Other Inputs				
		$I_{out} = 0 \mu A$	5.5	2.9	2.4	mA

#### NOTES:

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5.0 V ±10%, C<sub>L</sub>=50 pF, Input t<sub>f</sub>=t<sub>f</sub>=6 ns)

	Value Staff This device contains			Pr	Symba		
Symbol	Parameter (18.2)	25°C to -55°C		≤85°C	≤125°C	Unit	
tPLH, tPHL	Maximum Propagation Del (Figures 1 and 3)	ay, A to B, B to A	IOM	22	28	33	ns
tPLZ, tPHZ	Maximum Propagation Del (Figures 2 and 4)	ay, OEA or OEB to A or B		30	38	45	ns
tPZL,	Maximum Propagation Del (Figures 2 and 4)	ay, OEA or OEB to A or B	thic or Caramio DIP1	30	38	45	ns
tTLH, tTHL	Maximum Output Transitio (Figures 1 and 3)	n Time, Any Output	Tagains 1 Cities	12	15	18	ns
Cin	Maximum Input Capacitano	ce 2	serior 10 Seconds	10	10	10	pF
Cout	Maximum Three-State I/O	Capacitance (Output in High-Impe	edance State)	15	15	15	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD Vcc <sup>2</sup> f + Icc Vcc	MOITHUMOS DINITA 45 TO CIRCUIAN	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	The second secon	

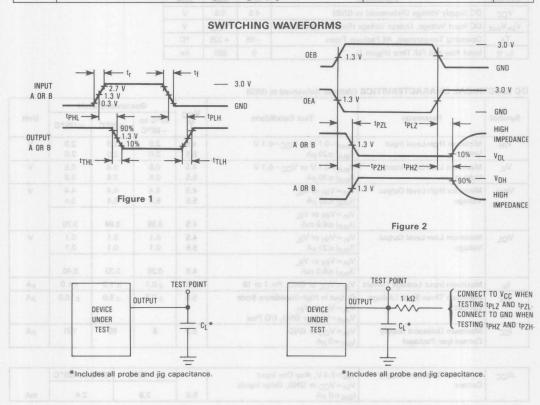
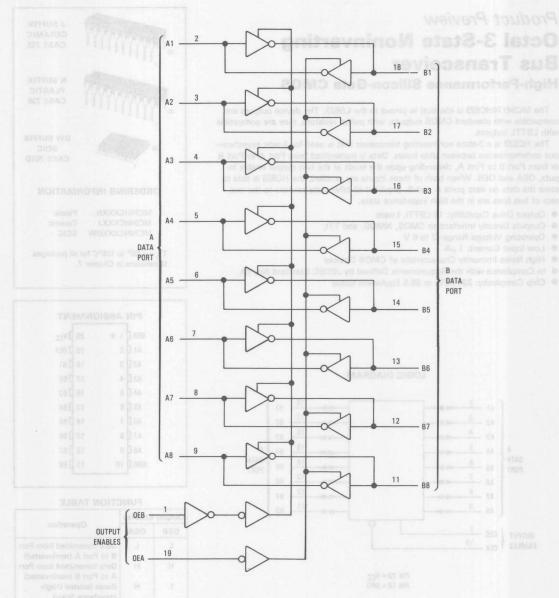


Figure 3. Test Circuit

Figure 4. Test Circuit



## Product Preview

## **Octal 3-State Noninverting Bus Transceiver**

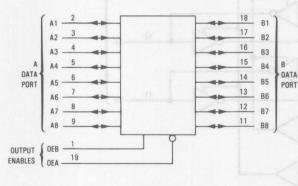
## **High-Performance Silicon-Gate CMOS**

The MC54/74HC623 is identical in pinout to the LS623. The device outputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC623 is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. Data is transmitted from Port A to Port B or from Port B to Port A, depending upon the levels at the two output enable inputs, OEA and OEB. When both of these inputs are enabled, the HC623 is able to store the data on data ports A and B, provided all other data sources to the two sets of bus lines are in the high impedance state.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates

#### LOGIC DIAGRAM



PIN 20 = VCC PIN 10 = GND



J SUFFIX CERAMIC **CASE 732** 



N SUFFIX PLASTIC **CASE 738** 



DW SUFFIX SOIC CASE 751D

#### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXDW SOIC

Plastic Ceramic

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT

				4
	OEB [	1 •	20	vcc
	A1 [	2	19	OEA
	A2 [	3	18	]B1
	A3 [	4	17	] B2
	A4 [	5	16	] B3
	A5 [	6	15	] B4
Ĥ	A6 [	7	14	B5
	A7 [	8	13	<b>3</b> B6
	A8 [	9	12	] B7
	GND [	10	11	B8

#### **FUNCTION TABLE**

Output	Enables	
OEB	OEA	Operation
L 91	L	Data transmitted from Port B to Port A (noninverted)
Н	Н	Data transmitted from Port A to Port B (noninverted)
L	Н	Buses isolated (High- Impedance State)
Н	L	Data transmitted from Port B to Port A (noninverted) and from Port A to Port B (noninverted)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Symbol	Herid betwee Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to V <sub>CC</sub> +1.5	V
VI/O	DC I/O Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin 1 or 19	±20	mA
11/0	DC I/O Current, per I/O Pin	±35	mA
Icc	DC Supply Current, VCC and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C May ami

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions. †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mbox{GND} \! \leq \! (V_{in})$  or  $V_{out} \! \mid \! \leq \! V_{CC}$ .

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to	GND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage	(Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Packag	Operating Temperature, All Package Types		+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> =2.0 V	0	1000	ns
17.1	(Figure 1)	V <sub>CC</sub> =4.5 V	0	500	
		Vcc=6.0 V	0	400	

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	and the same of th			Guaranteed Limit			11/999
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	TUPINUS A CR 6
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2,0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
BAUTHER		$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 6.0 \text{ mA}$ $ I_{\text{out}}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
	TEST POINT	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 6.0 \text{ mA}$ $ I_{\text{out}}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND, Pin 1 or 19	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND, I/O Pins	6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

5

AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

	Make Chit This daylos contains			Pr	ladmyk		
Symbol	Parameter 0.1 + or 0.5 + or 0.		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, A to B, B to A		2.0	100	125	150	ns
tpHL (Figures 1 and 3)	(Figures 1 and 3)		4.5 6.0	20 17	25 21	30 26	nd.
tPLZ,	Maximum Propagation Delay, OEA or OEB to A or B		2.0	150	190	225	ns
tPHZ	(Figures 2 and 4)		4.5	30	38	45	335
constrained to the range CPID ss (V)	260 on Viro constrained to the range C		6.0	26	33	38	09
tPZL,	Maximum Propagation Delay, OEA or OEB to A or B	Tegszosti	2.0	150	190	225	ns
tPZH	(Figures 2 and 4)		4.5	30	38	45	Torio
- 8/11/ Jane	agol mandorate os ot		6.0	26	33	38	T
tTLH,	Maximum Output Transition Time, Any Output	Linguista (	2.0	60	75	90	ns
THL	(Figures 1 and 3)		4.5	12	15	18	
or two Soo Disputed & suitled	lation requirement. Link or him Son Linkelier		6.0	10	13	15	and the same
Cin	Maximum Input Capacitance	O belonsing	900 <del>11</del> 96	10	10	10	pF
Cout	Maximum Three-State I/O Capacitance (Output in High-Imped State)	lance	07 to 130 1007 to	15	15	15	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	STORY OF
	Used to determine the no-load dynamic power consumption:	START A PRINTED BY SERVICE AND ADDRESS OF THE ADDRE	DOK
	PD=CPD VCC2f+ICC VCC	material material section 40 mov rocal 00	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	Change of Tennandium A. Roden in Tunio	0.7

#### **SWITCHING WAVEFORMS**

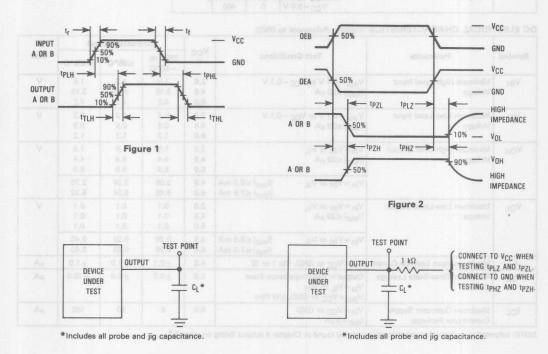


Figure 3. Test Circuit

Figure 4. Test Circuit

DATA

OEB -

OUTPUT ENABLES

PORT

## Product Preview

## Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs

**High-Performance Silicon-Gate CMOS** 

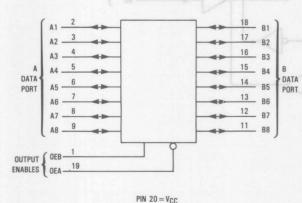
The MC54/74HCT623 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT623 is identical in pinout to the LS623.

The HCT623 is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. Data is transmitted from Port A to Port B or from Port B to Port A, depending upon the levels at the two output enable inputs, OEA and OEB. When both of these inputs are enabled, the HCT623 is able to store the data on data ports A and B, provided all other data sources to the two sets of bus lines are in the high impedance state.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates

#### LOGIC DIAGRAM



PIN 10 = GND

MC54/74HCT623



#### ORDERING INFORMATION

MC74HCTXXXN Plastic MC54HCTXXXJ Ceramic MC74HCTXXXDW SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT OFR I 1 e 20 VCC 19 0EA A1 0 2 18 B1 A2 [ 3 A3 [ 4 A4 [ 5 A5 [ 6 14 T B5 АБП A7 [ 8 13 DB6 A8 [ 9 12 B7 11 B8 GND [

#### FUNCTION TABLE

Output	Enables				
OEB	OEA	Operation			
L	L	Data transmitted from Port B to Port A (noninverted)			
Н	Н	Data transmitted from Port A to Port B (noninverted)			
L	Н	Buses isolated (High- Impedance State)			
Н	L	Data transmitted from Port B to Port A (noninverted) and from Port A to Port B (noninverted)			

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

## 5

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this highimpedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or V<sub>out</sub>)≤V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic level (e.g., either GND or VCC). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject

listing on page 4-2.

#### **MAXIMUM RATINGS\***

Symbol	Menia boddele Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5  to  +7.0	٧
Vin	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to V <sub>CC</sub> +1.5	V
VI/O	DC I/O Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	V
lin	DC Input Current, per Pin 1 or 19	±20	mA
1/0	DC I/O Current, per I/O Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
≒JL åq	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	٧
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
tr, tf	Input Rise and Fall Time (Figure 1)	0	500	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	T. T.	Add data	Voc	Guaranteed Limit			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	2 70 V
VIL	Maximum Low-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V or } V_{\text{CC}} - 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu\text{A}$	4.5 5.5	0.8	0.8 0.8	0.8 0.8	V
VOH Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V	
	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	3.98	3.84	3.70		
VOL	Maximum Low-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \mu \text{A}$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
lin	Maximum Input Leakage Current	Vin=V <sub>CC</sub> or GND, Pin 1 or 19	5.5	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or $V_{IH}$ $V_{out} = V_{CC}$ or GND, I/O Pins	5.5	±0.5	±5.0	±10.0	μА
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	5.5	8	80	160	μА

ΔICC	Additional Quiescent Supply	Vin=2.4 V, Any One Input		≥ -55°C	25°C to 125°C	
	Current	Vin = Vcc or GND, Other Inputs				
	estationers of the exception in a	I <sub>out</sub> =0 μA	5.5	2.9	2.4	mA

#### NOTES

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5.0 V  $\pm$  10%, C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

	Trils daylor contains		Veltue		Projected Limit			
Symbol	circultry to guard again	Parameter	to SND) GND), Plo Tur 19	25°C to -55°C	≤85°C	≤125°C	Unit	
tPLH, tPHL	Maximum Propagation Delay, (Figures 1 and 3)	A to B, B to A	101/1	22	28	33	ns	
tPLZ, tPHZ	Maximum Propagation Delay, (Figures 2 and 4)	OEA or OEB to A or B		30	38	45	ns	
tPZL, tPZH	Maximum Propagation Delay, (Figures 2 and 4)	OEA or OEB to A or B	ID Para	30	38	45	ns	
tTLH, tTHL	Maximum Output Transition (Figures 1 and 3)	Fime, Any Output	Trabable Ands	12	15	18	ns	
Cin	Maximum Input Capacitance	34	abopen 8 of not see	10	10	10	pF	
Cout	Maximum Three-State I/O Ca	pacitance (Output in High-Impe	edance State)	15	15	15	pF	

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	Hot tulle
	Used to determine the no-load dynamic power consumption:	Service and the service and th	
	PD = CPD VCC <sup>2</sup> f+ICC VCC	DMOO DM IA 45 TU USUMSIA	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

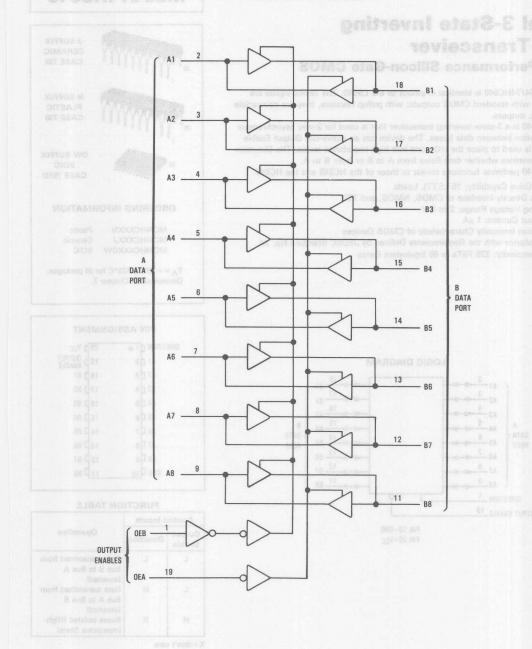
#### SWITCHING WAVEFORMS 3.0 V 1.3 V GND INPUT 3.0 V 3.0 V A OR B 1.3 V - GND GND tPLH . - tPHL - tpzL tPLZ-HIGH OUTPUT IMPEDANCE A OR B A OR B 10% \_ VOL TLH -tPZH tpHZ -> VOH HIGH IMPEDANCE Figure 1 Figure 2 TEST POINT TEST POINT CONNECT TO $v_{CC}$ when testing $t_{PLZ}$ and $t_{PZL}$ . OUTPUT OUTPUT DEVICE DEVICE CONNECT TO GND WHEN UNDER UNDER TESTING THE AND THE CL 4 TEST TEST

Figure 3. Test Circuit

\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

\*Includes all probe and jig capacitance.

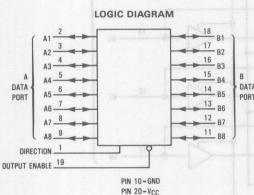


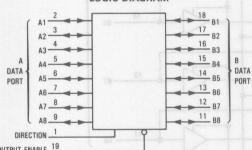
The MC54/74HC640 is identical in pinout to the LS640. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC640 is a 3-state inverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HC640 performs functions similar to those of the HC245 and the HC643.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 276 FETs or 69 Equivalent Gates





IVIUUTI / TI IUUTU



#### ORDERING INFORMATION

CASE 751D

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

## PIN ASSIGNMENT

DIRECTION [1	20 D VCC
A1 C2	19 OUTPUT
A2 🖸 3	18 J B1
A3 🖸 4	17 D B2
A4 C 5	16 D B3
A5 🗆 6	15 D B4
A6 C 7	14 D B5
A7 08	13 B6
A8 Q9	12 B7
GND C 10	11 B8

#### FUNCTION TABLE

Contro	ol Inputs	
Output Enable	Direction	Data transmitted from Bus B to Bus A (inverted) Data transmitted from
L	L 439	
L H		Data transmitted from Bus A to Bus B
Н	×	(inverted) Buses isolated (High- Impedance State)

X = don't care

#### **MAXIMUM RATINGS\***

Symbol	stant I been Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to V <sub>CC</sub> +1.5	V
VI/O	DC I/O Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	٧
lin	DC Input Current, per Pin	± 20	mA
1/0	DC I/O Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Parameter		Min	Max	Unit
DC Supply Voltage (Referenced to	C Supply Voltage (Referenced to GND)		6.0	V
DC Input Voltage, Output Voltage	Referenced to GND)	0	Vcc	V
Operating Temperature, All Package Types		- 55	+ 125	°C
Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V	0	1000 500	ns
	DC Supply Voltage (Referenced to DC Input Voltage, Output Voltage ( Operating Temperature, All Package Input Rise and Fall Time	DC Supply Voltage (Referenced to GND)  DC Input Voltage, Output Voltage (Referenced to GND)  Operating Temperature, All Package Types  Input Rise and Fall Time  VCC = 2.0 V	DC Supply Voltage (Referenced to GND)         2.0           DC Input Voltage, Output Voltage (Referenced to GND)         0           Operating Temperature, All Package Types         -55           Input Rise and Fall Time         VCC = 2.0 V           (Figure 1)         VCC = 4.5 V	DC Supply Voltage (Referenced to GND)         2.0         6.0           DC Input Voltage, Output Voltage (Referenced to GND)         0         V <sub>CC</sub> Operating Temperature, All Package Types         -55         +125           Input Rise and Fall Time         V <sub>CC</sub> =2.0 V         0         1000           (Figure 1)         V <sub>CC</sub> =4.5 V         0         500

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol		Test Conditions		V <sub>CC</sub>	Guaranteed Limit			
	Parameter				25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
	France 2	Vin=VIH or VIL	$ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	THE PLANT	Vin=VIH or VIL	I <sub>out</sub>   ≤6.0 mA  I <sub>out</sub>   ≤7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=V <sub>CC</sub> or GND, Pin 1 or 19		6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND		6.0	±0.5	±5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 µA		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

	aniambo solvets sid?		.,	Gua	aranteed Li	imit	
Symbol	disperies of production of the state of the	Parameter 100 m 8.0 m	Vcc	25°C to -55°C	≤85°C	≤ 125°C  150 30 26  225 45 38  225 45 38  90 18 15	Unit
tPLH,	Maximum Propagation Delay	, A to B, B to A	2.0	100	125	150	ns
tPHL	(Figures 1 and 3)		4.5 6.0	20 17	25 21	41-17-1802-1803-0	
tPLZ,	Maximum Propagation Delay	, Direction or Output Enable to A or B	2.0	150	190	225	ns
tPHZ	(Figures 2 and 4)		4.5	30	38	45	
	agnavast of benistenes		6.0	26	33	38	
tPZL,	Maximum Propagation Delay	, Direction or Output Enable to A or B	2.0	150	190	225	ns
tPZH	(Figures 2 and 4)		4.5	30	38	45	
	olgel standarde na et		6.0	26	33	38	
tTLH,	Maximum Output Transition	Time, Any Output	2.0	60	75	90	ns
tTHL	(Figures 1 and 3)		4.5	12	15	18	
	Pine to be San Change		6.0	10	13	15	
Cin	Maximum Input Capacitance	, Pin 1 or 19	orrace# add	10	10	10	pF
C <sub>out</sub>	Maximum Three-State I/O C State)	apacitance (Output in High-Impedance	967-20 125°C 100° to 125	15	15	15	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	MS of merumanism afficient diddes and	
	PD = CPD VCC2f+ICC VCC	197 from Von 04 , Output Valley (Ref	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	Character Temperature All Deplement	

#### **SWITCHING WAVEFORMS**

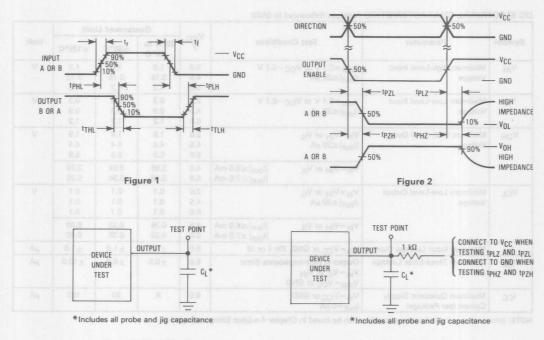


Figure 3. Test Circuit

Figure 4. Test Circuit

The MC54/74HCT640 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT640 is identical in pinout to the LS640.

The HCT640 is a 3-state inverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HCT640 performs functions similar to those of the HCT245 and the HCT643.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 358 FETs or 89.5 Equivalent Gates

J SUFFIX
CERAMIC
CASE 732

N SUFFIX
PLASTIC
CASE 738

DW SUFFIX
SOIC
CASE 751D

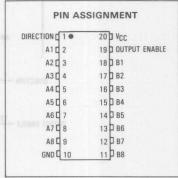
#### ORDERING INFORMATION

MC74HCTXXXN MC54HCTXXXJ MC74HCTXXXDW Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# LOGIC DIAGRAM A1 2 3 4 16 83 16 83 86 14 85 PORT A6 7 48 9 11 88 DIRECTION 1 19 OUTPUT ENABLE 19 DIRECTION 1 19

PIN 10-GND PIN 20-V<sub>CC</sub>



#### **FUNCTION TABLE**

Contro	ol Inputs	
Output Enable	Direction	Operation
L	L	Data transmitted from Bus B to Bus A (inverted)
L	Н	Data transmitted from Bus A to Bus B (inverted)
Н	X	Buses Isolated (High- Impedance State)

X = don't care

#### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to V <sub>CC</sub> +1.5	V
VI/O	DC I/O Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
1/0	DC I/O Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>Lq</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300 1 1001	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\text{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
T <sub>A</sub>	Operating Temperature, All Package Types	- 55	+ 125	°C
tr, tf	Input Rise and Fall Time (Figure 1)	0	500	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	The state of the s	Value 1980 to 1970 to 1970		Guaranteed Limit			
Symbol	Parameter	Test Conditions	Vcc	25°C to -55°C	≤85°C	mit  ≤125°C  2.0  2.0  0.8  0.8  4.4  5.4  3.70  0.1  0.40  ±1.0  ±10.0	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0		٧
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	4.5 5.5	0.8	0.8		٧
Vон	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4		V
HON EMPEDANCE		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1		V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$	4.5	0.26	0.33	≤125°C  2.0 2.0 0.8 0.8 4.4 5.4  3.70 0.1 0.1  0.40 ±1.0 ±10.0	
lin	Maximum Input Leakage Current	Vin=Vcc or GND, Pin 1 or 19	5.5	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  Vin = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND, I/O Pins	5.5	±0.5	±5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 µA	5.5	8	80	160	μΑ

7ICC	Additional Quiescent Supply	Vin=2.4 V, Any One Input	tenna.	≥ -55°C	25°C to 125°C	
	Current	Vin = VCC or GND, Other Inputs				
	gro 4. Test Circuit	I <sub>out</sub> = 0 µA	5.5	2.9	2.4	

#### NOTES:

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5.0 V ± 10%, C<sub>L</sub>=50 pF, Input t<sub>r</sub>=t<sub>f</sub>=6 ns)

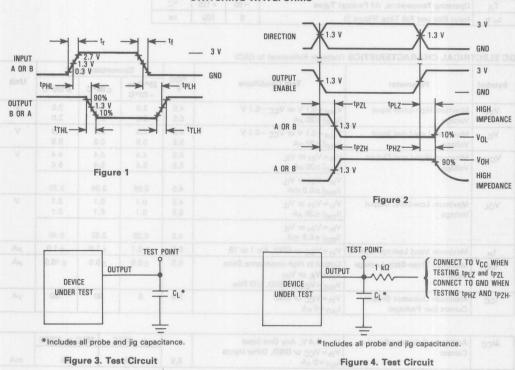
	This device continue			Guaranteed Limit			
Symbol	circuity to guero aspending to the comparison of	Parameter 400	25°C to -55°C	≤85°C	≤125°C	Unit	
tPLH, tPHL	Maximum Propagation Delay, (Figures 1 and 3)	A to B or B to A	22	28	33	ns	
tPLZ, tPHZ	Maximum Propagation Delay, (Figures 2 and 4)	Direction or Output Enable to A or B	30	38	45	ns	
tPZL, tPZH	Maximum Propagation Delay, (Figures 2 and 4)	Direction or Output Enable to A or B	30	38	45	ns	
tTLH, tTHL	Maximum Output Transition T (Figures 1 and 3)	ime, Any Output	12	15	18	ns	
Cin	Maximum Input Capacitance,	Pin 1 or 19	10	10	10	pF	
Cout	Maximum Three-State I/O Ca	pacitance (Output in High-Impedance State)	15	15	15	pF	

#### NOTES:

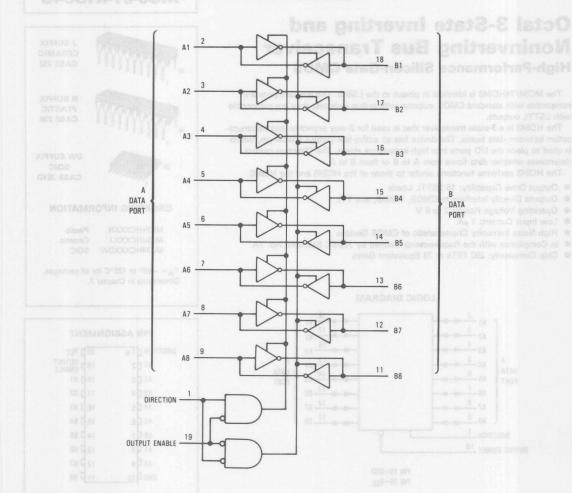
- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	at addut to
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	виотпаноз випувано аваиз	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	Paramater	Seminal .

#### SWITCHING WAVEFORMS



**EXPANDED LOGIC DIAGRAM** 



The MC54/74HC643 is identical in pinout to the LS643. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC643 is a 3-state transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HC643 performs functions similar to those of the HC245 and the HC640.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 292 FETs or 73 Equivalent Gates

J SUFFIX CERAMIC CASE 732

N SUFFIX PLASTIC CASE 738

DW SUFFIX SOIC CASE 751D

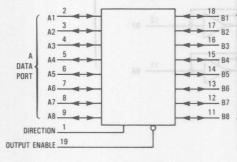
CASE 751D

#### ORDERING INFORMATION

MC74HCXXXN Plastic MC54HCXXXJ Ceramic MC74HCXXXDW SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM



PIN 10-GND PIN 20-VCC

#### **PIN ASSIGNMENT** DIRECTION [1. 20 UVCC 19 DOUTPUT A1 02 A2 [3 18 B1 A3 04 17 h B2 A4 0 5 A5 0 6 15 B4 A6 07 14 85 A7 08 13 B6 12 B7 A8 Q9 GND Q 10 11 B8

#### **FUNCTION TABLE**

Control Inputs		
Output Enable	Direction	Operation
L	L	Data transmitted from Bus B to Bus A (not inverted)
L	н	Data transmitted from Bus A to Bus B (inverted)
Н	X	Buses Isolated (High-Impedance State)

X = don't care

DATA

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to V <sub>CC</sub> +1.5	V
VI/O	DC I/O Voltage (Referenced to GND)	$-0.5$ to $V_{CC} + 0.5$	V
lin	DC Input Current, per Pin	± 20	mA
1/0	DC I/O Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$  VCC.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to G	ND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (R	eferenced to GND)	0	Vcc	٧
TA	Operating Temperature, All Package	Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Parameter Test Conditions			Guaranteed Limit			10
Symbol		VCC	25°C to -55°C	≤85°C	≤125°C	Unit	
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL JOV	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	Figure 2	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 6.0 \text{ mA}$ $ I_{\text{out}}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
4M 25A D.L.	TPUT   1 KO CORNED	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=Vcc or GND, Pin 1 or 19	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND	6.0	±0.5	±5.0	±10.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8 agas gij bra	80 400 mg lis a	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

Symbol			Vcc	Guaranteed Limit			Syrobel	
	dign through or yellowing operation of the control	Parameter	ameter 0 - or 2.0-		25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation De (Figures 1 and 3)	lay, A to B, B to A	at 8.0	2.0 4.5	100 20	125 25	150 30	ns
Sid slift	ni supptiev bates			6.0	17	21	26	T.F.
tPLZ, tPHZ	Maximum Propagation De (Figures 2 and 4)	ay, Direction or Output E	enable to A or B	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL,	Maximum Propagation De (Figures 2 and 4)	ay, Direction or Output E		2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition (Figures 1 and 3)	on Time, Any Output	Package? mto DPRI	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitan	ce, Pin 1 or 19	conded Downsting C	moself-citi	10	10	10	pF
C <sub>out</sub>	Maximum Three-State I/O State)	Capacitance (Output in	High-Impedance	#152_10, 269 m 18Q° to 12	15	15	15	pF

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD Vcc <sup>2</sup> f + Icc Vcc	salest a stoy methol at 40 ov ment ox	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	Converse Lamondaire Ad Burlana Tun	

#### **SWITCHING WAVEFORMS**

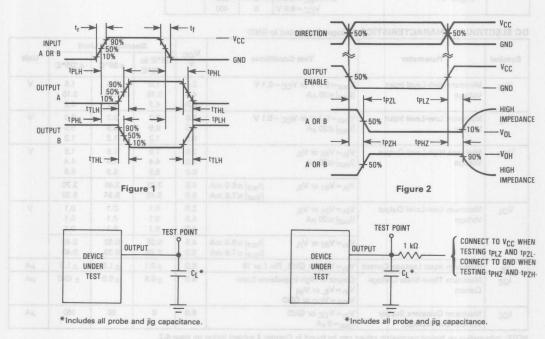


Figure 3. Test Circuit

Figure 4. Test Circuit

17 B2

16 B3

15\_B4

14 B5

13\_B6

12 B7

B DATA

DATA
PORT

DIRECTION -

OUTPUT ENABLE 19

MOTTA MANAGEMENT DATA

PORT

# **Octal 3-State Inverting and Noninverting Bus Transceiver** with LSTTL-Compatible Inputs **High-Performance Silicon-Gate CMOS**

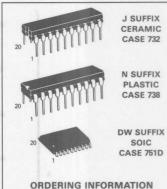
The MC54/74HCT643 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT643 is identical in pinout to the LS643.

The HCT643 is a 3-state transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HCT643 performs functions similar to those of the HCT245 and the HCT640.

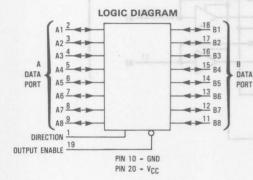
- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 342 FETs or 85.5 Equivalent Gates



MC74HCTXXXN MC54HCTXXXJ MC74HCTXXXDW

Plastic Ceramic SOIC

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.



#### PIN ASSIGNMENT DIRECTION 1 1 20 VCC 19 DOUTPUT A1 2 A2 [ 3 18 B1 17 B2 16 B3 A4 [ 5 A5 0 6 15 B4 14 D B5 A6 0 7 13 B6 A7 0 8 A8 0 9 12 B7 11 B8 GND [ 10

#### **FUNCTION TABLE**

Control Inputs		
Output Enable Direction		Operation
L	L	Data transmitted from Bus B to Bus A (not inverted)
L	Н	Data transmitted from Bus A to Bus B (inverted)
Н	X	Buses Isolated (high-impedance state)

X = don't care

#### **MAXIMUM RATINGS\***

Symbol	Heria Hayares Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to V <sub>CC</sub> +1.5	V
VI/O	DC I/O Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
1/0	DC I/O Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
√L Aq	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this highimpedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (Vin or Vout)≤VCC.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or VCC). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	4.5	5.5	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Parameter	grand de la constant	1	Gua	*			
Symbol		Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu A$	Bell	4.5 5.5	2.0	2.0 2.0	2.0	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤20 μA	163/1	4.5 5.5	0.8	0.8	0.8	V
Vон	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤20 μA		4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	٧
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤6.0 mA	2,07	4.5	3.98	3.84	3.70	
V <sub>OL</sub> Maximum Low-Level Output Voltage		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤20 μA		4.5 5.5	0.1	0.1 0.1	0.1 0.1	V
	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$		4.5	0.26	0.33	0.40		
lin	Maximum Input Leakage Current	Vin=VCC or GND, Pin 1 or 19		5.5	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND, I/O Pins		5.5	±0.5	±5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		5.5	8	80	160	μΑ

ΔI <sub>CC</sub> Additional Quiescent Supply V <sub>in</sub> =2.4 V, Any One Input	· Helm	≥ -55°C	25°C to 125°C	
Current $V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0 \mu A$	5.5	2.9	2.4	

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5.0 V  $\pm$  10%, C<sub>L</sub>=50 pF, Input t<sub>r</sub>=t<sub>f</sub>=6 ns)

Symbol	Value Ualt This device concerns	49764716	Guaranteed Limit			
	Parameter of 3.0	25°C to -55°C	<85°C	≤125°C	Unit	
tPLH, tPHL	Maximum Propagation Delay, A to B or B to A (Figures 1 and 3)	22	28	33	ns	
tPLZ, tPHZ	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	30	38	45	ns	
tPZL, tPZH	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	30	38	45	ns	
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	. 12	15	18	ns	
Cin	Maximum Input Capacitance, Pin 1 or 19	10	10	10	pF	
Cout	Maximum Three-State I/O Capacitance (Output in High-Impedance State)	15	15	15	pF	

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	He was a second
	Used to determine the no-load dynamic power consumption:  PD = CPD Vcc <sup>2</sup> f + Icc Vcc	виот сиоо висти	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	Parameter	Gymbal

#### SWITCHING WAVEFORMS

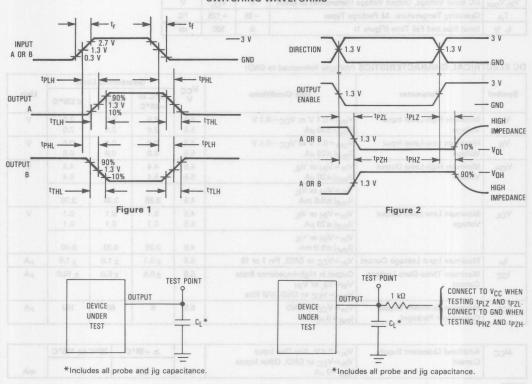


Figure 3. Test Circuit

Figure 4. Test Circuit

**EXPANDED LOGIC DIAGRAM** 

# Octal 3-State Bus Transceivers and D Flip-Flops

## **High-Performance Silicon-Gate CMOS**

The MC54/74HC646 and the MC54/74HC648 are identical in pinout to the LS646 and the LS648. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices are bus transceivers with D flip-flops. Depending on the status of the Data-Source Selection pins, data may be routed to the outputs either from the flip-flops or transmitted real-time from the inputs (see Function Table and Application Information).

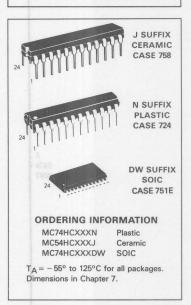
The Output Enable and the Direction pins control the transceiver's function. Bus A and Bus B cannot be routed as outputs to each other simultaneously, but can be routed as inputs to the A and B flip-flops simultaneously. Also, the A and B flip-flops can be routed as outputs to Bus A and Bus B simultaneously. Additionally, when either or both of the ports are in the high-impedance state, these I/O pins may be used as inputs to the D flip-flops for data storage.

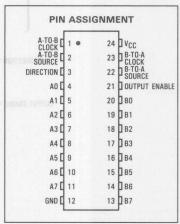
The user should note that because the clocks are not gated with the Direction and Output Enable pins, data at the A and B ports may be clocked into the storage flip-flops at any time.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 780 FETs or 195 Equivalent Gates

#### LOGIC DIAGRAM 20 19 18 17 DATA DATA 16 PORT 15 14 -B6 13 **OUTPUT ENABLE** DIRECTION FLIP-FLOP A-TO-B CLOCK 23 CLOCKS B-TO-A CLOCK DATA-SOURCE ( A-TO-B SOURCE SELECTION B-TO-A SOURCE . PIN 24 = Vcc INPUTS PIN 12 = GND

# MC54/74HC648





HC646 - Noninverting Outputs HC648 - Inverting Outputs

This device contains protection circuitry to guard against damage

constrained to the range GND  $\leq$  (V<sub>in</sub> or V<sub>Out</sub>)  $\leq$  V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

#### **MAXIMUM RATINGS\***

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	٧
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
VI/0	DC I/O Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
1/0	DC I/O Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	d to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	/ <sub>CC</sub> =2.0 V / <sub>CC</sub> =4.5 V / <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns (4) ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	A mass 20 x 15 um @ model.	The second secon		Gua			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V or } V_{\text{CC}} = 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Vон	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
	3 8 8	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
	18 20 24 14 17 20	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND (Pins 1, 2, 3, 21, 22, and 23)	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND, I/O Pins	6.0	±0.5	±5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C1 = 50 pF, Input tr=tf=6 ns)

	Value Unit This series consine p		Gua	aranteed Li	mit	
Symbol	Parameter 0.5% of 8.0— augustus ottem rigid of odb	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
fmax	Maximum Clock Frequency (50% Duty Cycle)	2.0	6.0	4.8	4.0	MHz
muminas cinia	(Figures 3, 4 and 9)	4.5 6.0	30 35	24 28	20 24	
tPLH,	Maximum Propagation Delay, Input A to Output B (or Input B to	2.0	170	215	255	ns
tPHL	utput A) All All All All All All All All All	4.5	34	43	51	
of Via G	(Figures 1, 2 and 9)	6.0	29	37	43	
tPLH,	Maximum Propagation Delay, A-to-B Clock to Output B (or B-to-A Clock	2.0	220	275	330	ns
tPHL	to Output A)	4.5	44	55	66	
2.07 10	(Figures 3, 4 and 9)	6.0	37	47	56	
tPLH,	Maximum Propagation Delay, A-to-B Source to Output B (or B-to-A Source	2.0	170	215	255	ns
tPHL	to Output A)	4.5	34	43	51	
	(Figures 5, 6 and 9)	6.0	29	37	43	
tPLZ,	Maximum Propagation Delay, Direction or Output Enable to Output A or B	2.0	175	220	265	ns
tPHZ	(Figures 7, 8 and 10)	4.5	35	44	53	
		6.0	30	37	45	
tPZL,	Maximum Propagation Delay, Direction or Output Enable to Output A or B	2.0	175	220	265	ns
tPZH	(Figures 7, 8 and 10)	4.5	35	44	53	
		6.0	30	37	45	
tTLH,	Maximum Output Transition Time, Any Output	2.0	60	75	90	ns
THL	(Figures 1 and 9)	4.5	12	15	18	
	Will Make Held	6.0	10	13	15	
Cin	Maximum Input Capacitance	00000	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High-Impedance State)	elegyT :	15	15	15	pF

#### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Channel)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
seu	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	60	pF

TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

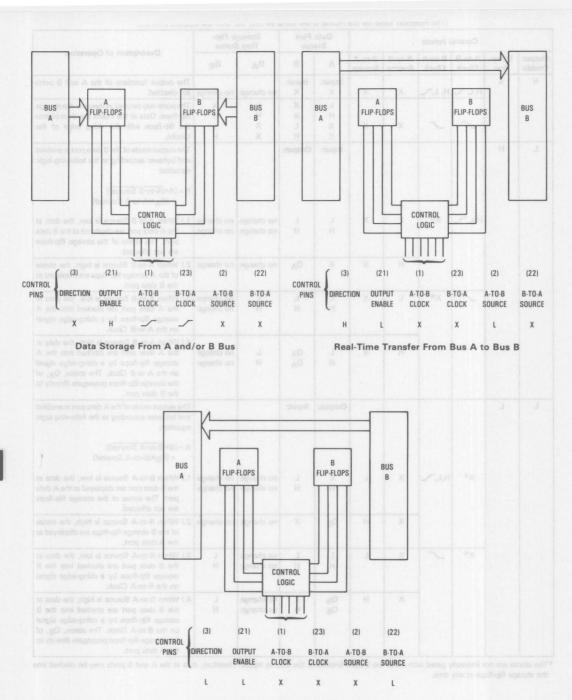
	0.0 0.0 0.0 0.0 0.0 0.0 0.0 0.0 0.0 0.0	On the	Gua			
Symbol	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Input A to A-to-B Clock (or Input B to B-to-A Clock) (Figures 3 and 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, A-to-B Clock to Input A (or B-to-A Clock to Input B) (Figures 3 and 4)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
tw	Minimum Pulse Width, A-to-B Clock (or B-to-A Clock) (Figures 3 and 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

		Contro	Inputs				Port		ge Flip- States	
Output Enable	Direc- tion	A-to-B Clock	B-to-A Clock	A-to-B Source	B-to-A Source	А	В	QA	α <sub>B</sub>	Description of Operation
Н	X	H,L,~	H, L,\	X	Х	Input:	Input:	no change	no change	The output functions of the A and B ports are disabled.
8118		1	~	×	×	H X X	X X L H	L H X	X X L H	The ports may be used as inputs to the storage flip-flops. Data at the inputs are clocked into the flip-flops with the rising edge of the Clocks.
L	Н	H,L,~	×*		X	Input:	Output:	no change	no change	The output mode of the B data port is enabled and behaves according to the following logic equation:  B = [A•(A-to-B Source)] + [QA•(A-to-B Source)]  1.) When A-to-B Source is low, the data at the A data port are displayed at the B data
			m	T		,,,		no change	no change	port. The states of the storage flip-flops are not affected.
1221		(65	19	Н	X	X	QA	no change	no change	<ol> <li>When A-to-B Source is high, the states of the A storage flip-flops are displayed at the B data port.</li> </ol>
A:01-9 308003 X		1	X*	L 10	х	L H	L H	L H	no change no change	When A-to-B Source is low, the data at the A data port are clocked into the A storage flip-flops by a rising-edge signal on the A-to-B Clock.
	Bus B	lus A to	From I	н	x	L H	Q <sub>A</sub> Q <sub>A</sub>	L H	no change no change	4.) When A-to-B Source is high, the data at the A data port are clocked into the A storage flip-flops by a rising-edge signal on the A-to-B Clock. The states, Q <sub>A</sub> , of the storage flip-flops propagate directly to the B data port.
L	L					Output:	Input:			The output mode of the A data port is enabled and behaves according to the following logic equation:
		X*	H,L,~_	X	L	8 L H	L H	no change no change	no change no change	A=[B•(B-to-A Source)] +[Q <sub>B</sub> •(B-to-A Source)]  1.) When B-to-A Source is low, the data at the B data port are displayed at the A data port. The states of the storage flip-flops are not affected.
				X	Н	QB	X	no change	no change	When B-to-A Source is high, the states of the B storage flip-flops are displayed at the A data port.
		X*	5	X	L	L H	H JOHN SIDE	no change no change	L H	When B-to-A Source is low, the data at the B data port are clocked into the B storage flip-flops by a rising-edge signal on the B-to-A Clock.
				X USSI	H (S)	Q <sub>B</sub>	L H	no change no change	L H (6)	4.) When B-to-A Source is high, the data at the B data port are clocked into the B storage flip-flops by a rising-edge signal on the B-to-A Clock. The states, Q <sub>B</sub> , of the storage flip-flops propagate directly to the A data port.

<sup>\*</sup>The clocks are not internally gated with either the Output Enables or the Source inputs. Therefore, data at the A and B ports may be clocked into the storage flip-flops at any time.





Real-Time Transfer From Bus B to Bus A

#### TIMING DIAGRAMS AND SWITCHING DIAGRAMS - HC646

(The Diagrams For The HC648 Are The Same As Below, But With The Outputs Inverted)

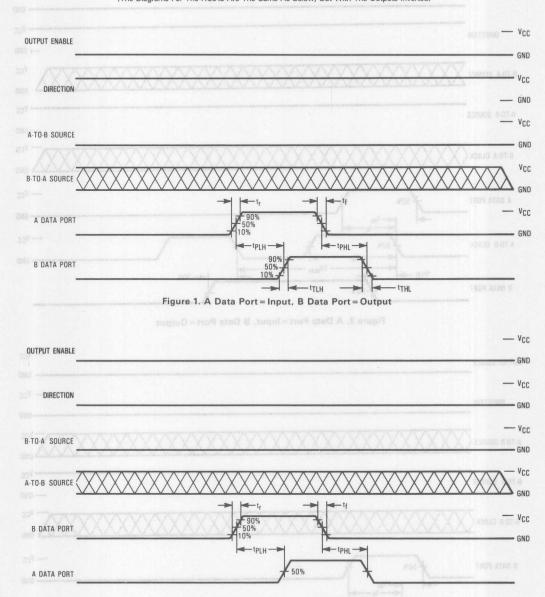


Figure 2. A Data Port = Output, B Data Port = Input

= Don't Care State

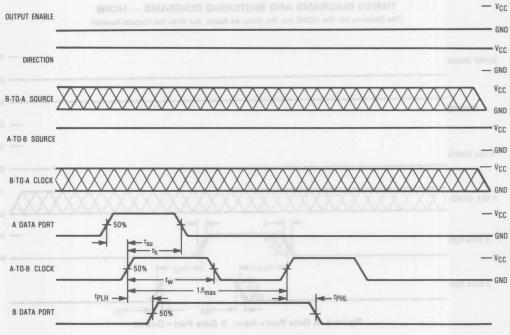


Figure 3. A Data Port = Input, B Data Port = Output

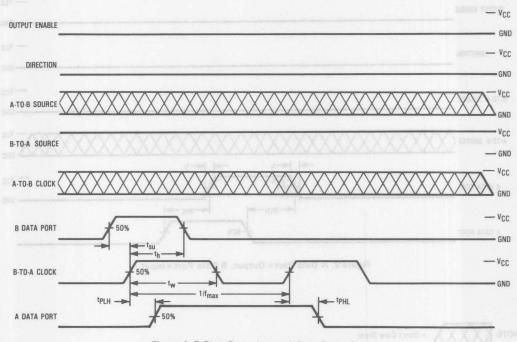
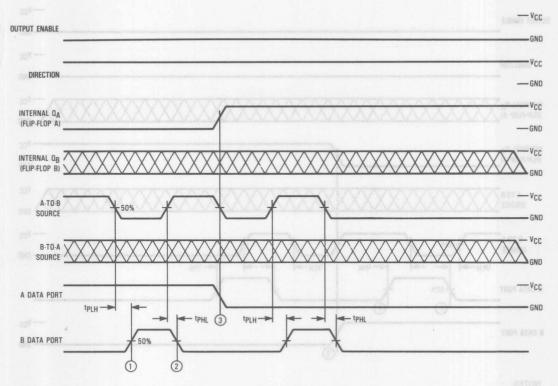


Figure 4. B Data Port = Input, A Data Port = Output



#### NOTES:

- 1. B Data Port (output) changes from the level of the storage flip-flop, Q<sub>A</sub>, to the level of A Data Port (input).
- 2. B Data Port (output) changes from the level of A Data Port (input) to the level of the storage flip-flop, QA.
- 3. The A storage flip-flop, A-to-B Source, and A Data Port (input) have simultaneously changed states.

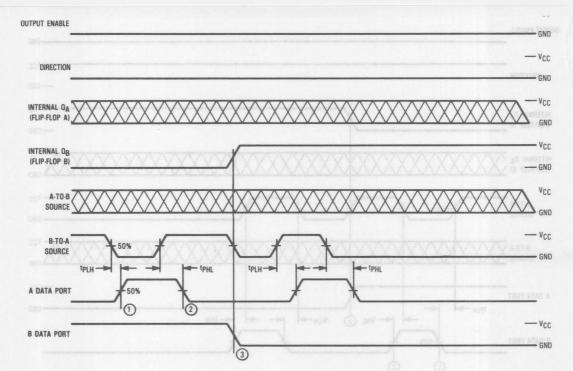
Figure 5. A Data Port = Input, B Data Port = Output

5

ource relection pine. Depending upon the states of the one the Function Table), deta at the outputs may con UTS/OUTFUTS

D-A7 (PINS 6-11) and 80-13 (PINS 25-13) — A and 8 ports. These pins may function either as inputs to or puts from the transceivers.

CONTROL INPUTS
OUTPUT ENABLE IFIN 21) — Active low output enable.
When this pin is low, the outputs are anabled and function
normality. When this pin is high, the A and B data ports are
in high-impedance states. See the Function Table.
DIRECTION IPIN 31 — Data election control. When the



#### NOTES:

- 1. A Data Port (output) changes from the level of the storage flip-flop, QB, to the level of B Data Port (input).
- 2. A Data Port (output) changes from the level of B Data Port (input) to the level of storage flip-flop, QB.
- 3. The B storage flip-flop, B-to-A Source, and B Data Port (input) have simultaneously changed states for the purpose of this example. A Data Port (output) is now displaying the voltage level of B Data Port (input).

Figure 6. A Data Port = Output, B Data Port = Input

## 5

#### PIN DESCRIPTIONS

#### INPUTS/OUTPUTS

A0-A7 (PINS 4-11) and B0-B7 (PINS 20-13) — A and B data ports. These pins may function either as inputs to or outputs from the transceivers.

#### **CONTROL INPUTS**

OUTPUT ENABLE (PIN 21) — Active-low output enable. When this pin is low, the outputs are enabled and function normally. When this pin is high, the A and B data ports are in high-impedance states. See the Function Table.

**DIRECTION (PIN 3)** — Data direction control. When the Output Enable pin is low, this control pin determines the direction of data flow. When Direction is high, the A data

ports are inputs and the B data ports are outputs. When Direction is low, the A data ports are outputs and the B data ports are inputs.

A-TO-B CLOCK, B-TO-A CLOCK (PINS 1, 23) — Clocks for the internal D flip-flops. With a low-to-high transition on the appropriate Clock pin, data on the A (or B) inputs are clocked into the internal A (or B) flip-flops. These clocks are not internally gated with the Output Enable or the Direction pins, therefore data at the A and B pins may be clocked into the storage flip-flops at any time.

A-TO-B SOURCE, B-TO-A SOURCE (PINS 2, 22) — Datasource selection pins. Depending upon the states of these pins (see the Function Table), data at the outputs may come either from the inputs or from the D flip-flops.

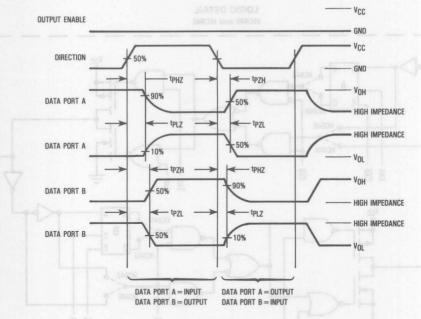


Figure 7

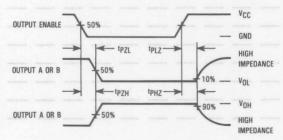


Figure 8

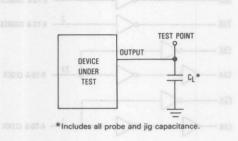


Figure 9. Test Circuit

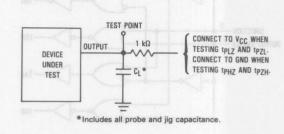
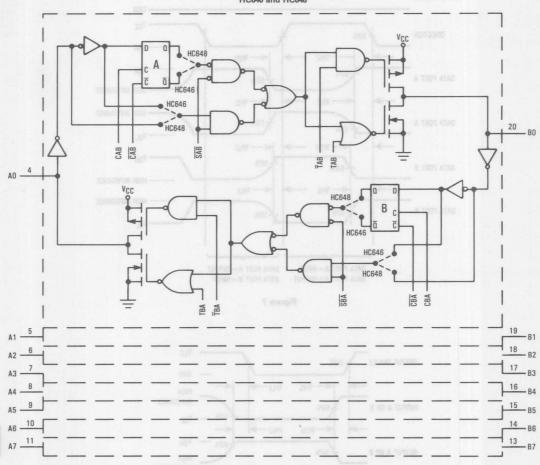
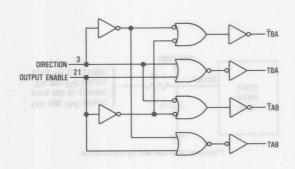
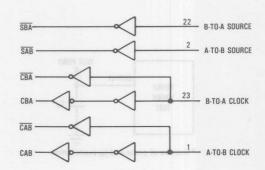


Figure 10. Test Circuit

LOGIC DETAIL HC646 and HC648







# Octal 3-State Bus Transceivers and D Flip-Flops

### **High-Performance Silicon-Gate CMOS**

The MC54/74HC651 and the MC54/74HC652 are identical in pinout to the LS651 and the LS652. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices are bus transceivers with D flip-flops. Depending on the status of the Data-Source Selection pins, data may be routed to the outputs either from the flip-flops or transmitted real-time from the inputs (see Function Table and Application Information).

The Output Enables, A-to-B (OEB) and B-to-A (OEA), control the transceiver's function. Bus A and Bus B cannot be routed as outputs to each other simultaneously, but can be routed as inputs to the A and B flip-flops simultaneously. Also, the A and B flip-flops can be routed as outputs to Bus A and Bus B simultaneously. Additionally, when either or both of the ports are in the high impedance state, these I/O pins may be used as inputs to the D flip-flops for data storage.

The user should note that because the clocks are not gated with the Output Enable pins, data at the A and B ports may be clocked into the storage flip-flops at any time.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 764 FETs or 191 Equivalent Gates

#### LOGIC DIAGRAM 20 BO AD 19 -B1 18\_B2 17\_B3 DATA DATA 16\_B4 PORT PORT 15 B5 A6 10 14\_B6 A7-11 13 -B7 OUTPUT OFA ENABLES FLIP-FLOP A-TO-B CLOCK CLOCKS B-TO-A CLOCK DATA-SOURCE ( A-TO-B SOURCE SELECTION 4 B-TO-A SOURCE PIN 24 = VCC INPUTS ( PIN 12 = GND

# MC54/74HC651 MC54/74HC652



MC74HCXXXDW SOIC  $T_A = -55^{\circ}$  to 125°C for all packages.

Dimensions in Chapter 7.

#### PIN ASSIGNMENT 24 D VCC 23 B-TO-A CLOCK A.TO.R 22 B-TO-A OEB [ 3 21 DOEA AO [ 20 BO A1 [ A2 0 6 19 B1 18 1 B2 A3 0 7 17 B3 A4 [ 16 B4 A5 [ 9 15 B5 A6 1 10 14 B6 A7 [ 13 B7 GND 12

HC651 - Inverting Outputs HC652 - Noninverting Outputs

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Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
VI/0	DC I/O Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	٧
lin	DC Input Current, per Pin	±20	mA
11/0	DC I/O Current, per Pin	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TLS TLS	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$  VCC.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O prins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to	GND)	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (	Referenced to GND)	0	Vcc	٧
TA	Operating Temperature, All Package	Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	NS 0 1 8-07-A			Guaranteed Limit			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>  ≤20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
V <sub>IL</sub> s	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  l <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
Vон	Minimum High-Level Output Voltage	Vin=V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	ACEST - Jovanning Qu	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND (Pins 1, 2, 3, 21, 22, or 23)	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND, I/O Pins	6.0	±0.5	±5.0	±10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μА

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

	Parameter state gold more and a more state gold more and a more state gold mor	V <sub>C</sub> C V	Guaranteed Limit			
Symbol			25°C to -55°C	≤85°C	≤125°C	Unit
fmax	Maximum Clock Frequency (50% Duty Cycle)	2.0	6.0	4.8	4.0	MHz
e and 8	(Figures 3, 4 and 8)	4.5 6.0	30 35	24 28	20 24	
tPLH,	Maximum Propagation Delay, Input A to Output B (or Input B to	2.0	170	215	255	ns
tPHL	Output A)	4.5	34	43	51	
a both	(Figures 1, 2 and 8)	6.0	29	37	43	
tPLH,	Maximum Propagation Delay, A-to-B Clock to Output B (or B-to-A Clock	2.0	220	275	330	ns
tPHL	to Output A)	4.5	44	55	66	
nite ine si	(Figures 3, 4 and 8)	6.0	37	47	56	
tPLH,	Maximum Propagation Delay, A-to-B Source to Output B (or B-to-A Source	2.0	170	215	255	ns
tPHL	to Output A) word Brown Array = B	4.5	34	43	51	
	(Figures 5, 6 and 8)	6.0	29	37	43	
tPLZ,	Maximum Propagation Delay, OEA or OEB to Output A or B	2.0	175	220	265	ns
tPHZ	(Figures 7 and 9)	4.5	35	44	53	
	are show-out sections and to satisfie	6.0	30	37	45	
tPZL,	Maximum Propagation Delay, OEA or OEB to Output A or B	2.0	175	220	265	ns
tPZH	(Figures 7 and 9)	4.5	35	44	53	
	5106	6.0	30	37	45	
tTLH,	Maximum Output Transition Time, Any Output	2.0	60	75	90	ns
THL	(Figures 1 and 8)	4.5	12	15	18	
an-A Bar	no large agle-grief it yil agait	6.0	10	13	15	
Cin	Maximum Input Capacitance		10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	-	15	15	15	pF

For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
 Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Channel)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
B edit is si	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	× 60	pF

#### TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

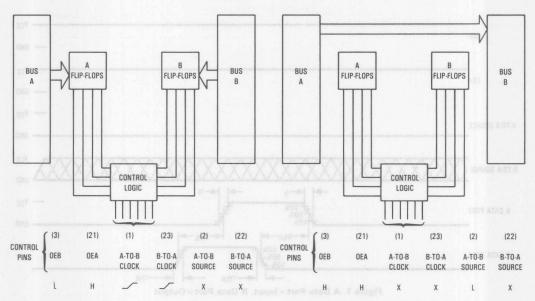
		V <sub>CC</sub>	Gua	E Ban		
Symbol	B edi ani bedada asa haa ani Parameter aasaada an 18 N		25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Input A to A-to-B Clock (or Input B to B-to-A Clock)	2.0	100	125	150	ns
	(Figures 3 and 4)	4.5	20	25	30	
	A deal register to the control of th	6.0	17	21	26	
th	Minimum Hold Time, A-to-B Clock to Input A (or B-to-A Clock to Input B)	2.0	5	5	5	ns
on the den	(Figures 3 and 4)	4.5	5	5	5	
	g sinh A arti et vitarrih enuscoru	6.0	5	5	5	
tw	Minimum Pulse Width, A-to-B Clock (or B-to-A Clock)	2.0	80	100	120	ns
no souther	(Figures 3 and 4)	4.5	16	20	24	
	displayed on the IB part and/or the IB	6.0	14	17	20	
tr, tf	Maximum Input Rise and Fall Times	2.0	1000	1000	1000	ns
	(Figure 1)	4.5	500	500	500	
	SECTION OF THE POLICE HEAVILLY LINES ON THE TIME OF SECTION OF THE SECTION OF	6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Control Inputs						Data Port Status		Storage Flip- Flop States		Symbol Pan
OEB	OEA	A-to-B Clock	B-to-A Clock	A-to-B Source	B-to-A Source	А	В	QA	αB	Description of Operation
L	Н	H, L,\	H, L, \	X	×	Input:	Input:	no change	no change	The output functions of the A and B ports and disabled.
un		365	215	-081	0.0	L	X	E E	X	The ports may be used as inputs to the storag
		19	69	36	8	Н	X	Н	X	flip-flops. Data at the inputs are clocked into th
	-	1	1	X	X	X	L	X	L H H	flip-flops with the rising edge of the Clocks.
- 301	-	83	225	220	1 1/2			A	09 - <b>n</b> - 0 - 0	7
Н	Н	33	47	18	0.	Input:	Output:			The outputs of the B data port are enabled an behave according to the following logic equation
		10	216	34	6. 6.	20114	2 A-01-8	sol @ spepal	20 20 20 20 20 20 20 20 20 20 20 20 20 2	$B = [A \circ (\overline{A - to - B \ Source})] + [Q_{A} \circ (A - to - B \ Source)]$
		X*	X*	- SK	×	L H	L H	no change no change	no change no change	When A-to-B Source is low, the data at the adata port are displayed at the B data port. The states of the storage flip-flops are not affected.
		205	220	H	×	X	QA	no change	no change	When A-to-B Source is high, the states of th A storage flip-flops are displayed at the B dat port.
		81	X*	L 00	×	L H	L H	L H	no change no change	When A-to-B Source is low, the data at the data port are clocked into the A storage flip flops by a rising-edge signal on the A-to-Clock.
		81	81	Н 88	×	L H	Q <sub>A</sub> Q <sub>A</sub>	H	no change no change	4.) When A-to-B Source is high, the data at the data port are clocked into the A storage flip flops by a rising-edge signal on the A-to- Clock. The states, Q <sub>A</sub> , of the storage flip-flop propagate directly to the B data port.
L	L					Output:	Input:	A YasqarQ A	ballet ed a	The outputs of the A data port are enabled an behave according to the following logic equation
		0.0=5	3 2°8	(i) teolo				evitamoeno	(tonnest2	$A = [B \bullet (B-to-A Source)] + [Q_B \bullet (B-to-A Source)]$
70		X*	X*	Х	L	L H	L H	no change no change	no change no change	When B-to-A Source is low, the data at the data port are displayed at the A data port. The states of the storage flip-flops are not affected.
				×	Н	QB	х	no change	no change	When B-to-A Source is high, the states of th B storage flip-flops are displayed at the A dat port.
Sini		X*	0.488%	×	8 2	V L	H	no change no change	H	When B-to-A Source is low, the data at the data port are clocked into the B storage flip flops by a rising-edge signal on the B-to-y
		180	128	00	0	celt) 2	D.A-01-B	or 9 rugal to	a Design of	Clock.
		36	85 15	Х	н	Q <sub>B</sub>	L H	no change no change	L H	4.) When B-to-A Source is high, the data at the data port are clocked into the B storage flip
		0 0	8 8	8 8	8.0	5 5	gal Gl 35	ALP A-OF ID	as A sugal o	flops by a rising-edge signal on the B-to-/ Clock. The states, QB, of the storage flip-flop propagate directly to the A data port.
Has	L	X*	X*	H 86	На	Output: QB	Output: Q <sub>A</sub>	no change	no change	When A-to-B Source and/or B-to-A Source ar high, then states of the A storage flip-flops ar displayed on the B port and/or the state of the storage flip-flops are displayed on the A port.

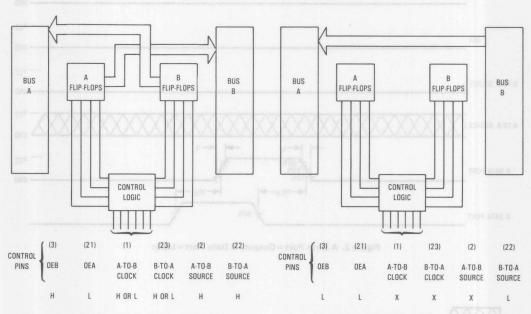
<sup>\*</sup>The clocks are not internally gated with either the Output Enables or the Source inputs. Therefore, data at the A and B ports may be clocked into the storage flip-flops at any time.

#### TYPICAL APPLICATIONS



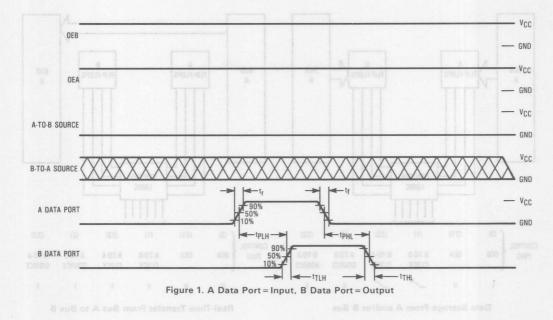
Data Storage From A and/or B Bus

Real-Time Transfer From Bus A to Bus B



Transfer Stored Data To A and/or B Bus

Real-Time Transfer From Bus B to Bus A



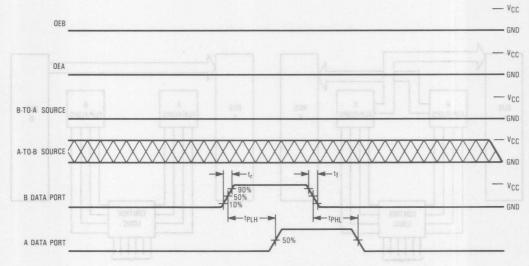


Figure 2. A Data Port = Output, B Data Port = Input

GND -VCC

— GND — V<sub>CC</sub>

- GND

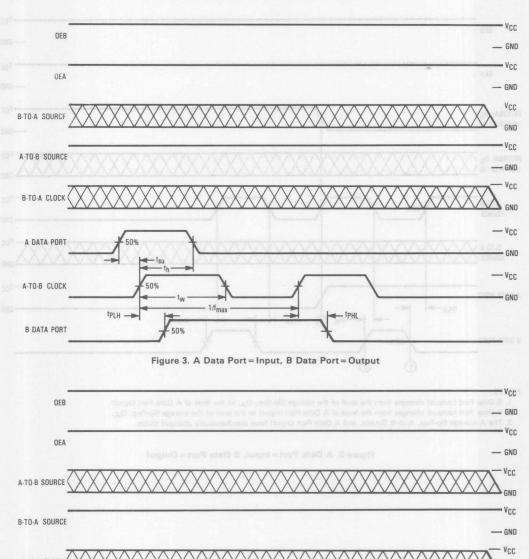


Figure 4. B Data Port = Input, A Data Port = Output

B DATA PORT

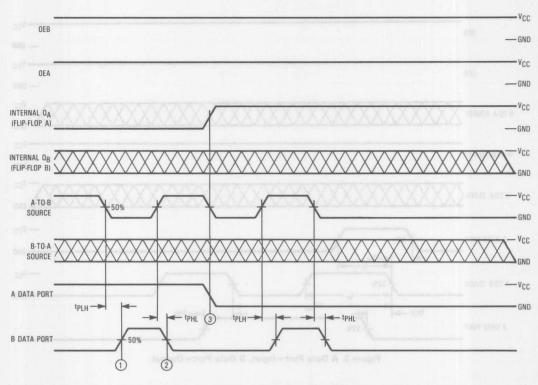
B-TO-A CLOCK

A DATA PORT

50%

50%

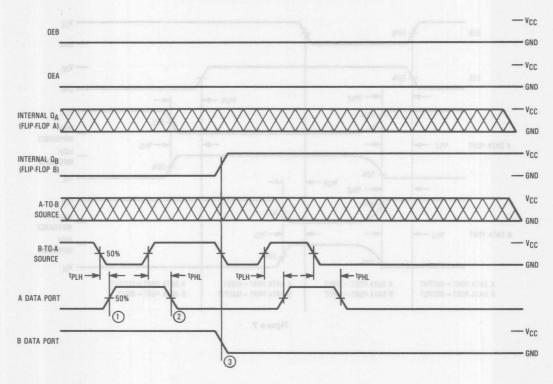
tPLH -



#### NOTES

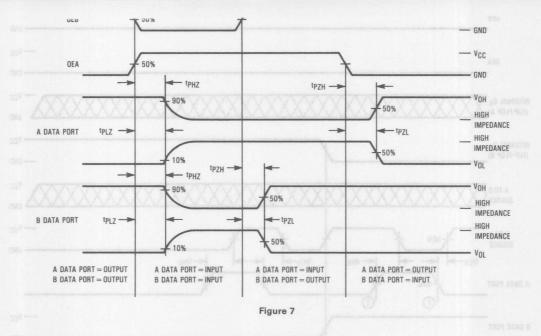
- 1. B Data Port (output) changes from the level of the storage flip-flop, QA, to the level of A Data Port (input).
- 2. B Data Port (output) changes from the level of A Data Port (input) to the level of the storage flip-flop, Q<sub>A</sub>.
- 3. The A storage flip-flop, A-to-B Source, and A Data Port (input) have simultaneously changed states.

Figure 5. A Data Port = Input, B Data Port = Output



- A Data Port (output) changes from the level of the storage flip-flop, Q<sub>B</sub>, to the level of B Data Port (input).
   A Data Port (output) changes from the level of B Data Port (input) to the level of storage flip-flop, Q<sub>B</sub>.
- 3. The B storage flip-flop, B-to-A Source, and B Data Port (input) have simultaneously changed states for the purpose of this example. A Data Port (output) is now displaying the voltage level of B Data Port (input).

Figure 6. A Data Port = Output, B Data Port = Input



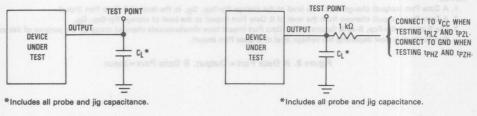
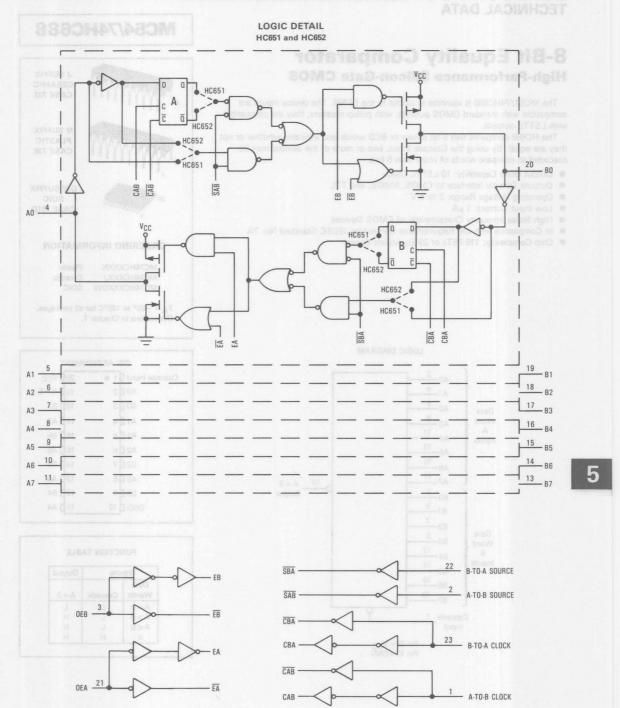


Figure 8. Test Circuit

Figure 9. Test Circuit



# 8-Bit Equality Comparator High-Performance Silicon-Gate CMOS

The MC54/74HC688 is identical in pinout to the LS688. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTIL outputs.

The HC688 compares two 8-bit binary or BCD words and indicates whether or not they are equal. By using the Cascade Input, two or more of the devices may be cascaded to compare words of more than 8 bits.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 116 FETs or 29 Equivalent Gates

# MC54/74HC688



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



DW SUFFIX SOIC CASE 751D

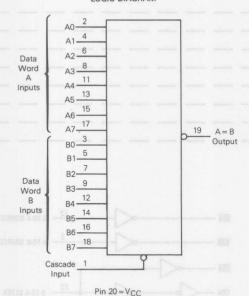
### ORDERING INFORMATION

MC74HCXXXN MC54HCXXXJ MC74HCXXXDW

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM



Pin 10=GND

#### PIN ASSIGNMENT Cascade Input 1 1 20 VCC A0 0 2 19 A = B 18 B7 BO 13 17 D A7 A1 I 16 B6 B1 5 15 A6 A2 0 6 B2 C 14 B5 13 A5 A3 08 B3 0 9 12 B4 11 A4 GND 10

### FUNCTION TABLE

Inp	outs	Output
Data Words	Cascade	<b>A</b> =B
A = B	L	L
A>B	L	Н
A <b< td=""><td>L</td><td>Н</td></b<>	L	Н
X	Н	Н

1707111110	TO T	RELEASE AND THE PERSON AND	100 Table 100
Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	no V. rug
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	DAVIDO SALVA	2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Refere	enced to GND)	0	Vcc	٧
TA	Operating Temperature, All Package Type	Operating Temperature, All Package Types		+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> =2.0 V	0	1000	ns
47.4	(Figure 2)	V <sub>CC</sub> =4.5 V	0	500	
		Vcc = 6.0 V	0	400	

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	JACO JACO	green courts		Guaranteed Limit			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Uni
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	± 1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

<sup>†</sup>Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

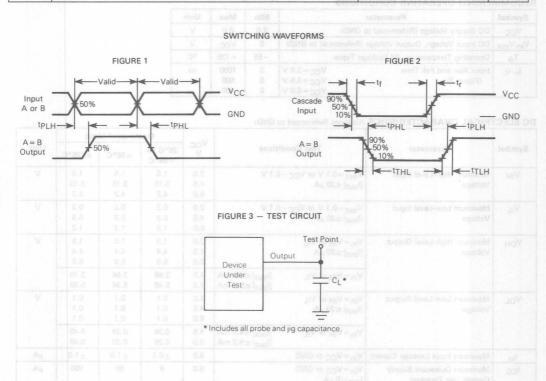
	This device contains pr			Gua			
Symbol	drouter to grand spaints	Parameter 0.1 + or 8.0	V	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay (Figures 1 and 3)	, Input A or B to Output A =	B 2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
tPLH, tPHL	Maximum Propagation Delay (Figures 2 and 3)	, Cascade Input to Output A	= B 2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
tTLH, tTHL	Maximum Output Transition (Figures 2 and 3)	Time, Any Output	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	085	16gaxisaP 31922 10	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

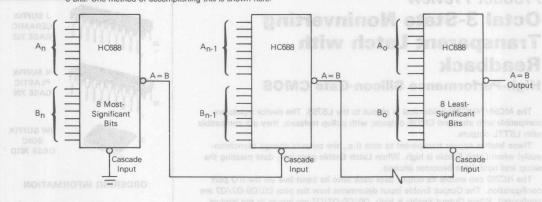
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption: PD = CPD VCC <sup>2</sup> f+ICC VCC	30	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

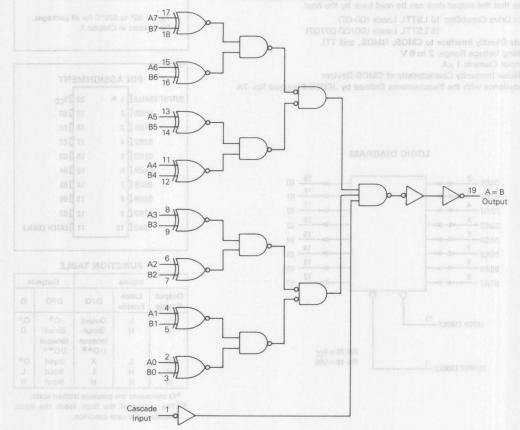


### TYPICAL APPLICATION

Two or more HC688 8-bit Equality Comparators may be cascaded to compare binary or BCD numbers having more than 8 bits. One method of accomplishing this is shown here.



### EXPANDED LOGIC DIAGRAM



## Product Preview

# **Octal 3-State Noninverting Transparent Latch with** Readback

### **High-Performance Silicon-Gate CMOS**

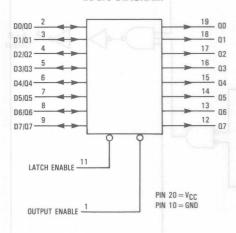
The MC54/74HC793 is identical in pinout to the LS793. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold times becomes latched.

The HC793 can enable its output data back onto its input bus via the I/O port configuration. The Output Enable input determines how the pins D0/Q0-D7/Q7 are configured. When Output Enable is high, D0/Q0-D7/Q7 are inputs to the latches, configuring D0/Q0-D7/Q7 as an input bus. When Output Enable is low, the outputs of the latches are enabled on D0/Q0-D7/Q7, configuring D0/Q0-D7/Q7 as an output bus so that the output data can be read back by the host.

- Output Drive Capability: 10 LSTTL Loads (Q0-Q7) 15 LSTTL Loads (D0/Q0-D7/Q7)
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A

### LOGIC DIAGRAM



### MC54/74HC793



J SUFFIX CERAMIC **CASE 732** 



N SUFFIX PLASTIC **CASE 738** 



DW SUFFIX SOIC CASE 751D

### ORDERING INFORMATION

MC74HCXXXN MC54HCXXX.I MC74HCXXXDW

Plastic Ceramic SOIC

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### PIN ASSIGNMENT

	710011	3141412	
OUTPUT ENABLE	1 •	20	I v <sub>CC</sub>
D0/Q0 [	2	19	00
D1/Q1 [	3	18	01
D2/Q2 [	4	17	02
D3/03 [	5	16	<b>1</b> a3
D4/Q4 [	6	15	04
D5/Q5 [	7	14	05
D6/Q6 [	8	13	06
D7/Q7 [	9	12	07
GND [	10	11	LATCH ENABLE

### **FUNCTION TABLE**

Inputs			Outputs		
Output Enable	Latch Enable	D/Q	D/Q	Q	
L	L	Output	Ω*	Q*	
L	Н	Simul-	Simul-	D	
		taneous I/O**	taneous I/O**		
H	L	X	Input	0*	
H-O	Н	L	Input	L	
H	Н	Н	Input	Н	

\*Q represents the previous latched state. \*\*The output of the latch feeds the input, resulting in a race condition.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

IAXIMU	M RATINGS*	Seat stand July 30	= 101 BS
Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin (Pins 1, 11)	±20	mA
lout	DC Output Current, per Pin (Pins 12-19)	± 25	mA
11/0	DC Output Current, per Pin (Pins 2-9)	±35	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GN	D)	2.0	6.0	٧
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package T	Operating Temperature, All Package Types		+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> =2.0 V	0	1000	ns
	(Figure 1)	V <sub>CC</sub> =4.5 V	0	500	
	A even Disk to en di munita	V <sub>CC</sub> =6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

		Lid spon no prival based	e l paro	Guaranteed Limit			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V or } V_{\text{CC}} = 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
Vон	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
	8 8 8 8 000T 0001 000F 008 008 968	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 6.0 \text{ mA}$ Pins 2-9 $ I_{\text{out}}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	Ar of
	400 400 400	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 4.0 \text{ mA}$ Pins 12-19 $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}} \qquad  I_{\text{out}}  \le 6.0 \text{ mA}$ Pins 2-9 $ I_{\text{out}}  \le 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
		$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}} $ $ I_{\text{out}}  \le 4.0 \text{ mA}$ Pins 12-19 $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	± 1.0	μΑ
loz	Maximum Three-State Leakage Current	Output in High-Impedance State  V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	± 10.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

or Vout/ ≤ VCC.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or VCC). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C1 = 50 pF, Input tr=tf=6 ns)

	Integration solves and an arranged brang of years against dight or solt and against dight or solt and arranged branged by all and a solution of the solution o	Voluv		Gua	Symbol		
Symbol			CC V	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay, Input Data to (	2 33V or d.9- 2	2.0	150	190	225	ns
tPHL	(Figures 1 and 5)		1.5 3.0	30 26	38	45 38	nt.
tPLH, tPHL	Maximum Propagation Delay, Latch Enable to (Figures 2 and 5)	4	2.0 1.5	175 35	220 44	265 53	ns
ATT SEAR	office on or no-to rectal		5.0	30	37	45	3.7
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable (Figures 3 and 6)		2.0 4.5	150 30	190 38	225 45	ns
nucture ha	mind America Cité Dandin	81 + or 89 - 6	6.0	26	33	38	Faste
tPZL, tPZH	Maximum Propagation Delay, Output Enable (Figures 3 and 6)	10 C Package) 280	2.0 4.5 3.0	150 30 26	190 38 33	225 45 38	ns
tTLH,	Maximum Output Transition Time, D0/Q0-D7	/07	2.0	60	75	90	ns
<sup>t</sup> THL	.601		1.5 3.0	12	15 13	18 15	nedone enderet
tTLH,	Maximum Output Transition Time, Q0-Q7 (Figures 1 and 5)	0°321 014	2.0 4.5 5.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance (Pins 1, 11)		UP TO	10	10	10	pF
Cout	Maximum I/O Capacitance (I/O in High-Impe (Output Enable = VIH)	dance State)	Ma) o	15	15 agarloV y	15 Iggue 20	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Latch)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	postovi SOTTRIRETTO TBD HO JAOHATI	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

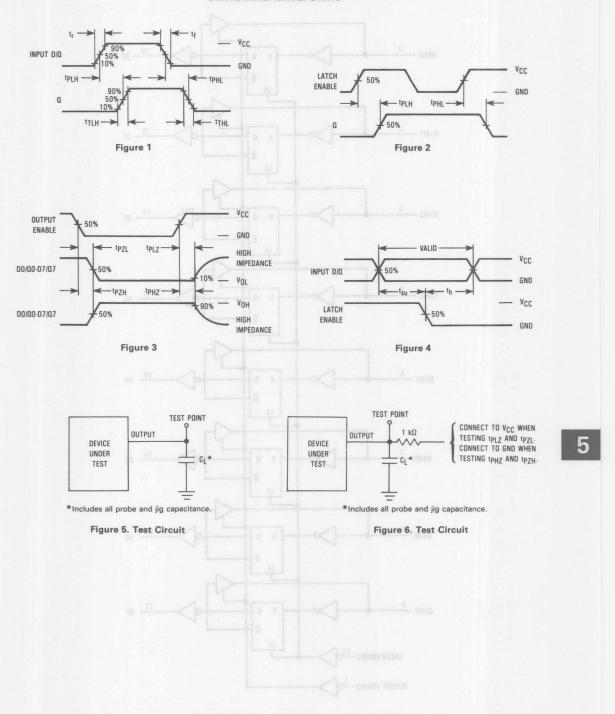
### TIMING REQUIREMENTS (Input to = te = 6 ns)

	31.5 3.15 3.15 3.15 3.15 3.15 3.15		Gua	511.0		
Symbol	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Input Data to Latch Enable	2.0	100	125	150	ns
	(Figure 4)	4.5	20	25	30	
V.	91 91 91 92 19	6.0	17	21	26	
th	Minimum Hold Time, Latch Enable to Input Data	2.0	5	5	5	ns
	(Figure 4) 6.8 6.8 6.8	4.5	5	5	5	
	GC P 48 C 86 E P 8 Am U 8 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	6.0	5	5	5	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	2.0	1000	1000	1000	ns
	(Figure 1)	4.5	500	500	500	
	OV.5 ES.E SEE GA AM 0.9 2 Inch HV IS	6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

### MC54/74HC793

### **SWITCHING WAVEFORMS**



5

D Q

E LE

D7/Q7 -

LATCH ENABLE 110

OUTPUT ENABLE -

# **Dual 4-Input NOR Gate**

### **High-Performance Silicon-Gate CMOS**

The MC54/74HC4002 is identical in pinout to the MC14002B and MC14002UB. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 28 FETs or 7 Equivalent Gates

# MC54/74HC4002



J SUFFIX CERAMIC **CASE 632** 



N SUFFIX PLASTIC **CASE 646** 



D SUFFIX SOIC CASE 751A

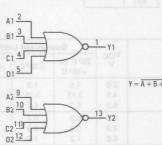
### ORDERING INFORMATION

MC74HCXXXXN MC54HCXXXXJ MC74HCXXXXD

Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM



 $Y = \overline{A + B + C + D}$ 

PIN 14 = VCC PIN 7 = GND

PINS 6, 8 = NO CONNECTION

### PIN ASSIGNMENT

1 114	ASSIC	TIAIAIT	1 1 1
Y1 [	1 •	14	vcc
A1 [	2	13	] Y2
B1 [	3	12	D2
C1 [	4	11	C2
D1 [	5	10	] B2
NC [	6	9	] A2
GND [	7	8	NC

NC = NO CONNECTION

### **FUNCTION TABLE**

Inputs			Output	
Α	В	С	D	Y
L	L	L	L	Н
Н	X	X	X	L
X	Н	X	X	L
X	X	Н	X	L
X	X	X	Н	L

X = don't care

### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
Vcc	DC Supply Voltage (Referenced to GN	2.0	6.0	V	
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Re	0	Vcc	V	
TA	Operating Temperature, All Package Types			+ 125	°C
tr, tf	Input Rise and Fall Time	V <sub>CC</sub> = 2.0 V	0	1000	ns
	(Figure 1)	$V_{CC} = 4.5 \text{ V}$	0	500	
		$V_{CC} = 6.0 \text{ V}$	0	400	

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Parameter Test Conditions				Gua	imit		
Symbol			nditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL MO	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
Y	A B C D	Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL Maximum Low-Level Output Voltage		$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	H X X X	Vin=VIH or VIL	I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	± 1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA		6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

### AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol			Gua			
	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	MIZ IN	10	10	10	pF

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	ed so the
	Used to determine the no-load dynamic power consumption:	metal-gate CMOS analog switch	ROMER
	PD = CPD VCC <sup>2</sup> f + ICC VCC	26 milestrant	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	tradicants dilius atdisessores con	muneil hard

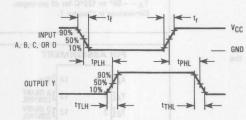
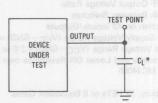


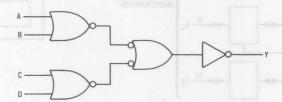
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM
(½ of the Device)



# Advance Information

# Quad Analog Switch/ Multiplexer/Demultiplexer High-Performance Silicon-Gate CMOS

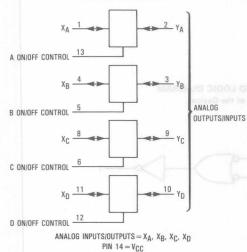
The MC54/74HC4016 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from V<sub>CC</sub> to GND).

The HC4016 is identical in pinout to the metal-gate CMOS MC14016 and MC14066. Each device has four independent switches. The device has been designed so that the ON resistances (R<sub>ON</sub>) are much more linear over input voltage than R<sub>ON</sub> of metal-gate CMOS analog switches.

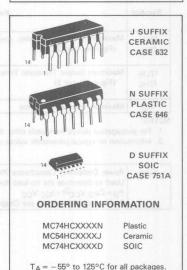
This device is identical in both function and pinout to the HC4066. The ON/OFF Control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the HC4316. For analog switches with lower  $R_{\mbox{\scriptsize ON}}$  characteristics, use the HC4066.

- · Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range (VCC GND) = 2.0 to 12.0 Volts
- Analog Input Voltage Range (V<sub>CC</sub> GND) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise
- Chip Complexity: 32 FETs or 8 Equivalent Gates

### LOGIC DIAGRAM



# MC54/74HC4016



### 

Dimensions in Chapter 7.

0 1011 0	0
On/Off Control	State of
Input	Analog Switch
L	Off
H	On

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN 7 = GND

# 5

### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	Positive DC Supply Voltage (Referenced to GND)	-0.5 to +14.0	V
VIS	Analog Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
Vin	Digital Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
1	DC Current Into or Out of Any Pin	± 25	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 65° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \! \leq \! (V_{in})$  or  $V_{out}) \! \leq \! V_{CC}$ .

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	tolore for		Paramete	r	and gunstalasy	Min	Max	Unit
Vcc	Positive DC Supply Voltage (Referenced to GND)					2.0	12.0	V
VIS	Analog Inp	out Voltage	Reference	d to GNE	))	GND	Vcc	V
Vin	Digital Inpo	ut Voltage (I	Referenced	to GND		GND	Vcc	V
V <sub>IO</sub> *	Static or Dynamic Voltage Across Switch					190	1.2	V
TA	Operating Temperature, All Package Types					- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time, ON/OFF Control Inputs (Figure 10)							ns
	35				V <sub>CC</sub> =2.0 V	0	1000	
	81				V <sub>CC</sub> = 4.5 V	0	500	
	15				V <sub>CC</sub> =9.0 V	0	400	
	31				V <sub>CC</sub> = 12.0 V	0	250	

<sup>\*</sup>For voltage drops across the switch greater than 1.2 V (switch on), excessive V<sub>CC</sub> current may be drawn, i.e., the current out of the switch may contain both V<sub>CC</sub> and switch input components. The reliability of the device will be unaffected uless the Maximum Ratings are exceeded.

### DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND)

	LE 25 50	10.0		Guaranteed Limit			
Symbol	Parameter Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Voltage	R <sub>on</sub> = per spec	2.0	1.5	1.5	1.5	V
	ON/OFF Control Inputs	- Joseph	4.5	3.15	3.15	3.15	
	0.7 3.5 5.5	/ Ageurations	9.0	6.3	6.3	6.3	
			12.0	8.4	8.4	8.4	133
VIL	Maximum Low-Level Voltage	Ron = per spec	2.0	0.3	0.3	0.3	V
	ON/OFF Control Inputs	und in Chapter 4.	4.5	0.9	0.9	0.9	
			9.0	1.8	1.8	1.8	
			12.0	2.4	2.4	2.4	
lin	Maximum Input Leakage Current, ON/OFF Control Inputs	V <sub>in</sub> =V <sub>CC</sub> or GND	12.0	±0.1	±1.0	± 1.0	μΑ
Icc	Maximum Quiescent Supply	Vin=VCC or GND	6.0	2	20	40	μΑ
	Current (per Package)	V <sub>IO</sub> = 0 V	12.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

	This divine contains	title enlaw		Guaranteed Limit			Symbol
Symbol	Parameter	V Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
Ron	Maximum "ON" Resistance	$V_{IN} = V_{IH}$ $V_{IS} = V_{CC} \text{ to GND}$ $I_{S} \le 2.0 \text{ mA (Figures 1, 2)}$	2.0† 4.5 9.0 12.0	320 170 170	400 215 215	- 480 255 255	Ω
	beestion, V <sub>In</sub> and V <sub>oct</sub> controlled to the range C or V <sub>out</sub> ) s V <sub>CC</sub> Unused inputs next ave	$V_{\text{IN}} = V_{\text{IH}}$ $V_{\text{IS}} = V_{\text{CC}}$ or GND (Endpoints) $I_{\text{S}} \le 2.0$ mA (Figures 1, 2)	2.0 4.5 9.0 12.0	180 135 135	225 170 170	270 205 205	gha <sup>T</sup>
ΔR <sub>on</sub>	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$\begin{aligned} &V_{\text{IR}} = V_{\text{IH}} \\ &V_{\text{IS}} = 1/2 \; (V_{\text{CC}} - \text{GND}) \\ &I_{\text{S}} \leq 2.0 \; \text{mA} \end{aligned}$	2.0 4.5 9.0 12.0	30 20 20	35 25 25	40 30 30	Ω Maximum Functional Detailing
l <sub>off</sub>	Maximum Off-Channel Leakage Current, Any One Channel	Vin = V <sub>IL</sub> V <sub>IO</sub> = V <sub>CC</sub> or GND Switch Off (Figure 3)	12.0	0.1	0.5	1.0	μ <b>Α</b>
lon	Maximum On-Channel Leakage Current, Any One Channel	Vin = VIH VIS = VCC or GND (Figure 4)	12.0	0.1 GMOD 8	0.5	1.0	μ <b>Α</b> ИМООЭ

†At supply voltage (V<sub>CC</sub> – GND) approaching 2 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals. NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

### AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, ON/OFF Control Inputs: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

			1 801 4 1 82		Gu	imit	AT	
Symbol		Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit	
tPLH,	Maximum Propagation De	elay, Analog I	nput to Analog Output	2.0	50	65	75	ns
tPHL	(Figures 8 and 9)		VCC-4.5 V 0 600	4.5	10	13	15	
			00F 8 V 0.6 - 50V	9.0	10	13	15	
			Marc = 18.0 V 0 1 280	12.0	10	13	15	
tPLZ,	Maximum Propagation De	elay, ON/OFF	Control to Analog Output	2.0	150	190	225	ns
tPHZ	(Figures 10 and 11)		wall for and water input compone	4.5	30	38	45	
			tidnum Refings are expeeded.	9.0	30	38	45	
				12.0	30	38	45	
tPZL,	Maximum Propagation De	elay, ON/OFF	Control to Analog Output	2.0	125	160	185	ns
tPZH	(Figures 10 and 11)		SMS or hisonamed sagettev) notice	4.5	25	32	37	
	Supportuged Little			9.0	25	32	37	
shall		30	Fore Constitution	12.0	25	32	37	
С	Maximum Capacitance	* 65 V	ON/OFF Control Input	-	10	10	10	pF
	1.5		Control Input = GND		noistic		muovinitet	
	177		A -1 - 1/O	-	35	35	35	
	Sign Co.			-	1.0	1.0	1.0	

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

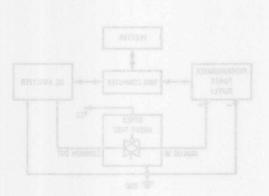
CPD	Power Dissipation Capacitance (Per Switch) (Figure 13)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	EDINATE CONTROL	nF
	For load considerations, see Chapter 4 subject listing on page 4-2.	Moormum Quintonnt Supply	201

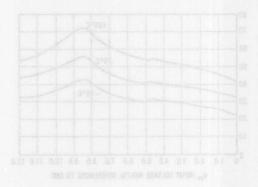
ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND unless noted)

Symbol	Parameter	Test Conditions	V <sub>CC</sub>	Limit* 25°C 54/74HC	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	f <sub>in</sub> = 1 MHz Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>OS</sub> Increase f <sub>in</sub> Frequency Until dB Meter Reads -3 dB R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	4.5 9.0 12.0	150 160 160	MHz
	Off-Channel Feedthrough Isolation (Figure 6)	$ \begin{aligned} f_{In} &\equiv \text{Sine Wave} \\ &\text{Adjust } f_{In} \text{ Voltage to Obtain 0 dBm at V}_{IS} \\ &f_{In} = 10 \text{ kHz}, \text{ R}_{L} = 600 \Omega, \text{ C}_{L} = 50 \text{ pF} \end{aligned} $	4.5 9.0 12.0	- 50 - 50 - 50	dB
8 4.0	0.5 2.5 0.5 2.5 0.5 2.5	$f_{in}$ = 1.0 MHz, $R_L$ = 50 $\Omega$ , $C_L$ = 10 pF	4.5 9.0 12.0	-40 -40 -40	0
0 680 T	Feedthrough Noise, Control to Switch (Figure 7)	$V_{in} \le 1$ MHz Square Wave ( $t_r = t_f = 6$ ns) Adjust R <sub>L</sub> at Setup so that $I_S = 0$ A R <sub>L</sub> = 600 $\Omega$ , C <sub>L</sub> = 50 pF	4.5 9.0 12.0	60 130 200	mVpp
		$R_L = 10 \text{ k}\Omega$ , $C_L = 10 \text{ pF}$	4.5 9.0 12.0	30 65 100	
-	Crosstalk Between Any Two Switches (Figure 12)	$f_{in} \stackrel{.}{=} \text{Sine Wave}$ Adjust $f_{in}$ Voltage to Obtain 0 dBm at V <sub>IS</sub> $f_{in} = 10 \text{ kHz}$ , $R_L = 600 \Omega$ , $C_L = 50 \text{ pF}$	4.5 9.0 12.0	-70 -70 -70	dB
		$f_{in}$ = 1.0 MHz, $R_L$ = 50 $\Omega$ , $C_L$ = 10 pF	4.5 9.0 12.0	-80 -80 -80	120
THD	Total Harmonic Distortion (Figure 14)	$f_{in}$ = 1 kHz, $R_L$ = 10 k $\Omega$ , $C_L$ = 50 pF THD=THDMeasured - THDSource $V_{IS}$ = 4.0 Vpp sine wave $V_{IS}$ = 8.0 Vpp sine wave $V_{IS}$ = 11.0 Vpp sine wave	4.5 9.0 12.0	0.10 0.06 0.04	%

\*Guaranteed limits not tested. Determined by design and verified by qualification.

Figure 1s. Typical On Resistance. VCC





### MC54/74HC4016

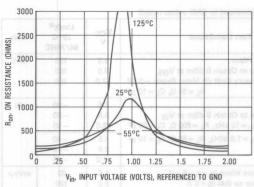


Figure 1a. Typical On Resistance, V<sub>CC</sub>=2.0 V

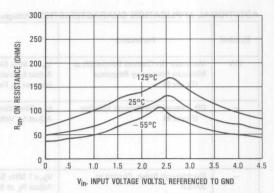


Figure 1b. Typical On Resistance, V<sub>CC</sub> = 4.5 V

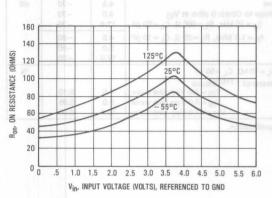


Figure 1c. Typical On Resistance, V<sub>CC</sub> = 6.0 V

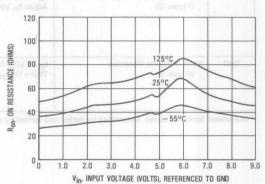


Figure 1d. Typical On Resistance, V<sub>CC</sub> = 9.0 V

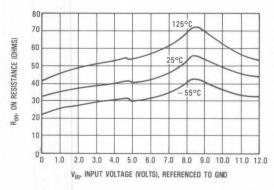


Figure 1e. Typical On Resistance, VCC = 12.0 V

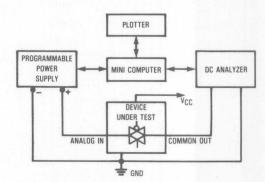


Figure 2. On Resistance Test Set-Up

Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

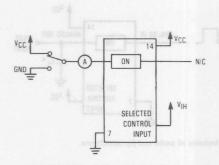
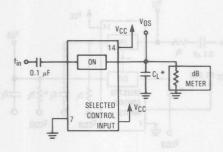
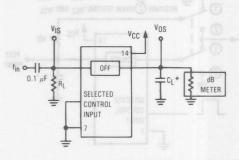


Figure 4. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



\*Includes all probe and jig capacitance.

Figure 5. Maximum On-Channel Bandwidth
Test Set-Up



\*Includes all probe and jig capacitance.

Figure 6. Off-Channel Feedthrough Isolation, Test Set-Up

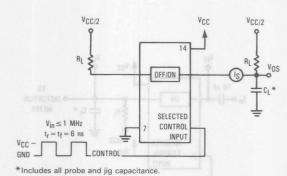


Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up

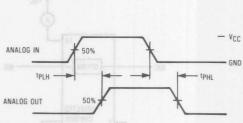
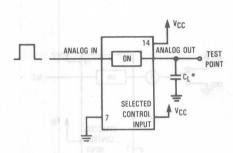


Figure 8. Propagation Delays, Analog In to Analog Out

### MC54/74HC4016



\*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set-Up

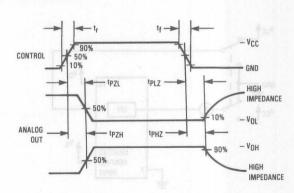
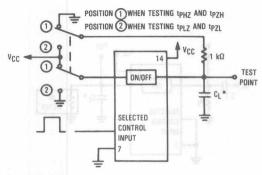


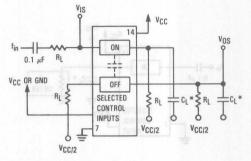
Figure 10. Propagation Delay, ON/OFF Control to Analog Out



\*Includes all prope and jig capacitance.

5

Figure 11. Propagation Delay Test Set-Up



\*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

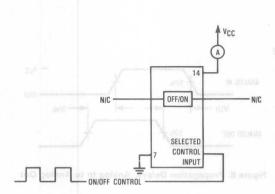
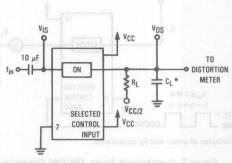


Figure 13. Power Dissipation Capacitance Test Set-Up



\*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set-Up

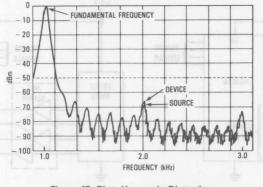


Figure 15. Plot, Harmonic Distortion

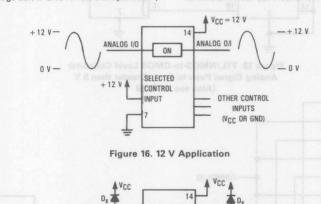
### **APPLICATION INFORMATION**

The ON/OFF Control pins should be at V<sub>CC</sub> or GND logic levels, V<sub>CC</sub> being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V<sub>CC</sub> or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and GND. The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below GND. In the example below,

the difference between V<sub>CC</sub> and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above VCC and/or below GND are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with MO-sorbs (Motorola high current surge protectors). MO-sorbs are fast turn-on devices ideally suited for precise DC protection with no inherent wear-out mechanism.



V<sub>CC</sub> = SELECTED CONTROL INPUT (V<sub>CC</sub> OR GND)

Figure 17. Transient Suppressor Application

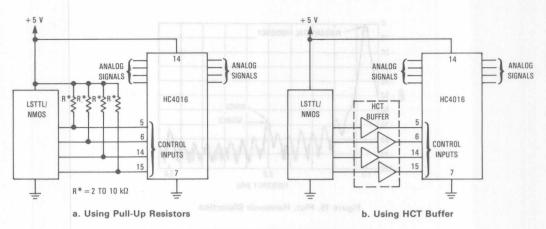


Figure 18. LSTTL/NMOS to HCMOS Interface

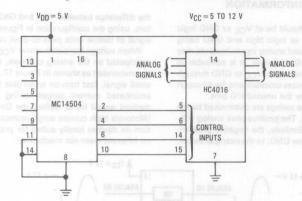


Figure 19. TTL/NMOS-to-CMOS Level Converter Analog Signal Peak-to-Peak Greater than 5 V (Also see HC4316)

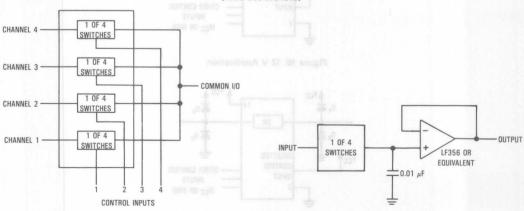


Figure 20. 4-Input Multiplexer Figure 21. Sample/Hold Amplifier

# **Decade Counter**High-Performance Silicon-Gate CMOS

The MC54/74HC4017 is identical in pinout to the standard CMOS MC14017B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC4017 uses a five stage Johnson counter and decoding logic to provide high-speed operation. This device also has an active-high, as well as active-low clock input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 176 FETs or 44 Equivalent Gates

## MC54/74HC4017



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

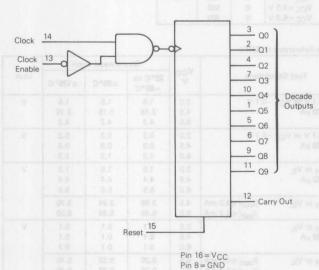
### ORDERING INFORMATION

MC74HCXXXXN MC54HCXXXXJ MC74HCXXXXD

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.





### PIN ASSIGNMENT

Q5 <b>C</b>	10	16	I V <sub>CC</sub>
Q1 C	2	15	Reset
Q0 <b>E</b>	3	14	Clock
Q2 [	4	13	Clock Enable
Q6 [	5	12	Carry Out
Q7 [	6	11	Q9
Q3 <b>[</b>	7	10	I Q4
GND [	8	9	Q8

### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
VCC	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL HUR Q	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND≤(Vin or Vout)≤VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced	to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	CC = 2.0 V CC = 4.5 V CC = 6.0 V	0 0 0	1000 500 400	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	00 03 100	100		Gua			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VILSO	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	± 1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

<sup>†</sup>Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C and published a 33°C and published enumanium R set of warming and on the set of warming and on the set of the s

### MC54/74HC4017

### AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	Ousrameed Cimit	.,	Gua			
Symbol	Pastre Orane Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 9)	2.0 4.5 6.0	4.0 20 24	3.2 16 19	2.6 13 15	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to Q (Figures 1 and 9)	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
tPLH, tPHL	Maximum Propagation Delay, Clock to Carry Out (Figures 2 and 9)	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
tPLH, tPHL	Maximum Propagation Delay, Reset to Q (Figures 3 and 9)	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
<sup>t</sup> PLH	Maximum Propagation Delay, Reset to Carry Out (Figures 3 and 9)	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
tPLH, tPHL	Maximum Propagation Delay, Clock Enable to Q (Figures 4 and 9)	2.0 4.5 6.0	250 50 43	315 63 54	375 75 64	ns
tPLH, tPHL	Maximum Propagation Delay, Clock Enable to Carry Out (Figures 5 and 9)	2.0 4.5 6.0	250 50 43	315 63 54	375 75 64	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 8 and 9)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	id = 3 a	10	10	10	pF

#### NOTES

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	14	
	PD = CPD Vcc <sup>2</sup> f+Icc Vcc For load considerations, see Chapter 4 subject listing on page 4-2.	35	pF

### TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

	Metanhard Limit		Gua			
Symbol	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Clock Enable to Clock	2.0	50	65	75	ns
	(Figure 6)	4.5	10	13	15	
	Pr 9r 10 0.8	6.0	9	11	13	
t <sub>su</sub>	Minimum Setup Time, Clock Enable to Clock (Inhibit Count)	2.0	50	65	75	ns
ou	(Figure 6)	4.5	10	13	15	
	80 80 80 00 100	6.0	9	11	13	
th	Minimum Hold Time, Clock to Clock Enable	2.0	50	65	75	ns
	(Figure 6)	4.5	10	13	15	
	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	6.0	9	11	13	
trec	Minimum Recovery Time, Reset to Clock	2.0	100	125	150	ns
	(Figure 7)	4.5	20	25	30	
	62 62 63 63	6.0	17	21	26	
tw	Minimum Pulse Width, Clock Input	2.0	80	100	120	ns
	(Figure 2)	4.5	16	20	24	
	63 60 62 0.0	6.0	14	17	20	
tw	Minimum Pulse Width, Reset Input	2.0	80	100	120	ns
	(Figure 3)	4.5	16	20	24	
	10 6 6 6 6 6 6	6.0	14	17	20	
tw	Minimum Pulse Width, Clock Enable Input	2.0	80	100	120	ns
	(Figure 4)	4.5	16	20	24	
	18 A S 16 16 1	6.0	14	17	20	- Anna
tr, tf	Maximum Input Rise and Fall Times	2.0	1000	1000	1000	ns
	(Figure 1)	4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

### FUNCTION TABLE

Clock	Clock Enable	Reset	Output State*
L	×	L	no change
X	Н	L	no change
X	X	Н	reset counter, Q0=H, Q1-Q9=L, C0=H
	L	L	advance to next state
_	X	L	no change
X		L	no change
Н	_	L	advance to next state

X = Don't care

\*Carry Out = H for Q0, Q1, Q2, Q3, or Q4 = H; Carry Out = L otherwise.

### PIN DESCRIPTIONS

### **INPUTS**

CLOCK (PIN 14) — Counter clock input. While Clock Enable is low, a low-to-high transition on this input advances the counter to its next state.

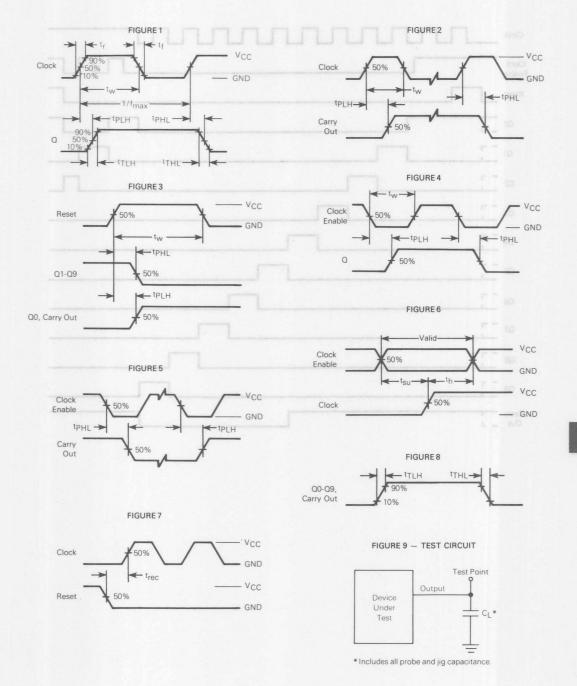
RESET (PIN 15) — Asynchronous counter reset input. A high level at this input initializes the counter and forces Q0 and Carry Out to a high, Q1-Q9 are forced to a low level.

CLOCK ENABLE (PIN 13) — Active-low clock enable input. A low level on this input allows the device to count. A high level on this input inhibits the counting operation. This input may also be used as a negative-edge clock input, using Clock (Pin 14) as an active-high enable pin.

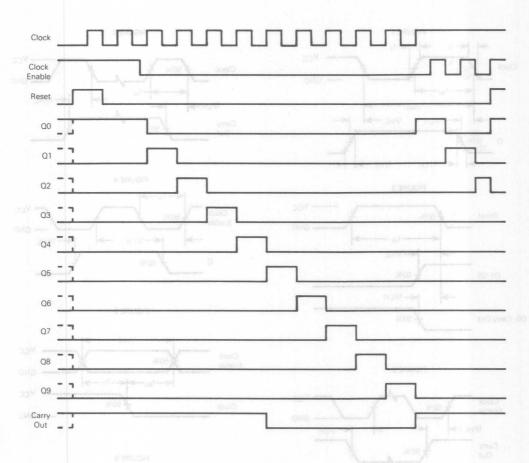
### **OUTPUTS**

Q0-Q9 (PINS 3, 2, 4, 7, 10, 1, 5, 6, 9, 11) — Decoded decade counter outputs. Each of these outputs is high for one clock period only.

CARRY OUT (PIN 12) — Cascading output pin. This output is used either as a cascading output or a symmetrical divide-by-ten output. This output goes low when a count of five is reached and high when the counter advances to zero or when reset. When the counters are cascaded this output provides a rising-edge signal for the clock input of the next counter stage.



TIMING DIAGRAM



### TYPICAL APPLICATIONS

FIGURE 10 - ÷2 THROUGH ÷ 10 CIRCUIT

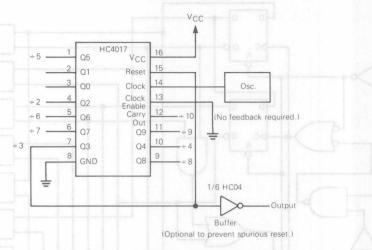


Figure 10 shows a divide by 2 through 10 circuit using one HC4017. Please note that since Reset is asynchronous, the output pulse widths are narrow.

### FIGURE 11 - COUNTER EXPANSION

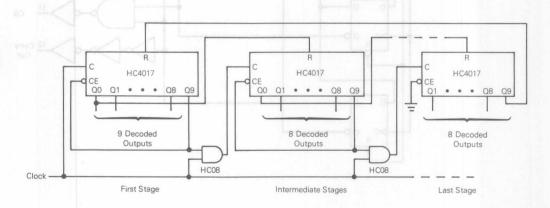


Figure 11 shows a technique for cascading the counters to extend the number of decoded output states. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

# 14-Stage Binary Ripple Counter High-Performance Silicon-Gate CMOS

The MC54/74HC4020 is identical in pinout to the standard CMOS MC14020B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 14 master-slave flip-flops with 12 stages brought out to pins. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4020 for some designs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates

# MC54/74HC4020



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

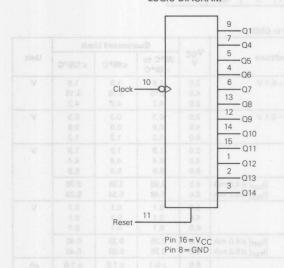
### ORDERING INFORMATION

MC74HCXXXXN MC54HCXXXXJ MC74HCXXXXD

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM



### PIN ASSIGNMENT

FIIA	ASSI	214IAICIA I	
Q12 C	1 •	16 VCC	
Q13 C	2	15 1011	
Q14 <b>L</b>	3	14 010	
Q6 <b>[</b>	4	13 <b>1</b> Q8	
Q5 <b>C</b>	5	12 09	
Q7 <b>C</b>	6	11 Rese	et
Q4 <b>L</b>	7	10 Cloc	k
GND	8	9 101	

### FUNCTION TABLE

Clock	Reset	Output State
	L	No Change
_	L	Advance to next state
X	less-Hi-oro	All Outputs are low

### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\text{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced	to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	CC = 2.0 V CC = 4.5 V CC = 6.0 V	0 0 0	1000 500 400	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	8 9 440		40		Guaranteed Limit			
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  I <sub>out</sub>   ≤20 μA		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V  l <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	011	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	one Advance	Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	± 1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$		6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

			W	Guaranteed Limit			
Symbol	Parameter 1.49/18/19/19/19/19/19/19/19/19/19/19/19/19/19/		V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
fmax	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	pall to are beloggs to	2.0 4.5 6.0	5.0 25 29	4.0 20 24	3.4 17 20	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to Q1* (Figures 1 and 4)		2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
<sup>t</sup> PHL	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	· urunuan	2.0 4.5 6.0	240 48 41	300 60 51	360 72 61	ns
tPLH, tPHL	Maximum Propagation Delay, $Q_N$ to $Q_{N+1}$ (Figures 3 and 4)	- GND	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tTLH,	Maximum Output Transition Time, Any Output (Figures 1 and 4)		2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance			10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

\*For T<sub>A</sub> = 25°C and C<sub>L</sub> = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

 $V_{CC} = 2.0 \text{ V}: \text{ tp} = [205 + 107.5(N - 1)] \text{ ns}$   $V_{CC} = 4.5 \text{ V}: \text{ tp} = [41 + 21.5(N - 1)] \text{ ns}$   $V_{CC} = 6.0 \text{ V}: \text{ tp} = [35 + 18.3(N - 1)] \text{ ns}$ 

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+I <sub>CC</sub> VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	30 HJ97 HH-	pF

### TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

			Gua			
1	Parameter MARDAIG DIDGU GEGMA	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
trec	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
tw	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
tw	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

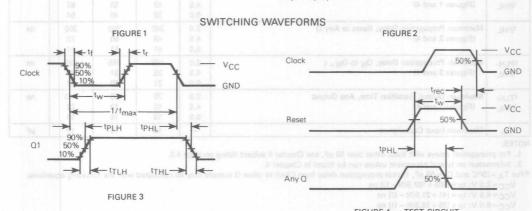
### **INPUTS**

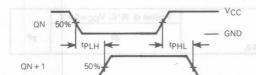
CLOCK (PIN 10) - Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the

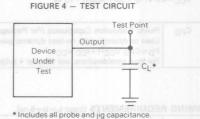
RESET (PIN 11) - Active-high reset. A high level applied

to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

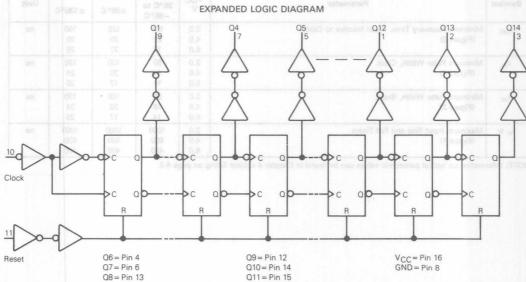
Q1, Q4-Q14 (PINS 9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3) -Active-high outputs. Each QN output divides the Clock input frequency by 2N.



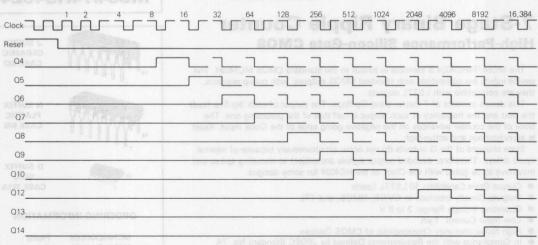




EXPANDED LOGIC DIAGRAM





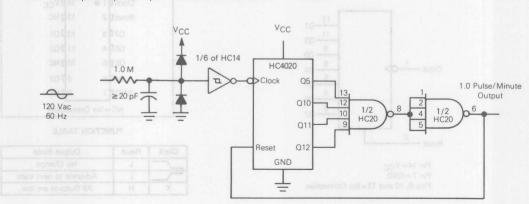


### APPLICATIONS INFORMATION

### TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the input of the MC54/74HC14, Schmitt-trigger inverter. The HC14 squares-up the input waveform and feeds the

HC4020. Selecting outputs Q5, Q10, Q11, and Q12 causes a reset every 3600 clocks. The HC20 decodes the counter outputs, produces a single (narrow) output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



# 7-Stage Binary Ripple Counter High-Performance Silicon-Gate CMOS

The MC54/74HC4024 is identical in pinout to the standard CMOS MC14024. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTI outputs.

This device consists of 7 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4024 for some designs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 206 FETs or 51.5 Equivalent Gates

# MC54/74HC4024



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



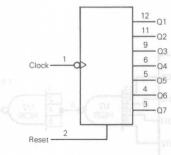
D SUFFIX SOIC CASE 751A

### ORDERING INFORMATION

MC74HCXXXXN MC54HCXXXXJ MC74HCXXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### Needug 0.1 al voneupest jugrue prof LOGIC DIAGRAM (15.00)



Pin 14 = V<sub>CC</sub> Pin 7 = GND

Pins 8, 10 and 13 = No Connection

### PIN ASSIGNMENT

Clock	1 •	14	Vcc
Reset [	2	13	-
Q7 <b>C</b>	3	12	Q1
Q6 <b>[</b>	4	11	Q2
Q5 <b>c</b>	5	10	NC
Q4 C	6	9	Q3
GND	7	8	NC

# NC = No Connection FUNCTION TABLE

Clock	Reset	Output State
	L	No Change
_	L	Advance to next state
X	Н	All Outputs are low

### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	ndino Dissipo ut	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

### DC FLECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter of the parame	Test Conditions	V <sub>CC</sub>	Guaranteed Limit			
				25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
2/1	1000 1000 1000 1000 1000	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	12 117
	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V MI STO
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	± 1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

	Value Uses contains			Gua	agmile		
Symbol	due to high static voltage		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency	50% Duty Cycle)	2.0	5.4	4.4	3.6	MHz
ster more	(Figures 1 and 4)		4.5	27	22	18	-
onubequi	volumes to this high	Acres BC -	6.0	32	26	21	
tPLH,	Maximum Propagation Delay	, Clock to Q1*	2.0	210	265	315	ns
tPHL	(Figures 1 and 4)		4.5	42	53	63	CLUP
DOME!	onW compa GND ≤ (Vip. or Vip.	6.0	36	45	54	.09	
tPHL	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	, Reset to Any Q	2.0	210	265	315	ns
sacint I de			4.5	42	53	63	Teto
			6.0	36	45	54	JT.
tPLH,	Maximum Propagation Delay	, QN to QN+1	2.0	125	155	190	ns
tPHL	(Figures 3 and 4)		4.5	25	31	38	
			6.0	21	26	32	urnheah
tTLH,	Maximum Output Transition	Time, Any Output	2.0	75	95	110	ns
tTHL	(Figures 1 and 4)		4.5	15	19	22	Derating
			6.0	13	16	19	
Cin	Maximum Input Capacitance		0.000 pt. 70 ta	10	10	10	pF

#### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

\*For TA = 25°C and CL = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:  $V_{CC} = 2.0 \text{ V}$ : tp =[205 + 100(N - 1)] ns

 $V_{CC} = 4.5 \text{ V: } t_P = [41 + 20(N - 1)] \text{ ns}$ 

 $V_{CC} = 6.0 \text{ V: } t_P = [35 + 17(N - 1)] \text{ ns}$ 

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	II mucini	
	PD = CPD VCC <sup>2</sup> f + ICC VCC	30	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

#### TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

	Simil beomersus				Guaranteed Limit			
Symbol	0°85/2 0°85/2 0°85/4			VCC	25°C to -55°C	≤85°C	≤125°C	Unit
trec	Minimum Recovery Time, Re	set Inactive to Clock	V i.0 - poV to V f.0	2.0	100	125	150	ns
	(Figure 2)			4.5	20	25	30	
	4.2 4.2 4.2			6.0	17	21	26	- 3
tw	Minimum Pulse Width, Clock	0.0	V 110-00V so V 110	2.0	80	100	120	ns
	(Figure 1)			4.5	16	20	24	
	1.2 1.2 1.2	0.9		6.0	14	17	20	
tw	Minimum Pulse Width, Reset	2.0	31V 90 54L	2.0	80	100	120	ns
	(Figure 2)			4.5	16	20	24	
	8.8 8.8	0.8		6.0	14	17	20	
tr, tf	Maximum Input Rise and Fall	Times	H or Air Lead's	2.0	1000	1000	1000	ns
	(Figure 1)			4.5	500	500	500	
	100 100 100			6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

# PIN DESCRIPTIONS

INPUTS

OUTPUTS

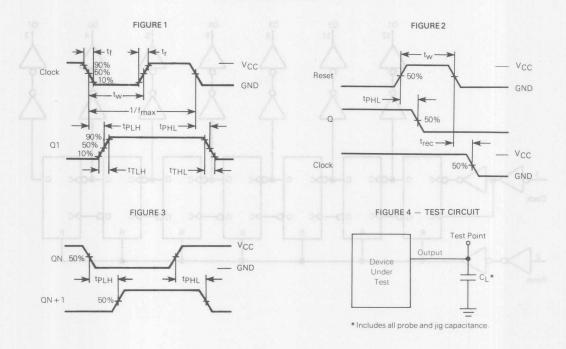
CLOCK (PIN 1) — Negative-edge triggering clock input. A high-to-low transition of this input advances the state of the high-to-low transition of this input advances the state of the Each QN output divides the Clock input frequency by 2<sup>N</sup>.

Q1-Q7 (PINS 12, 11, 9, 6, 5, 4, 3) - Active-high outputs.

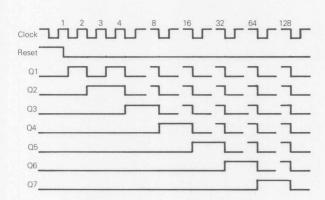
RESET (PIN 2) - Active-high asynchronous reset. A high level applied to this input resets the counter to its zero state, thus forcing all Q outputs low.

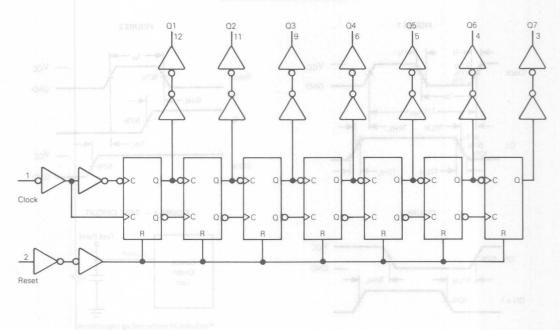
# MC54/74HC4024

# SWITCHING WAVEFORMS



# TIMING DIAGRAM





TIMING BIAGRAM

# 12-Stage Binary Ripple Counter High-Performance Silicon-Gate CMOS

The MC54/74HC4040 is identical in pinout to the standard CMOS MC14040. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 12 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4040 for some designs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates

# MC54/74HC4040



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



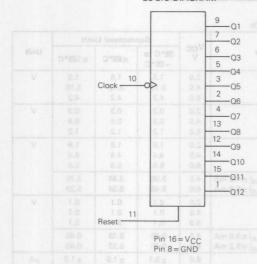
D SUFFIX SOIC CASE 751

# **ORDERING INFORMATION**

MC74HCXXXXN MC54HCXXXXJ MC74HCXXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# LOGIC DIAGRAM



# PIN ASSIGNMENT

PIN	ASSIGN	INIENT
Q12	1 •	16 V <sub>CC</sub>
Q6 C	2	15 011
Q5 <b>C</b>	3	14 010
Q7 <b>[</b>	4	13 Q8
Q4 C	5	12 <b>Q</b> 9
Q3 <b>C</b>	6	11 Reset
Q2 <b>D</b>	7	10 Clock
GND [	8	9 <b>1</b> Q1
		ARTHUR VI

# **FUNCTION TABLE**

Clock	Reset	Output State
	L	No Change
7	no Lucia	Advance to next state
X	Н	All Outputs are low

# MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	٧
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	٧
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

 $^\dagger \mbox{Derating} - \mbox{Plastic DIP:} - 10 \mbox{ mW/°C from 65° to 125°C}$ 

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types			+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1) V	CC = 2.0 V CC = 4.5 V CC = 6.0 V	0 0 0	1000 500 400	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Parameter	2000	Vcc	Gua			
Symbol		Test Conditions		25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	Vin=VIH or VIL  I <sub>out</sub>   ≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	Clock Roses Output	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=Vcc or GND	6.0	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

			Vcc	Gua			
Symbol	Parameter			25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)		2.0 4.5 6.0	5.0 25 29	4.0 20 24	3.4 17 20	MHz
tPLH, tPHL	Maximum Propagation Delay, Clock to Q1* (Figures 1 and 4)	009	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
<sup>t</sup> PHL	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)		2.0 4.5 6.0	240 48 41	300 60 51	360 72 61	ns
tPLH, tPHL	Maximum Propagation Delay, QN to QN+1 (Figures 3 and 4)		2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)		2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance		-	10	10	10	pF

#### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

\*For T<sub>A</sub> = 25°C and C<sub>L</sub> = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations: : V<sub>CC</sub> = 2.0 V: tp = [205 + 107.5(N - 1)] ns

 $V_{CC} = 4.5 \text{ V: } tp = [41 + 21.5(N - 1)] \text{ ns}$ 

 $V_{CC} = 6.0 \text{ V: } tp = [35 + 18.3(N - 1)] \text{ ns}$ 

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	35	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

# TIMING REQUIREMENTS (Input tr=tf=6 ns)

	Parameter MASBAIG CHOLL GROWASKS		Gua			
Symbol			25°C to -55°C	≤85°C	≤125°C	Unit
<sup>t</sup> rec	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

## PIN DESCRIPTIONS

# **INPUTS**

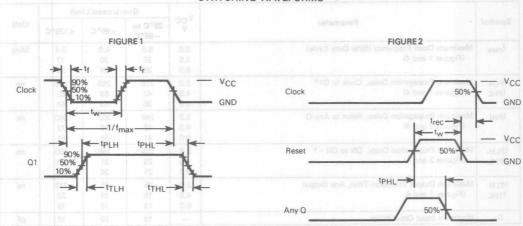
**OUTPUTS** 

CLOCK (PIN 10) - Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the

Q1 THRU Q12 (PINS 9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1) - Active-high outputs. Each QN output divides the Clock input frequency by 2N.

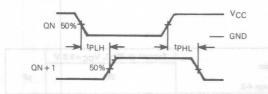
RESET (PIN 11) - Active-high reset. A high level applied to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.



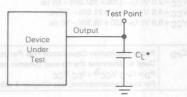


# FIGURE 3

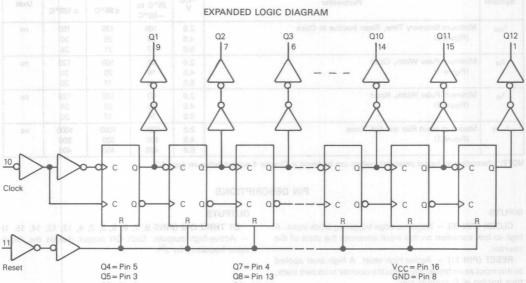
FIGURE 4 - TEST CIRCUIT



Q6= Pin 2



\* Includes all probe and jig capacitance.

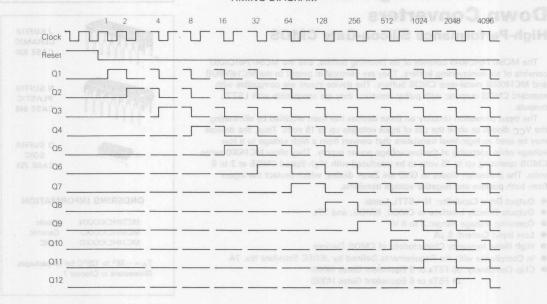


5

Q9 = Pin 12

# MC54/74HC4040

# TIMING DIAGRAM

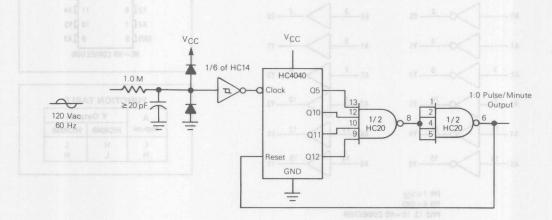


# APPLICATIONS INFORMATION

# TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the input of the HC14, Schmitt-trigger inverter. The HC14 squares-up the input waveform and feeds the HC4040.

Selecting outputs Q5, Q10, Q11, and Q12 causes a reset every 3600 clocks. The HC20 decodes the counter outputs, produces a single (narrow) output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



# Hex Buffers/Logic-Level Down Converters

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC4049 consists of six inverting buffers, and the MC54/74HC4050 consists of six noninverting buffers. They are identical in pinout to the MC14049UB and MC14050B metal-gate CMOS buffers. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The input protection circuitry on these devices has been modified by eliminating the V<sub>CC</sub> diodes to allow the use of input voltages up to 15 volts. Thus, the devices may be used as logic-level translators that convert from a high voltage to a low voltage while operating at the low-voltage power supply. They allow MC14000-series CMOS operating up to 15 volts to be interfaced with High-Speed CMOS at 2 to 6 volts. The protection diodes to GND are Zener diodes, which protect the inputs from both positive and negative voltage transients.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 5 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 36 FETs or 9 Equivalent Gates (4049)
   24 FETs or 6 Equivalent Gates (4050)

# MC54/74HC4049 MC54/74HC4050



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

# ORDERING INFORMATION

MC74HCXXXXN	ı
MC54HCXXXXJ	
MC74HCXXXXD	)

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAMS

	HC4049 (INVERTING BUF	FER) ORGENSEN		4050 FING BUFFER)
A0 —	->	Y0	A0 3	Y0
A1 —	<b>-</b> >	Y1	A15	<u>4</u> Y1
A2 —	7	6Y2	A27	<u>6</u> Y2
A3 -	9	10 Y3	A3 9	<u>10</u> γ3
A4 —	11	12Y4	A4 11	<u>12</u> y4
A5 —	14	15 Y5	A5 14	Y5
		PIN 1 = Vcc		

PINS 13, 16 = NO CONNECTION

PIN 8 = GND

# PIN ASSIGNMENT

vcc d	1.0	16	] NC
	l in	A PERCY A	Section 1
YO [	2	15	] Y5
AO [	3	14	] A5
Y1 [	4	13	NC
A1 [	5	12	] Y4
Y2 [	6	11	] A4
A2 [	7	10	] Y3
GND [	8	9	] A3
NC	= NO CO	NNECTIO	IN

# FUNCTION TABLE

Α	Y Outputs			
Inputs	HC4049	HC4050		
L	Н	L		
Н	L	Н		

# MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to +18	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	os °C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the GND pin, only. Extra precuations must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges  $\text{GND}\!\leq\!\text{V}_{\text{IN}}\!\leq\!\text{15}\ \text{V}$  and  $\text{GND}\!\leq\!\text{V}_{\text{OUt}}\!\leq\!\text{V}_{\text{CC}}$  are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>).

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	Supply Voltage (Referenced to GND)		6.0	V
Vin	DC Input Voltage (Referenced to GND)	100 100	0	V <sub>CC</sub> to	٧
Vout	DC Output Voltage (Referenced to GND)		0	Vcc	٧
TA	Operating Temperature, All Package Type	es Y III STEE	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Guaranteed Limit			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Uni
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$		3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND V <sub>in</sub> = 15 V	6.0 6.0	±0.1 0.5	± 1.0 5.0	± 1.0 5.0	μΔ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = 15 V or GND I <sub>out</sub> = 0 μA	6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

# AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	stue Unit This device contains o			Vcc	Guaranteed Limit			lodmy
	protest the inputs against	Parameter DATE of 0.0-			25°C to	Voltage (II.	DC Supply	Unit
	dissipation citate rigin of sub-			1 days	-55°C	≤85°C	≤125°C	- n'V
tPLH,	Maximum Propagation Dela	y, Input A to Output Y		2.0	85	105	130	ns
tPHL .	(Figures 1 and 2)			4.5	17	21	26	150
mumban	voltage frighter than the			6.0	14	18	22	
tTLH,	Maximum Output Transition	Time, Any Output	-	2.0	75	95	110	ns
THL	(Figures 1 and 2)			4.5	15	19	22	0.00
one V a	Die rangea GND≤Vijg≤		1910 sir	6.0	13	16	19	gq.
Cin	Maximum Input Capacitance	9	regaring	A 710/2	10	10	10	pF

#### NOTEC

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	enditanu
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2.	or *00" most 0" Win 07 - 910 arraig on *00" most 0" Win 0.27 (910 arraig)	pF

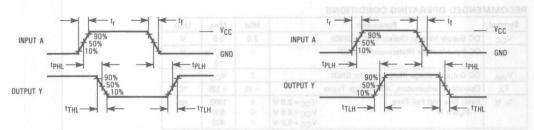
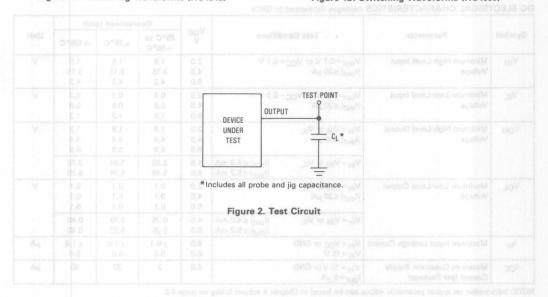


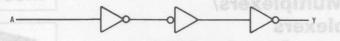
Figure 1a. Switching Waveforms (HC4049)

Figure 1b. Switching Waveforms (HC4050)



## LOGIC DETAIL

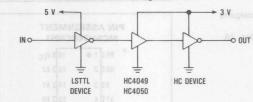
HC4049 (1/6 of the Device)



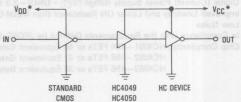
# HC4050 (1/6 of the Device)

# TYPICAL APPLICATIONS

LSTTL to Low-Voltage HSCMOS



High-Voltage CMOS to HSCMOS



NOTE: To determine the noise immunity for the LSTTL to lowvoltage configuration, use Eq. 1 and Eq. 2:

For the supply levels shown: 2.4-3 (75%) = 2.4-2.25 = 0.15 V 0.4-3 (15%) = 0.4-0.45 = 0.05 V

Therefore, worst case noise immunity is 50 mV.
For supply levels greater than 4.5 volts use the 74HCT04 for direct interface to TTL outputs.

\*Table 1. Supply Examples

VDD	Vcc
15 V	2 V
12 V	5 V
12 V	3 V

# Advance Information

# **Analog Multiplexers/ Demultiplexers**

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC4051, MC54/74HC4052, and MC54/74HC4053 utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from VCC to VEE).

The HC4051, HC4052, and HC4053 are identical in pinout to the metal-gate MC14051B, MC14052B, and MC14053B. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is high, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance (Ron) is more linear over input voltage than Ron of metal-gate CMOS analog switches.

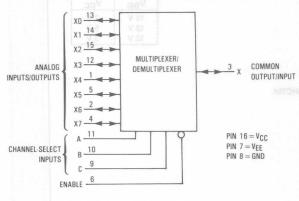
For multiplexers/demultiplexers with channel select latches, see HC4351, HC4352, and HC4353.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (V<sub>CC</sub> V<sub>EE</sub>) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range (VCC GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance than Metal-Gate Counterparts

- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: HC4051 184 FETs or 46 Equivalent Gates

HC4052-168 FETs or 42 Equivalent Gates HC4053-156 FETs or 39 Equivalent Gates

# LOGIC DIAGRAM MC54/74HC4051 Single-Pole, 8-Position Plus Common Off



# MC54/74HC4051 MC54/74HC4052 MC54/74HC4053



J SUFFIX CERAMIC **CASE 620** 



N SUFFIX PLASTIC **CASE 648** 



DW SUFFIX SOIC CASE 751G

#### ORDERING INFORMATION

MC74HCXXXXN MC54HCXXXXI MC74HCXXXXDW Plastic Ceramic SOIC

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# PIN ASSIGNMENT MC54/74HC4051

X4 C	1 •	160 V <sub>C</sub>
X60	2	15 X2
ΧC	3	140 X1
X7 🛚	4	13 X0
X5 C	5	12 X3
ENABLE C	6	11 D A
VEE	7	10 B
GND	8	9 D C

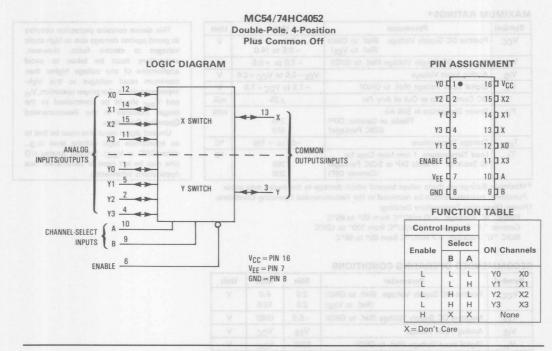
# FUNCTION TABLE MC54/74HC4051

Cont	rol Ir	puts		Theory		
Enable	Select			ON Channels		
Enable	С	В	Α	101 (111		
L	L	L	L	X0		
L	L	L	Н	X1		
L	L	Н	L	X2		
L	L	Н	Н	X3		
L	Н	L	L	X4		
L	Н	L	Н	X5		
L	Н	Н	L	X6		
L	Н	Н	Н	X7		
H	X	X	X	None		

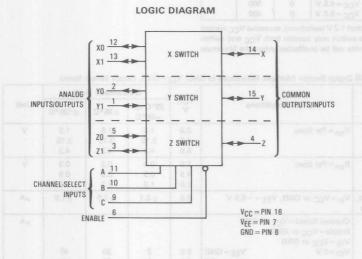
X = don't care

This document contains information on a new product. Specifications and information herein are subject to change without notice

# MC54/74HC4051•MC54/74HC4052•MC54/74HC4053







NOTE: This device allows independent control of each switch. Channel-Select Input
A controls the X Switch, Input B controls the Y Switch, and Input C controls
the Z Switch.

# PIN ASSIGNMENT

Y1 C	1 .	16	b vcc
Y0 C	2	15	1 Y
Z1 C	3	14	x
E Z C	4	13	1 X1
Z0 C	5	12	1 XO
ENABLE C	6	11	J A
V <sub>EE</sub> C	7	10	В
GND C	8	9	рс

# **FUNCTION TABLE**

Cont	rol li	nputs	BIEW!			
- 100	Select C B A		ON	ON Ch		
Enable			ON Channel			
L.	L	L	L	ZO	YO	XO
L	L	L	Н	ZO	YO	X1
L	L	Н	L	Z0	Y1	X0
L	L	Н	Н	Z0	Y1	X1
L	Н	L	L	Z1	Y0	X0
Long	H	ollo	H	Z1	YO	X1
L	Н	Н	L	Z1	Y1	X0
L	Н	Н	Н	Z1	Y1	X1
Н	X	X	X		None	

X = Don't Care

\_

#### **MAXIMUM RATINGS\***

Symbol	Parameter		Value Value	Unit
VCC	11,	to GND) to V <sub>EE</sub> )	-0.5 to +7.0 -0.5 to 14.0	٧
VEE	Negative DC Supply Voltage (Ref. to GND)		-7.0  to  +0.5	V
VIS	Analog Input Voltage		V <sub>EE</sub> - 0.5 to V <sub>CC</sub> + 0.5	V
Vin	Digital Input Voltage (Ref. to GND)		-1.5 to V <sub>CC</sub> +1.5	V
Dist.	DC Current Into or Out of Any Pin		± 25	mA
PD	Power Dissipation in Still Air Plastic or Cera SOIC	mic DIP† Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature		-65 to +150	°C
TLXE	Lead Temperature, 1 mm from Cas 10 Seconds (Plastic DIP or SOIC (Cera		260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Power Dissipation Temperature Derating:

Plastic "N" Package: -10 mW/°C from 65° to 85°C Ceramic "J" Package: -10 mW/°C from 100° to 125°C SOIC "D" Package: -7 mW/°C from 65° to 85°C

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	Positive DC Supply Voltage	(Ref. to GND) (Ref. to VFF)	2.0	6.0 12.0	V
VEE	Negative DC Supply Voltage		-6.0	GND	V
VIS	Analog Input Voltage	VEE	Vcc	٧	
Vin	Digital Input Voltage (Ref. to	GND)	GND	Vcc	V
V <sub>IO</sub> *	Static or Dynamic Voltage A	cross Switch	30=0H	1.2	V
TA	Operating Temperature, All I	Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time, (Channel Select or Enable Inputs)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0	1000 500 400	ns

<sup>\*</sup>For voltage drops across the switch greater than 1.2 V (switch on), excessive  $V_{CC}$  current may be drawn; i.e., the current out of the switch may contain both  $V_{CC}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

# DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V<sub>EF</sub> = GND, Except Where Noted

	विद्या ३ विद्या	намина 1		Gua			
Symbol	Parameter	Test Conditions	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	R <sub>on</sub> = Per Spec	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	R <sub>on</sub> =Per Spec		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
lin	Maximum Input Leakage Current, Channel-Select or Enable Inputs	V <sub>in</sub> =V <sub>CC</sub> or GND, V <sub>EE</sub> = -6.0 V	6.0	±0.1	± 1.0	± 1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)		6.0 6.0	2 8	20 80	40 160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vinand Vout should be constrained to the ranges indicated in the Recommended Operating Conditions.

Unused digital input pins must be tied to an appropriate logic voltage level (e.g.

This device contains protection circuitry to guard against damage due to high static

Unused digital input pins must be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused Analog I/O pins may be left open or terminated. See Applications Information.

# MC54/74HC4051•MC54/74HC4052•MC54/74HC4053

DC ELECTRICAL CHARACTERISTICS Analog Section

	- Waterial				Gua	aranteed L	imit	
Symbol	Parameter	Test Conditions VCC	Vcc	VEE	25°C to -55°C	≤85°C	≤125°C	Uni
Ron	Maximum "ON" Resistance	$V_{\text{in}} = V_{\text{IL}} \text{ or } V_{\text{IH}}$ $V_{\text{IS}} = V_{\text{CC}} \text{ to } V_{\text{EE}}$ $I_{\text{S}} \leq 2.0 \text{ mA (Figures 1, 2)}$	4.5 4.5 6.0	0.0 -4.5 -6.0	190 120 100	240 150 125	280 170 140	Ω
	4.50 -4.50 80 95 120 -40.05 4.00 80 95 120	V <sub>in</sub> =V <sub>IL</sub> or V <sub>IH</sub> V <sub>IS</sub> =V <sub>CC</sub> or V <sub>EE</sub> (Endpoints) I <sub>S</sub> ≤2.0 mA (Figures 1, 2)	4.5 4.5 6.0	0.0 -4.5 -6.0	150 100 80	190 125 100	230 140 115	
ΔR <sub>on</sub>	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IL}$ or $V_{IH}$ $V_{IS} = 1/2$ ( $V_{CC} - V_{EE}$ ) $I_S \le 2.0$ mA	4.5 4.5 6.0	0.0 -4.5 -6.0	30 12 10	35 15 12	40 18 14	Ω
loff	Maximum Off-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IO</sub> = V <sub>CC</sub> - V <sub>EE</sub> Switch Off (Figure 3)	6.0	-6.0	0.1	0.5	1.0	μΑ
	Maximum Off-Channel Leakage Current, Common Channel HC4051	V <sub>in</sub> =V <sub>IL</sub> or V <sub>IH</sub> V <sub>IO</sub> =V <sub>CC</sub> -V <sub>EE</sub> Switch Off (Figure 4)	6.0	-6.0	0.2	2.0	4.0	
	HC4052 HC4053	GAS=si: GAS=si:	6.0	-6.0 -6.0	0.1	1.0	2.0	
lon	Maximum On-Channel Leakage Current, Channel to Channel HC4051	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> Switch to Switch = V <sub>CC</sub> - V <sub>EE</sub> (Figure 5)	6.0	-6.0	0.2	2.0	4.0	μΑ
	HC4052 HC4053	r Sine Wavs	6.0	-6.0 -6.0	0.1	1.0	2.0	

AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

			Vcc	Gua	aranteed Li	mit	
Symbol	08-4 08-5 08-5 Parameter	raidilletei		25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Channel-Sel (Figure 9)	lect to Analog Output	2.0 4.5 6.0	370 74 63	465 93 79	550 110 94	ns
tPLH, tPHL	Maximum Propagation Delay, Analog Inpu (Figure 10)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns	
tPLZ, tPHZ				290 58 49	364 73 62	430 86 73	ns
tPZL, tPZH				345 69 59	435 87 74	515 103 87	ns
Cin	Maximum Input Capacitance, Channel-Sel	lect or Enable Inputs	-	10	10	10	pF
CI/O	Maximum Capacitance Analog I/O	All Switches Off	-	35	35	35	pF
	Common O/I: HC4051 HC4052 HC4053		-	130 80 50	130 80 50	130 80 50	
	Feedthrough		_	1.0	1.0	1.0	

# NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
   Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) (Figure 13)	Typical @ 25°C, V <sub>CC</sub> =5.0 V, V <sub>EE</sub> =0 V	
	Used to determine the no-load dynamic power consumption:		
	PD = CPD VCC2f+ICC VCC	45 (HC4051)	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	80 (HC4052)	
		45 (HC4053)	

# ADDITIONAL APPLICATION CHARACTERISTICS (GND=0.0 V)

	Limit					W		Limit*	
Symbol	3189 s	Para	meter	say s	Test Condition	VCC	VEE	25°C 54/74HC	Unit
BW	Maximum F Minimum F (Figure 6	requency			fin = 1 MHz Sine Wave Adjust fin Voltage to Obtain 0 dBm at Vos Increase fin Frequency Until dB Meter	2.25	-2.25	51 52 53 80 95 120	MHz
	OSS OSS	190			Reads - 3 dB R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	4.50 6.00	-4.50 -6.00	80 95 120 80 95 120	
_	Off-Channe	el Feedth	rough Isola	ation	f <sub>in</sub> ≡ Sine Wave			411.01	dB
	(Figure 7	ar er	30 12 10		Adjust $f_{in}$ Voltage to Obtain 0 dBm at VIS $f_{in}$ = 10 kHz, $R_L$ = 600 $\Omega$ , $C_L$ = 50 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	-50 -50 -50	появ
	0.1				$f_{in} = 1.0 \text{ MHz}, R_L = 50 \Omega, C_L = 10 \text{ pF}$	2.25 4.50 6.00	-2.25 -4.50 -6.00	-40 -40 -40	that
-	to Commo (Figure 8	n O/I	Channel S	Select Input	$V_{in} \le 1$ MHz Square Wave $(t_r = t_f = 6 \text{ ns})$ Adjust R <sub>L</sub> at Setup so that I <sub>S</sub> = 0 A Enable = GND R <sub>L</sub> = 600 $\Omega$ , C <sub>L</sub> = 50 pF	2.25 4.50	-2.25 -4.50	25 105	mVp
	8,8				$R_L = 10 \text{ k}\Omega$ , $C_L = 10 \text{ pF}$	6.00 2.25 4.50 6.00	-6.00 -2.25 -4.50 -6.00	135 35 145 190	,ngi
- 1	Crosstalk E (Figure 1 (Test do	(2)	Any Two S		$\begin{split} f_{In} &= \text{Sine Wave} \\ \text{Adjust } f_{In} &= \text{Voltage to Obtain 0 dBm at V}_{IS} \\ f_{In} &= 10 \text{ kHz}, \text{ R}_L = 600 \ \Omega, \text{ C}_L = 50 \text{ pF} \end{split}$	2.25 4.50 6.00	-2.25 -4.50 -6.00	- 50 - 50 - 50	dB
Unit	in ≤ 138°C	mil beet		25'0	$f_{in} = 1$ MHz, $R_L = 50 \Omega$ , $C_L = 10 pF$	2.25 4.50 6.00	-2.25 -4.50 -6.00	-60 -60 -60	ddmy8
THD	Total Harm (Figure 1				$f_{in}$ = 1 kHz, $R_L$ = 10 k $\Omega$ , $C_L$ = 50 pF THD = THDMeasured - THDSource $V_{IS}$ = 4.0 Vpp sine wave $V_{IS}$ = 8.0 Vpp sine wave	2.25 4.50	-2.25 -4.50	0.10 0.08	%
	108				V <sub>IS</sub> = 11.0 V <sub>PP</sub> sine wave	6.00	-6.00	0.05	HJGI

5

MOTOROLA HIGH-SPEED CMOS LOGIC DATA

# MC54/74HC4051•MC54/74HC4052•MC54/74HC4053

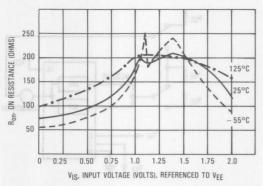


Figure 1a. Typical On Resistance, V<sub>CC</sub> - V<sub>EE</sub> = 2.0 V

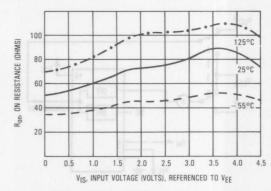


Figure 1b. Typical On Resistance, VCC - VEE = 4.5 V

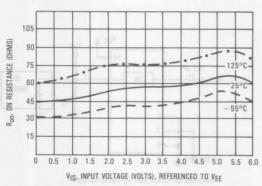


Figure 1c. Typical On Resistance, VCC - VEE = 6.0 V

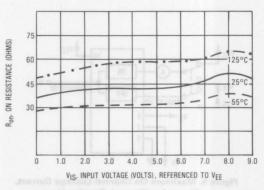


Figure 1d. Typical On Resistance, VCC - VEE = 9.0 V

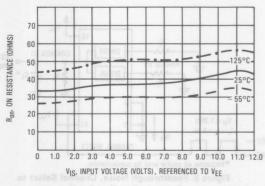


Figure 1e. Typical On Resistance, VCC - VEE = 12.0 V

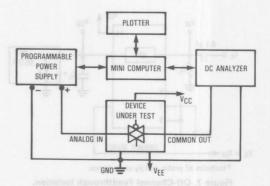


Figure 2. On Resistance Test Set-Up

# MC54/74HC4051 • MC54/74HC4052 • MC54/74HC4053

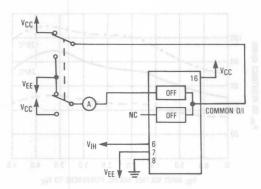


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

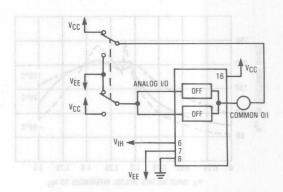


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

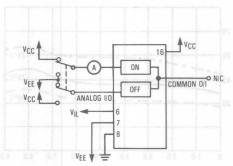
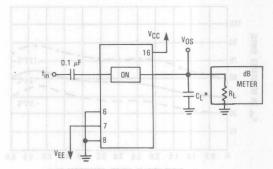


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



\*Includes all probe and jig capacitance.

Figure 6. Maximum On-Channel Bandwidth, Test Set-Up

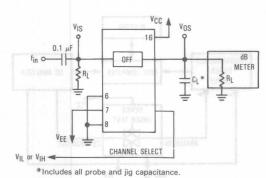


Figure 7. Off-Channel Feedthrough Isolation,

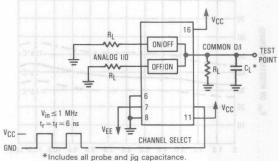


Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

# MC54/74HC4051•MC54/74HC4052•MC54/74HC4053

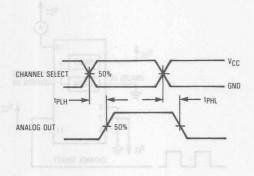
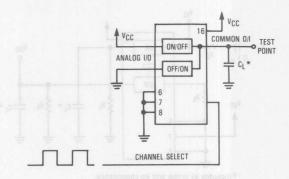


Figure 9a. Propagation Delays, Channel Select to Analog Out



\*Includes all probe and jig capacitance.

Figure 9b. Propagation Delay, Test Set-Up Channel Select to Analog Out

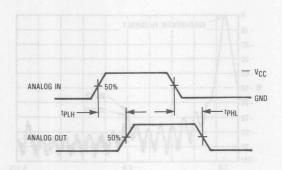
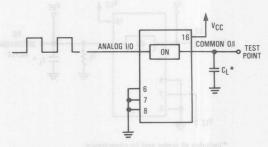


Figure 10a. Propagation Delays, Analog In to Analog Out



\*Includes all probe and jig capacitance.

Figure 10b. Propagation Delay, Test Set-Up Analog In to Analog Out

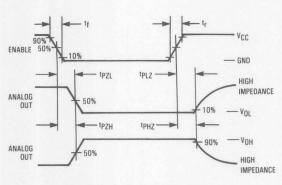


Figure 11a. Propagation Delays, Enable to Analog Out

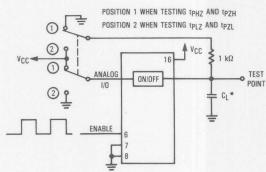
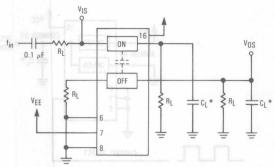


Figure 11b. Propagation Delay, Test Set-Up Enable to Analog Out

# MC54/74HC4051•MC54/74HC4052•MC54/74HC4053



\*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

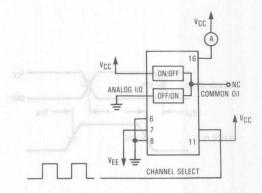
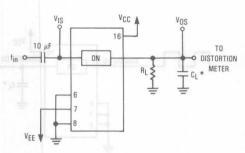


Figure 13. Power Dissipation Capacitance, Test Set-Up



\*Includes all probe and jig capacitance.

Figure 14a. Total Harmonic Distortion, Test Set-Up

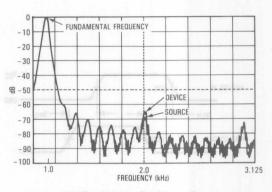


Figure 14b. Plot, Harmonic Distortion

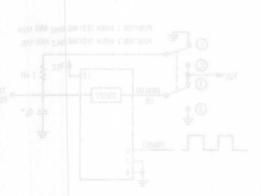
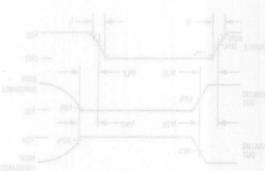


Figure 11h. Propagation Ooley, Test Se



ours 11s. Propagation Dalays, Eachle to Analog Out

# APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at VCC or GND logic levels. VCC being recognized as a logic high and GND being recognized as a logic low. In this example:

$$V_{CC} = +5 V = logic high$$
  
 $GND = 0 V = logic low$ 

The maximum analog voltage swings are determined by the supply voltages V<sub>CC</sub> and V<sub>EE</sub>. The positive peak analog voltage should not exceed V<sub>CC</sub>. Similarly, the negative peak analog voltage should not go below V<sub>EE</sub>. In this example, the difference between V<sub>CC</sub> and V<sub>EE</sub> is ten volts. Therefore, using the configuration in Figure 15, a maximum analog signal of

ten volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V<sub>CC</sub> or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked-up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

 $\begin{array}{c} V_{CC}-GND=2 \text{ to 6 volts} \\ V_{EE}-GND=0 \text{ to } -6 \text{ volts} \\ V_{CC}-V_{EE}=2 \text{ to } 12 \text{ volts} \\ \text{and } V_{EE} \leq GND \end{array}$ 

When voltage transients above  $V_{CC}$  and/or below  $V_{EE}$  are anticipated on the analog channels, external Germanium or Schottky diodes  $(D_X)$  are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

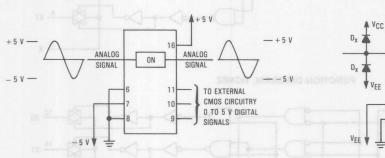


Figure 15. Application Example



ON/OFF

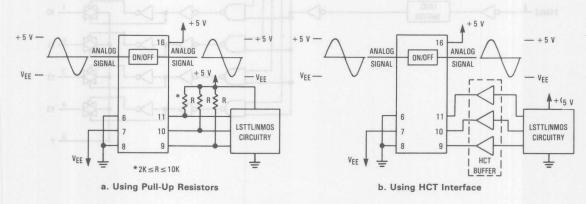
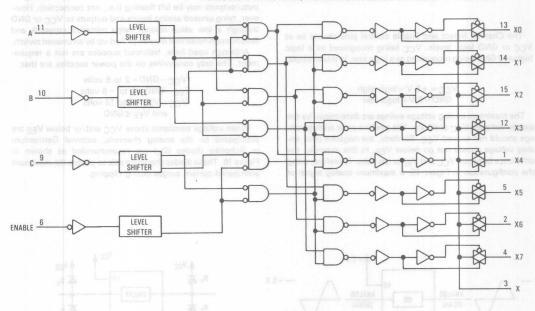
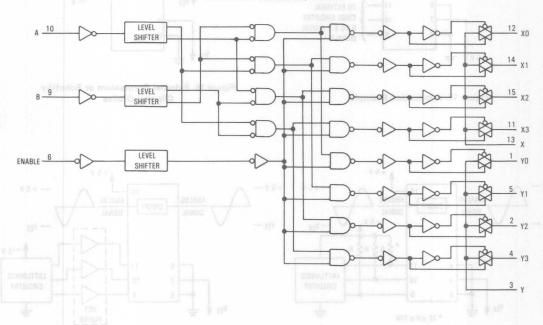


Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

# FUNCTION DIAGRAM, HC4051

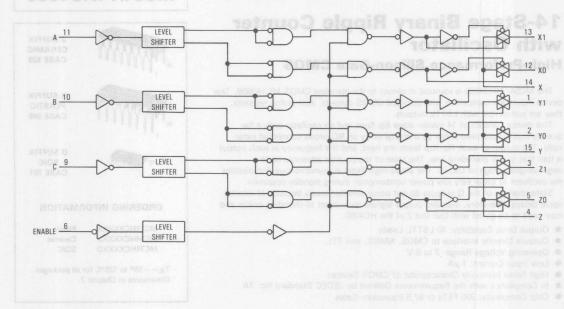


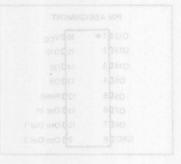
# **FUNCTION DIAGRAM, HC4052**

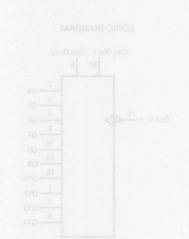


# MC54/74HC4051•MC54/74HC4052•MC54/74HC4053









# 14-Stage Binary Ripple Counter with Oscillator

# **High-Performance Silicon-Gate CMOS**

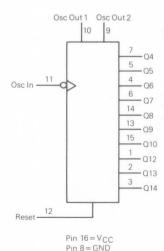
The MC54/74HC4060 is identical in pinout to the standard CMOS MC14060B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 14 master-slave flip-flops and an oscillator with a frequency that is controlled either by a crystal or by an RC circuit connected externally. The output of each flip-flop feeds the next, and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of Osc In. The active-high Reset is asynchronous and disables the oscillator to allow very low power consumption during standby operation.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may need to be gated with Osc Out 2 of the HC4060.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 390 FETs or 97.5 Equivalent Gates

# LOGIC DIAGRAM



# MC54/74HC4060



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751

# ORDERING INFORMATION

MC74HCXXXXN MC54HCXXXXJ MC74HCXXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# PIN ASSIGNMENT

Q12 <b>C</b> 1 •	16 VCC
Q13 C2	150010
Q14 <b>C</b> 3	14 <b>0</b> Q8
Q6 <b>C</b> 4	1309
Q5 <b></b> 5	12 Reset
Q7 <b>C</b> 6	11 Osc In
Q4 <b>C</b> 7	10 Osc Out 1
GND 08	90 Osc Out 2

# FUNCTION TABLE

Osc In Reset		Output State
	L	No Change
_	L	Advance to next state
X	Н	All Outputs are low

Symbol	plant Joseph Parameter	Value	Unit
VCC	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, VCC and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature 1.0 0.3	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	O C A C Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq \mathsf{VCC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter				Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)				6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage	0	Vcc	V		
TA	Operating Temperature, All Pack	Operating Temperature, All Package Types				
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	2.0	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

<sup>\*\*</sup>The oscillator is guaranteed to function at 2.5 V minimum. However, parametrics are tested at 2.0 V by driving Pin 11 with an external clock source.

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	125 186 190	0.5	NO at 9	Guaranteed Limit			
Symbol	Parameter	Test Conditions V	V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V or } V_{\text{CC}} = 0.1 \text{ V}$ $ I_{\text{out}}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Vон	Minimum High-Level Output Voltage (Q4-Q10, Q12-Q14)	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	- 33V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	Yee
VOL	Maximum Low-Level Output Voltage (Q4-Q10, Q12-Q14)	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
99	25	$V_{\text{in}} = V_{\text{IH}}$ or $V_{\text{IL}}$ $ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	

E

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) (Continued)

	anidaneo sonesh eidT	nt/ outsid		Guaranteed Limit			
Symbol	date by the Parameter bostov blaste right of sub	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
Voн	Minimum High-Level Output - Voltage (Osc Out 1, Osc Out 2)	$V_{\text{in}} = V_{\text{CC}} \text{ or GND}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	<sub>tuo</sub> V
		$V_{in} = V_{CC}$ or GND $ I_{out}  \le 1.0 \text{ m}$ $ I_{out}  \le 1.3 \text{ m}$		3.98 5.48	3.84 5.34	3.70 5.20	700 <sup>1</sup>
V <sub>OL</sub>	Maximum Low-Level Output Voltage (Osc Out 1, Osc Out 2)	$V_{in} = V_{CC}$ or GND $ I_{out}  \le 20 \ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	OV.
	ling, either GND or Vo ouques must be left ope	$V_{in} = V_{CC}$ or GND $ I_{out}  \le 1.0 \text{ m}$ $ I_{out}  \le 1.3 \text{ m}$		0.26 0.26	0.33 0.33	0.40 0.40	JT P
lin	Maximum Input Leakage Current	Vin=VCC or GND	6.0	± 0.1	± 1.0	± 1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 µA	6.0	8	80	160	μА

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

# AC ELECTRICAL CHARACTERISTICS ( $C_1 = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

				PADET	GMOO Gua	aranteed Li	mit	ECOM
Symbol	Parameter			V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	0	(QUE) or bea	2.0 4.5 6.0	5.0 25 29	4.0 20 24	3.4 17 20	MHz
<sup>t</sup> PLH,	Maximum Propagation Delay, Osc In to Q4* (Figures 1 and 4)	0 0 0	Vac=2.6 v Vac=4.5 v Vac=8.0 V	2.0 4.5 6.0	530 106 91	665 133 114	795 159 135	ns
tPLH, tPHL	Maximum Propagation Delay, Osc In to Q14* (Figures 1 and 4)	AND CONTRACT	awolf country	2.0 4.5 6.0	1600 320 272	2000 400 344	2400 480 408	ns
<sup>t</sup> PHL	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	(0)63	nt become type	2.0 4.5 6.0	240 48 41	300 60 51	360 72 61	ns
tPLH, tPHL	Maximum Propagation Delay, QN to QN + 1 (Figures 3 and 4)	enoil	Yest Condi	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)	V 1.0	-ggV to V t.i Au 05	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance				10	10	10	pF

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

For  $T_A = 25^{\circ}C$  and  $C_L = 50$  pF, typical propagation delay from Osc In to other Q outputs may be calculated with the following equations:  $V_{CC} = 2.0 \text{ V}$ : tp = [205 + 107.5(N - 1)] ns  $V_{CC} = 4.5 \text{ V}$ : tp = [41 + 21.5(N - 1)] ns  $V_{CC} = 6.0 \text{ V}$ : tp = [35 + 18.3(N - 1)] ns

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:		
	$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	35	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

		W	Gua			
Symbol	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
trec	Minimum Recovery Time, Reset Inactive to Osc In*	2.0	100	125	150	ns
	(Figure 2)	4.5	20	25	30	
	Y Y Y Y	6.0	17	21	26	
t <sub>W</sub> Minimum Pulse Width, Osc In	2.0	80	100	120	ns	
A	(Figure 1)	4.5	16	20	24	
		6.0	14	17	20	
tw	Minimum Pulse Width, Reset	2.0	80	100	120	ns
1 -	(Figure 2)	4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub> Maxii	Maximum Input Rise and Fall Times	2.0	1000	1000	1000	ns
	(Figure 1)	4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

\*Osc In driven with external clock.

# PIN DESCRIPTIONS

# **INPUTS**

OSC IN (PIN 11) — Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter. Osc In may be driven by an external clock source.

RESET (PIN 12) — Active-high reset. A high level applied to this input asynchronously resets the counter to its zero state (forcing all Q outputs low) and disables the oscillator.

#### **OUTPUTS**

QN + 1

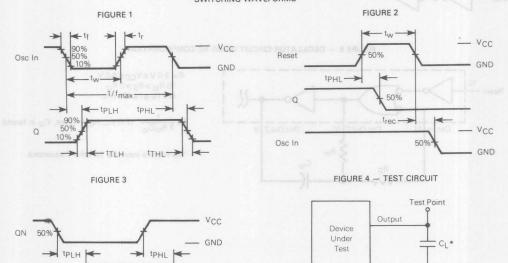
Q4-Q10, Q12-Q14 (PINS 7, 5, 4, 6, 14, 13, 15, 1, 2, 3) - Active-high outputs. Each QN output divides the oscillator

frequency by  $2^{\hbox{\scriptsize N}}.$  The user should note that Q1, Q2, Q3, and Q11 are not available as outputs.

OSC OUT 1, OSC OUT 2 (PINS 10, 9) — Oscillator outputs. These pins are used in conjunction with Osc In and the external components to form an oscillator. (See Figures 4 and 5). When Osc In is being driven with an external clock source, Osc Out 1 and Osc Out 2 must be left open circuited. With the crystal oscillator configuration in Figure 6, Osc Out 2 must be left open circuited.

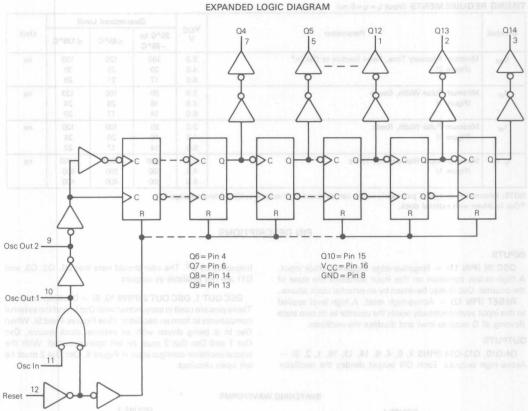
\* Includes all probe and jig capacitance.

# SWITCHING WAVEFORMS



MOTOROLA HIGH-SPEED CMOS LOGIC DATA





# FIGURE 5 — OSCILLATOR CIRCUIT USING RC CONFIGURATION

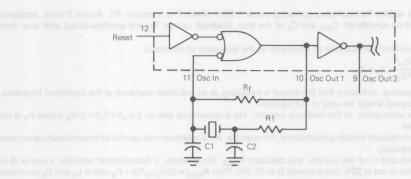
12 Reset Osc Out 1 10 Osc In 11 Osc Out 2 9 Rtc  $R_{\mathsf{S}}$ Ctc

For 2.0  $V \le V_{CC} \le 6.0 \text{ V}$ 10  $R_{tc} > R_S > 2 R_{tc}$ 400 Hz≤f≤400 kHz:

(f in Hz, Rtc in ohms, Ctc in farads)  $f \approx \frac{1}{3 R_{tc} C_{tc}}$ 

The formula may vary for other frequencies.

# FIGURE 6 - PIERCE CRYSTAL OSCILLATOR CIRCUIT



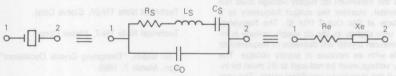
# TABLE 1 — CRYSTAL OSCILLATOR AMPLIFIER SPECIFICATIONS

TA = 25°C (Input = Pin 11, Output = Pin 10)

Type		Positive Reactance (Pierce)
Input Resistance, Rin		60 MΩ minimum
Output Impedance, Zo	ut (4.5 V supply)	200 Ω (see text)
Input Capacitance, Cin		5 pF typical
Output Capacitance, C	out	7 pF typical
Series Capacitance, Ca	arries 2 ent 5	5 pF typical
	(3 Vdc supply	5.0 expected minimum
Open loop voltage	4 Vdc supply	4.0 expected minimum
gain with output at	5 Vdc supply	3.3 expected minimum
full swing, α	6 Vdc supply	3.1 expected minimum

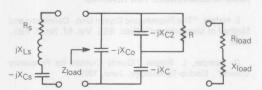
# PIERCE CRYSTAL OSCILLATOR DESIGN

# FIGURE 7 - EQUIVALENT CRYSTAL NETWORKS



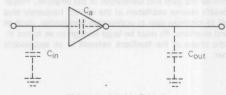
Values are supplied by crystal manufacturer (parallel resonant crystal).

# FIGURE 8 - SERIES EQUIVALENT CRYSTAL LOAD



NOTE:  $C = C1 + C_{in}$  and  $R = R1 + R_{out}$ .  $C_{o}$  is considered as part of the load.  $C_{a}$  and  $R_{f}$  typically have minimal effect below 2 MHz.

# FIGURE 9 — PARASITIC CAPACITANCES OF THE AMPLIFIER



Values are listed in Table 1.

Step 1: Calculate the equivalent series circuit of the crystal at the frequency of oscillation.

$$Z_{e} = \frac{-jX_{C_{0}}(R_{S} + jX_{L_{S}} - jX_{C_{S}})}{-jX_{C_{0}} + R_{S} + jX_{L_{S}} - jX_{C_{S}}} = R_{e} + jX_{e}$$

Reactance jX<sub>e</sub> should be positive, indicating that the crystal is operating as an inductive reactance at the oscillation frequency. The maximum R<sub>s</sub> for the crystal should be used in the equation.

Step 2: Determine  $\beta$ , the attenuation, of the feedback network. For a closed-loop gain of  $2, A_{\nu}\beta = 2, \beta = 2/A_{\nu}$  where  $A_{\nu}$  is the gain of the HC4060 amplifier.

Step 3: Determine the manufacturer's loading capacitance. For example: A manufacturer may specify an external load capacitance of 32 pF at the required frequency.

Step 4: Determine the required Q of the system, and calculate  $R_{load}$ . For example, a manufacturer specifies a crystal Q of 100,000. In-circuit Q is arbitrarily set at 20% below crystal Q or 80,000. Then  $R_{load} = (2\pi f_0 L_S/Q) - R_S$  where  $L_S$  and  $R_S$  are crystal parameters.

Step 5: Simultaneously solve, using a computer,

$$\beta = \frac{X_C \cdot X_{C2}}{R \cdot R_e + X_{C2} (X_e - X_C)} \text{ (with feedback phase shift = 180°)}$$
 (1)

$$X_e = X_{C2} + X_C + \frac{R_e X_{C2}}{R} = X_{Cload}$$
 (where the loading capacitor is an external load, not including Co) (2)

$$R_{load} = \frac{RX_{C_0}X_{C2}[(X_C + X_{C2})(X_C + X_{C_0}) - X_C(X_C + X_{C_0} + X_{C2})]}{X^2C_2(X_C + X_{C_0})^2 + R^2(X_C + X_{C_0} + X_{C2})^2}$$
(3)

Here R = R<sub>out</sub> + R1. R<sub>out</sub> is amp output resistance, R1 is Z. The C corresponding to X<sub>C</sub> is given by C = C1 + C<sub>in</sub>.

Alternately, pick a value for R1 (i.e. let R1=R<sub>s</sub>). Solve Equations 1 and 2 for C1 and C2. Use Equation 3 and the fact that  $Q = 2\pi f_0 L_s/(R_s + R_{load})$  to find in-circuit Q. If Q is not satisfactory pick another value for R1 and repeat the procedure.

#### **CHOOSING R1**

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 limits the drive level.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at Osc Out 2 (Pin 9). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

# SELECTING Rf

The feedback resistor, Rf, typically ranges up to 20 M $\Omega$ . Rf determines the gain and bandwidth of the amplifier. Proper bandwidth insures oscillation at the correct frequency plus roll-off to minimize gain at undesirable frequencies, such as the first overtone. Rf must be large enough so as to not affect the phase of the feedback network in an appreciable manner.

# ACKNOWLEDGEMENTS AND RECOMMENDED REFERENCES

The following publications were used in preparing this data sheet and are hereby acknowledged and recommended for reading:

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

D. Babin, "Designing Crystal Oscillators", Machine Design, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", Machine Design, April 25, 1985.

# ALSO RECOMMENDED FOR READING:

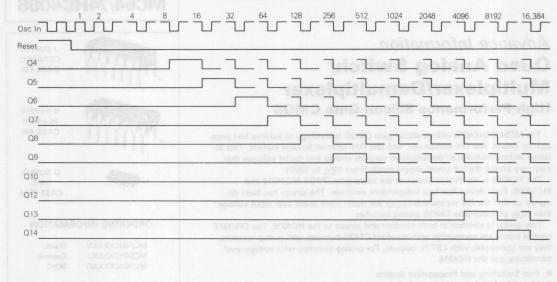
E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", Proc. IEEE, Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", Electro-Technology, June, 1969.

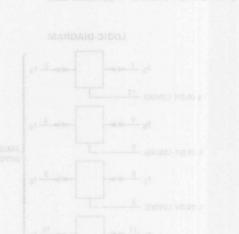
P. J. Ottowitz, "A Guide to Crystal Selection", Electronic Design, May, 1966.

# MC54/74HC4060

# TIMING DIAGRAM







# Advance Information

# Quad Analog Switch/ Multiplexer/Demultiplexer High-Performance Silicon-Gate CMOS

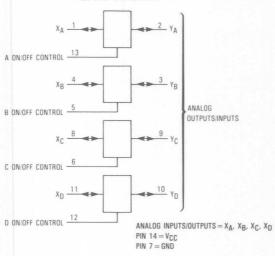
The MC54/74HC4066 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from VCC to GND).

The HC4066 is identical in pinout to the metal-gate CMOS MC14016 and MC14066. Each device has four independent switches. The device has been designed so that the ON resistances (R<sub>ON</sub>) are much more linear over input voltage than R<sub>ON</sub> of metal-gate CMOS analog switches.

This device is identical in both function and pinout to the HC4016. The ON/OFF control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the HC4316.

- · Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range (VCC GND) = 2.0 to 12.0 Volts
- Analog Input Voltage Range (VCC GND) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066 or HC4016
- Low Noise
- Chip Complexity: 44 FETs or 11 Equivalent Gates

#### LOGIC DIAGRAM



# MC54/74HC4066

14

J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

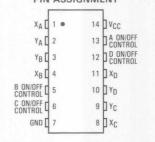
#### ORDERING INFORMATION

MC74HCXXXXN MC54HCXXXXJ MC74HCXXXXD

Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# PIN ASSIGNMENT



# **FUNCTION TABLE**

On/Off Control Input	State of Analog Switch
L	Off
Н	On

This document contains information on a new product. Specifications and information herein are subject to change without notice.

# **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	Positive DC Supply Voltage (Referenced to GND)	-0.5 to +14.0	V
VIS	Analog Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
Vin	Digital Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
- 1	DC Current Into or Out of Any Pin	± 25	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\text{GND} \leq (V_{in})$  or  $V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
Vcc	Positive DC Supply Voltage (Referenced to GND)	2.0	12.0	٧
VIS	Analog Input Voltage (Referenced to GND)	GND	Vcc	V
Vin	Digital Input Voltage (Referenced to GND)	GND	Vcc	V
V <sub>IO</sub> *	Static or Dynamic Voltage Across Switch	_	1.2	V
TA	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Inputs (Figure 10)			ns
	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$	0	1000 500	
	V <sub>CC</sub> = 9.0 V V <sub>CC</sub> = 12.0 V	0	400 250	

<sup>\*</sup>For voltage drops across the switch greater than 1.2 V (switch on), excessive  $V_{CC}$  current may be drawn; i.e., the current out of the switch may contain both  $V_{CC}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

## DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND)

	Parameter	Test Conditions	V	Gua	imit	-024s	
Symbol			VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Voltage ON/OFF Control Inputs	R <sub>on</sub> = Per Spec	2.0 4.5 9.0 12.0	1.5 3.15 6.3 8.4	1.5 3.15 6.3 8.4	1.5 3.15 6.3 8.4	V
V <sub>IL</sub>	Maximum Low-Level Voltage ON/OFF Control Inputs	R <sub>on</sub> = Per Spec	2.0 4.5 9.0 12.0	0.3 0.9 1.8 2.4	0.3 0.9 1.8 2.4	0.3 0.9 1.8 2.4	V
lin	Maximum Input Leakage Current, ON/OFF Control Inputs	V <sub>in</sub> =V <sub>CC</sub> or GND	12.0	±0.1	±1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND V <sub>IO</sub> =0 V	6.0 12.0	2 8	20 80	40 160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

	This device density	J. Bulski		Gua	SHOPS		
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
Ron	Maximum "ON" Resistance	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ to GND $I_{S} \le 2.0$ mA (Figures 1, 2)	2.0† 4.5 9.0 12.0	- 170 85 85	215 106 106	255 130 130	Ω
	opravelend V <sub>IM</sub> and V <sub>IM</sub> or V <sub>IM</sub> and V <sub>IM</sub> or V <sub>IM</sub> seven Or V <sub>IM</sub> as V <sub>IM</sub> or V <sub>IM</sub> as V <sub>IM</sub> or V <sub>IM</sub> as V <sub>IM</sub> or V <sub></sub>	$V_{IN} = V_{IH}$ $V_{IS} = V_{CC}$ or GND (Endpoints) $I_{S} \le 2.0$ mA (Figures 1, 2)	2.0 4.5 9.0 12.0	85 63 63	106 78 78	130 95 95	graff all
ΔR <sub>on</sub>	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$\begin{aligned} &V_{\text{in}} = V_{\text{IH}} \\ &V_{\text{IS}} = 1/2 \; (V_{\text{CC}} - \text{GND}) \\ &I_{\text{S}} \leq 2.0 \; \text{mA} \end{aligned}$	2.0 4.5 9.0 12.0	- 30 20 20	35 25 25	- 40 30 30	Ω
loff	Maximum Off-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IL</sub> V <sub>IO</sub> = V <sub>CC</sub> or GND Switch Off (Figure 3)	12.0	0.1	0.5	1.0	μΑ
lon	Maximum On-Channel Leakage Current, Any One Channel	Vin=VIH VIS=VCC or GND (Figure 4)	12.0	0.1 MO3 EAR	0.5	1.0 33003M	μΑ

<sup>†</sup>At supply voltage (V<sub>CC</sub> – V<sub>EE</sub>) approaching 2 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, ON/OFF Control Inputs: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

		· · ·	Gua	mit		
Symbol	Parameter of Vox=55V	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0 4.5	50 10	65 13	75 15	ns
	V (switch on), exausive V <sub>II</sub> C aurein only be a back-V <sub>IC</sub> and switch input compensus. The	9.0	10 10	13	15 15	
tPLZ, tPHZ	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0 4.5 9.0 12.0	150 30 30 30	190 38 30 30	225 45 30 30	ns
tPZL, tPZH	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0 4.5 9.0 12.0	125 25 25 25 25	160 32 32 32 32	185 37 37 37	ns
V C	Maximum Capacitance ON/OFF Control Input  Control Input = GND  Analog I/O  Feedthrough		35 1.0	10 35 1.0	35 1.0	pF

# NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

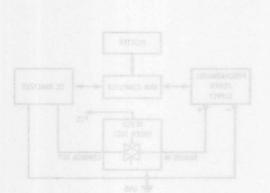
CPD	Power Dissipation Capacitance (Per Switch) (Figure 13)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	Andream Constant Andream	201
	PD = CPD VCC <sup>2</sup> f + ICC VCC	togad 15 mg/ marian	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		41 - 22

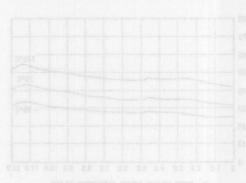
ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

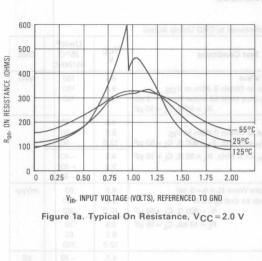
Symbol	Parameter	Test Conditions	V <sub>CC</sub>	Limit* 25°C 54/74HC	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	$\begin{array}{l} f_{in}\!=\!1 \text{ MHz Sine Wave} \\ \text{Adjust } f_{in} \text{ Voltage to Obtain 0 dBm at V}_{OS} \\ \text{Increase } f_{in} \text{ Frequency Until dB Meter Reads } -3 \text{ dB} \\ \text{RL} \!=\! 50 \ \Omega, \ \text{CL} \!=\! 10 \text{ pF} \end{array}$	4.5 9.0 12.0	150 160 160	MHz
	Off-Channel Feedthrough Isolation (Figure 6)	$ \begin{aligned} f_{IR} = & \text{Sine Wave} \\ & \text{Adjust } f_{IR} \text{ Voltage to Obtain 0 dBm at V}_{IS} \\ & f_{IR} = & 10 \text{ kHz}, \text{ R}_{L} = & 600 \Omega, \text{ C}_{L} = & 50 \text{ pF} \end{aligned} $	4.5 9.0 12.0	-50 -50 -50	dB
0.5	16 00 05 01 01 0	$f_{in}$ = 1.0 MHz, R <sub>L</sub> = 50 $\Omega$ , C <sub>L</sub> = 10 pF	4.5 9.0 12.0	-40 -40 -40	10
- ce	Feedthrough Noise, Control to Switch (Figure 7)	$\begin{aligned} &V_{in} \! \leq \! 1 \text{ MHz Square Wave (} t_r \! = \! t_f \! = \! 6 \text{ ns)} \\ &\text{Adjust R}_L \text{ at Setup so that I}_S \! = \! 0 \text{ A} \\ &\text{R}_L \! = \! 600 \ \Omega, \ C_L \! = \! 50 \text{ pF} \end{aligned}$	4.5 9.0 12.0	60 130 200	mVpi
	$R_L = 10 \text{ k}\Omega$ , $C_L = 10$		4.5 9.0 12.0	30 65 100	
	Crosstalk Between Any Two Switches (Figure 12)	$f_{in}$ = Sine Wave Adjust $f_{in}$ Voltage to Obtain 0 dBm at $V_{IS}$ $f_{in}$ = 10 kHz, $R_L$ = 600 $\Omega$ , $C_L$ = 50 pF	4.5 9.0 12.0	-70 -70 -70	dB
		$f_{in}$ = 1.0 MHz, $R_L$ = 50 $\Omega$ , $C_L$ = 10 pF	4.5 9.0 12.0	-80 -80 -80	05
THD	Total Harmonic Distortion (Figure 14)	$f_{in}$ = 1 kHz, $R_L$ = 10 k $\Omega$ , $C_L$ = 50 pF THD = THDMeasured = THDSource $V_{IS}$ = 4.0 Vpp sine wave $V_{IS}$ = 8.0 Vpp sine wave $V_{IS}$ = 11.0 Vpp sine wave	4.5 9.0 12.0	0.10 0.06 0.04	%

<sup>\*</sup>Guaranteed limits not tested. Determined by design and verified by qualification.









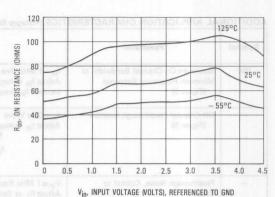
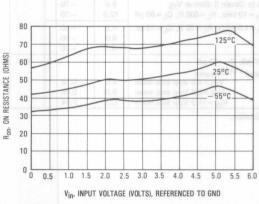


Figure 1b. Typical On Resistance, V<sub>CC</sub> = 4.5 V



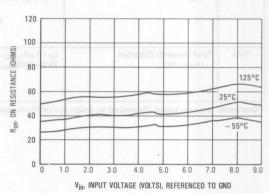
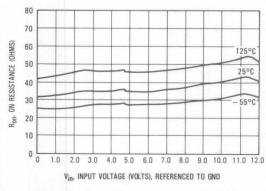


Figure 1c. Typical On Resistance, V<sub>CC</sub> = 6.0 V





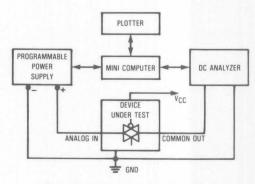


Figure 1e. Typical On Resistance, V<sub>CC</sub> = 12.0 V

Figure 2. On Resistance Test Set-Up

Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

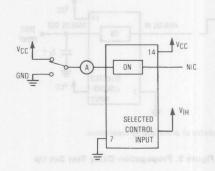
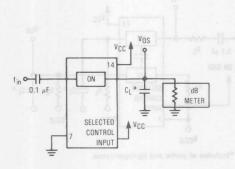
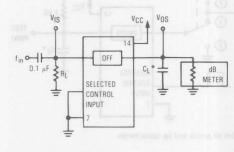


Figure 4. Maximum On Channel Leakage Current, Test Set-Up

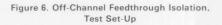


\*Includes all probe and jig capacitance.



\*Includes all probe and jig capacitance.

Figure 5. Maximum On-Channel Bandwidth
Test Set-Up



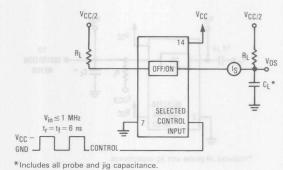


Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up

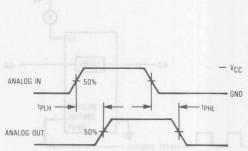
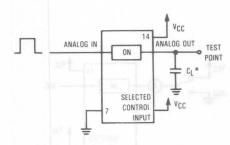


Figure 8. Propagation Delays, Analog In to Analog Out

# MC54/74HC4066



\*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set-Up

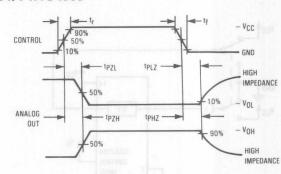
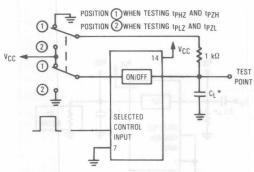
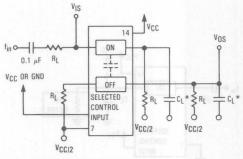


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



\*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set-Up



\*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

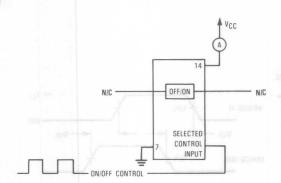
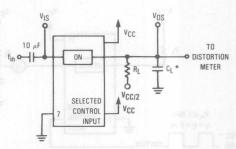


Figure 13. Power Dissipation Capacitance Test Set-Up



\*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set-Up

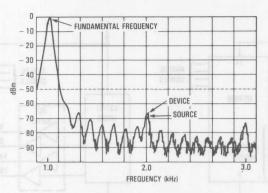


Figure 15. Plot, Harmonic Distortion

### APPLICATION INFORMATION

The ON/OFF Control pins should be at  $V_{CC}$  or GND logic levels,  $V_{CC}$  being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to  $V_{CC}$  or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked-up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V<sub>CC</sub> and GND. The positive peak analog voltage should not exceed V<sub>CC</sub>. Similarly, the negative peak analog voltage should not go below GND. In the example below,

the difference between V<sub>CC</sub> and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above V<sub>CC</sub> and/or below GND are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with MO-sorbs (Motorola high current surge protectors). MO-sorbs are fast turn-on devices ideally suited for precise DC protection with no inherent wear out mechanism.

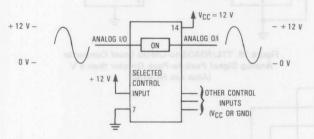


Figure 16. 12 V Application

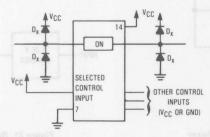


Figure 17. Transient Suppressor Application



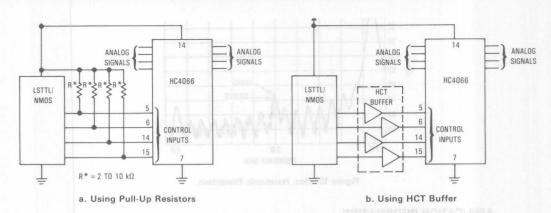


Figure 18. LSTTL/NMOS to HCMOS Interface

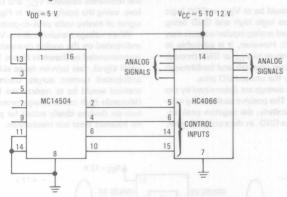


Figure 19. TTL/NMOS-to-CMOS Level Converter Analog Signal Peak-to-Peak Greater than 5 V (Also see HC4316)

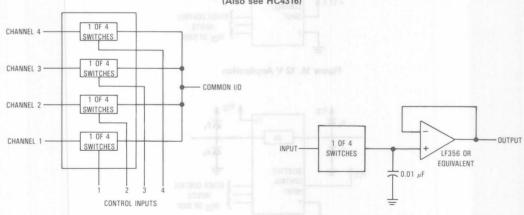


Figure 20. 4-Input Multiplexer

Figure 21. Sample/Hold Amplifier

# Triple 3-Input OR Gate High-Performance Silicon-Gate CMOS

The MC54/74HC4075 is identical in pinout to the MC14075B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 42 FETs or 10.5 Equivalent Gates

# MC54/74HC4075



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



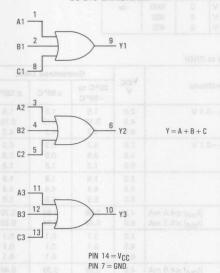
D SUFFIX SOIC CASE 751A

### ORDERING INFORMATION

MC74HCXXXXN MC54HCXXXXJ MC74HCXXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM



#### 

#### **FUNCTION TABLE** Inputs Output В C L L L H X H X X H X H X Н

### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
tr, tf	Input Rise and Fall Time	V <sub>CC</sub> = 2.0 V	0	1000	ns
TV	(Figure 1)	$V_{CC} = 4.5 \text{ V}$	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	Parameter Test Conditions			Vcc	Guaranteed Limit			
Symbol			st Conditions		25°C to -55°C	≤85°C	≤125°C	Uni
VIH	Minimum High-Level Input Voltage $ \begin{vmatrix} V_{\text{Out}} = 0.1 \ \text{V or V}_{\text{CC}} - 0.1 \ \text{V} \\   _{\text{out}}  \leq 20 \ \mu\text{A} \end{vmatrix}                                   $	I <sub>out</sub>   ≤20 μA		4.5	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub>  I <sub>out</sub>   ≤ 20 μA	-0.1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
VOH	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
1		Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{Out}  \le 20 \mu A$		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
		Vin=VIH or VIL	$ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	± 1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

<sup>†</sup>Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

# AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

Symbol		.,	Gua			
	Parameter	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 1 and 2)	2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	-7/36	10	10	10	pF

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	26	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

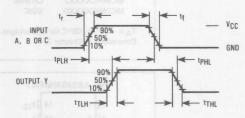
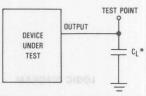


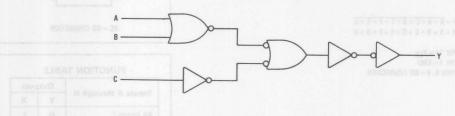
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

# EXPANDED LOGIC DIAGRAM (% of the Device)



# 8-Input NOR/OR Gate High-Performance Silicon-Gate CMOS

The MC54/74HC4078 is similar to the CD4078B metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 30 FETs or 7.5 Equivalent Gates

# MC54/74HC4078



J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



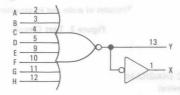
D SUFFIX SOIC CASE 751A

# ORDERING INFORMATION

MC74HCXXXXN MC54HCXXXXJ MC74HCXXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### LOGIC DIAGRAM



 $Y = \overline{A + B + C + D + E + F + G + H}$ X = A + B + C + D + E + F + G + H

PIN 14 = V<sub>CC</sub> PIN 7 = GND PINS 6, 8 = NO CONNECTION

### PIN ASSIGNMENT

	AUUIN	3141AII	1 0 1
ΧC	1 •	14	vcc
A	2	13	JΥ
в[	3	12	Эн
c [	4	11	G
DE	5	10	] F
NC [	6	9	]E
ND [	7	8	NC

NC = NO CONNECTION

### **FUNCTION TABLE**

Inputs A through H	Outputs		
inputs A through H	Υ	Х	
All inputs L	Н	L	
All other combinations	L	Н	

# 5

### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
lin	DC Input Current, per Pin	±20	mA
lout	DC Output Current, per Pin	±25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{\text{in}}$  and  $V_{\text{out}}$  should be constrained to the range  $\text{GND} \leq (V_{\text{in}} \text{ or } V_{\text{out}}) \leq V_{\text{CC}}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	DATE TALAK	Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Reference	ed to GND)	0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	(Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

	17,801				Guaranteed Limit			
Symbol	Parameter	Test Conditions		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$		2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	$V_{\text{out}} = 0.1 \text{ V or } V_{\text{CC}} = 0.0 $ $ I_{\text{out}}  \le 20 \mu\text{A}$	1 V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH Minimum High-Leve Voltage	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	30,1430 0,141,03	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>out</sub>   ≤4.0 mA  I <sub>out</sub>   ≤5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>  ≤20 μA	dang ilin apbelbal	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		Vin=VIH or VIL	I <sub>out</sub>   ≤4.0 mA  I <sub>out</sub>   ≤5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	Vin=VCC or GND		6.0	±0.1	±1.0	±1.0	μΑ
ICC	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA		6.0	2	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (C1 = 50 pF, Input t= t4 = 6 ps)

Symbol	midthan solveb ein?				Guaranteed Limit			
	due to high static voltage	Parameter 2. The of 3.0	Vcc	25°C to -55°C	≤85°C	≤125°C	Unit	
tPLH,	Maximum Propagation Dela	y, Any Input to Output Y	2.0	130	165	195	ns	
tPHL	(Figures 1 and 3)		4.5	26	33	39		
nebegar told sid a seguilov	light eith as aspation.		6.0	22	28	33		
tPLH, Maximum Propagation Delay, Any Input to Output X		y, Any Input to Output X	2.0	140	175	210	ns	
tPHL	(Figures 2 and 3)		4.5	28	35	42		
30/12/11	range GND≤(V <sub>III</sub> of V <sub>O</sub>		6.0	24	30	36		
tTLH,	Maximum Output Transition	Time, Any Output	2.0	75	95	110	ns	
tTHL	(Figures 1, 2, and 3)		4.5	15	19	22		
eu40-(0p)	N. D. WHO HERDER D. D.		6.0	13	16	19	13	
Cin	Maximum Input Capacitano	e	P - StrtC Padage	10	10	10	pF	

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	20	of the
	For load considerations, see Chapter 4 subject listing on page 4-2.	23	þi

# SWITCHING WAVEFORMS

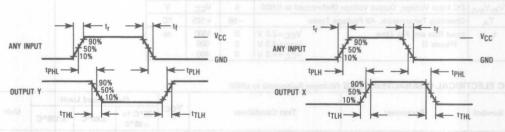


Figure 1

Figure 2

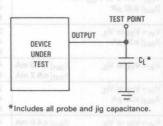
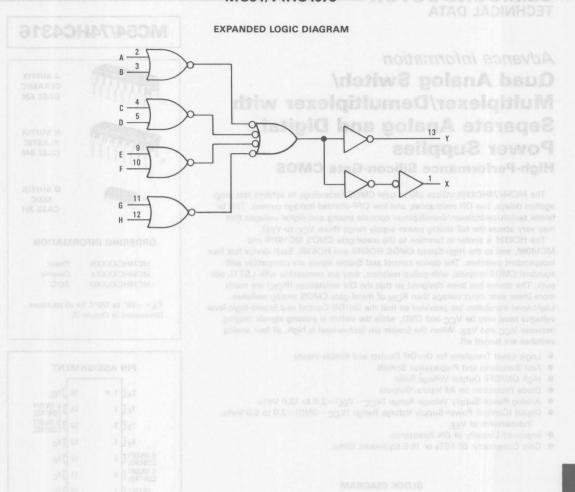


Figure 3. Test Circuit



SMITCH

SMITCH

SMITCH

ANALOS

# Advance Information

# **Quad Analog Switch/** Multiplexer/Demultiplexer with **Separate Analog and Digital Power Supplies**

**High-Performance Silicon-Gate CMOS** 

The MC54/74HC4316 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full analog power-supply range (from VCC to VFF).

The HC4316 is similar in function to the metal-gate CMOS MC14016 and MC14066, and to the High-Speed CMOS HC4016 and HC4066. Each device has four independent switches. The device control and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The device has been designed so that the ON resistances (RON) are much more linear over input voltage than RON of metal-gate CMOS analog switches. Logic-level translators are provided so that the On/Off Control and Enable logic-level voltages need only be VCC and GND, while the switch is passing signals ranging between VCC and VFF. When the Enable pin (active-low) is high, all four analog switches are turned off.

- Logic-Level Translator for On/Off Control and Enable Inputs
- · Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Diode Protection on All Inputs/Outputs
- Analog Power-Supply Voltage Range (VCC VEE) = 2.0 to 12.0 Volts
- Digital (Control) Power-Supply Voltage Range (VCC GND) = 2.0 to 6.0 Volts, Independent of VEE
- Improved Linearity of ON Resistance

5

· Chip Complexity: 66 FETs or 16.5 Equivalent Gates

# MC54/74HC4316



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC **CASE 648** 



D SUFFIX SOIC **CASE 751** 

### ORDERING INFORMATION

MC74HCXXXXN MC54HCXXXXJ MC74HCXXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

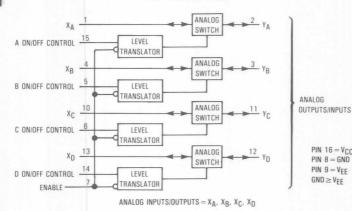
### PIN ASSIGNMENT

			,
XA	1 0	16	]v <sub>cc</sub>
YA	2	15	A ON/OF
YB	3	14	D ON/OF
x <sub>B</sub>	4	13	] X <sub>D</sub>
B ON/OFF CONTROL	5	12	) Y <sub>D</sub>
C ON/OFF CONTROL		11	YC
ENABLE		10	xc
GND	8	9	] V <sub>EE</sub>

### **FUNCTION TABLE**

Inp	uts	State of	
Enable	On/Off Control	Analog Switch	
L	Н	On	
L	L	Off	
Н	X	Off	

**BLOCK DIAGRAM** 



This document contains information on a new product. Specifications and information herein are subject to change without notice

PIN 16 = V<sub>CC</sub>

PIN 8 = GND

PIN 9 = VEE

 $GND \ge V_{EE}$ 

MAXIMUN	RATINGS*
1411/1/41/1014	111/11/11/00

Symbol	Parameter	Value	Unit
Vcc	Positive DC Supply Voltage (Ref. to GND) (Ref. to V <sub>EE</sub> )	-0.5 to +7.0 -0.5 to +14.0	V
VEE	Negative DC Supply Voltage (Ref. to GND)	-7.0 to +0.5	V
VIS	Analog Input Voltage	$V_{EE} - 0.5$ to $V_{CC} + 0.5$	V
Vin	Digital Input Voltage (Ref. to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
1	DC Current Into or Out of Any Pin	± 25	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: - 10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ . Unused inputs must always be tied

This device contains protection

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Paramet	Min	Max	Unit		
Vcc	Positive DC Supply Voltage (Ref	to GND		2.0	6.0	V
VEE	Negative DC Supply Voltage (Re	-6.0	GND	V		
VIS	Analog Input Voltage	VEE	Vcc	V		
Vin	Digital Input Voltage (Ref. to GN	GND	Vcc	V		
V <sub>IO</sub> *	Static or Dynamic Voltage Acros		-	1.2	V	
TA	Operating Temperature, All Pack	S	- 55	+ 125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Control or Enable Inputs)	4,5	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V	0	1000 500	ns
	(Figure 10)		VCC=6.0 V	0	400	

<sup>\*</sup>For voltage drops across the switch greater than 1.2 V (switch on), excessive V<sub>CC</sub> current may be drawn; i.e., the current out of the switch may contain both V<sub>CC</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) VEE=GND Except Where Noted

	01 01 01	- IosaaS 190 NO	Vcc	Gua	imit	0	
Symbol	Parameter	Test Conditions		25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Voltage, Control or Enable Inputs	R <sub>on</sub> =Per Spec	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Voltage, Control or Enable Inputs	R <sub>on</sub> = Per Spec	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
l <sub>in</sub>	Maximum Input Leakage Current, Control or Enable Inputs	V <sub>in</sub> =V <sub>CC</sub> or GND V <sub>EE</sub> = -6.0 V	6.0	±0.1	± 1.0	± 1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	$V_{IO} = V_{CC}$ or GND $V_{IO} = 0$ V $V_{EE} = GND$ $V_{FF} = -6.0$	6.0	2 8	20 80	40 160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to VFF)

	this device contains	Value Value	1,,		Gua	Symo		
Symbol	Parameter Test Conditions	VCC	VEE	25°C to -55°C	≤85°C	≤125°C	Unit	
R <sub>On</sub> Maximum "ON" Resistance		V <sub>in</sub> =V <sub>IH</sub> V <sub>IS</sub> =V <sub>CC</sub> to V <sub>EE</sub> I <sub>S</sub> ≤2.0 mA (Figures 1, 2)	2.0* 4.5 4.5 6.0	0.0 0.0 -4.5 -6.0	320 170 170	400 215 215	480 255 255	Ω
Impedance circuit. Foll seable operation, V <sub>Int</sub> and V <sub>Sult</sub> thought be covered to the range CMD StV <sub>Int</sub> or V <sub>Sult</sub> S-V <sub>C</sub> C.	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or $V_{EE}$ (Endpoints) $I_{S} \le 2.0$ mA (Figures 1, 2)	2.0 4.5 4.5 6.0	0.0 0.0 -4.5 -6.0	180 135 135	225 170 170	270 205 205	gq T	
ΔR <sub>on</sub>	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V <sub>in</sub> =V <sub>IH</sub> V <sub>IS</sub> =1/2 (V <sub>CC</sub> -V <sub>EE</sub> ) I <sub>S</sub> ≤2.0 mA	2.0 4.5 4.5 6.0	0.0 0.0 -4.5 -6.0	30 20 20	- 35 25 25	- 40 30 30	Ω
loff	Maximum Off-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IL</sub> V <sub>IO</sub> = V <sub>CC</sub> or V <sub>EE</sub> Switch Off (Figure 3)	6.0	-6.0	0.1	0.5	1.0	μА
lon	Maximum On-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> or GND (Figure 4)	6.0	-6.0	0.1	0.5	1.0	μА

<sup>\*</sup>At supply voltage (V<sub>CC</sub> – V<sub>EE</sub>) approaching 2 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

### AC ELECTRICAL CHARACTERISTICS (C<sub>1</sub> = 50 pF, Control or Enable: t<sub>r</sub> = t<sub>f</sub> = 6 ns, V<sub>EE</sub> = GND)

	1 22 132			Gua	mit					
Symbol			F	Parameter	1.1 000 1.1 -	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	and the second s	Propagations 8 and 9)	n Delay, A	, Analog Input to Analog Output			60 12 10	75 15 13	90 18 15	ns
tPLZ, tPHZ	The state of the s	Propagations 10 and 11)		ontrol or En	able to Analog Output	2.0 4.5 6.0	250 50 43	315 63 54	375 75 64	ns
<sup>t</sup> PZL <sup>,</sup> <sup>t</sup> PZH	(Figure:	s 10 and 11)			able to Analog Output	2.0 4.5 6.0	265 53 45	335 66 56	400 80 68	ns
С	Maximum	Capacitano	e	ooV	ON/OFF Control	-	10	10	10	pF
	DPBST >				and Enable Inputs  Control Input = GND		-	Parameter		
	41				Analog I/O Feedthrough	00 E	35 1.0	35 1.0	35 1.0	

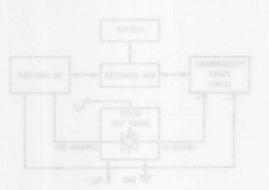
### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Switch) (Figure 13)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	SBA F	
	PD = CPD VCC <sup>2</sup> f + ICC VCC	Madmus Guidfan Sugan	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	Current Jour Placed up 1990	

Parameter	V <sub>C</sub> C V	V <sub>EE</sub>	Limit* 25°C	Unit	
Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	2.25 4.50 6.00	-2.25 -4.50 -6.00	150 160 160	MHz	
Off-Channel Feedthrough Isolation (Figure 6)	$f_{in}$ = Sine Wave Adjust $f_{in}$ Voltage to Obtain 0 dBm at $V_{iS}$ $f_{in}$ = 10 kHz, $R_{L}$ = 600 $\Omega$ , $C_{L}$ = 50 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	-50 -50 -50	dB
	$f_{in}$ = 1.0 MHz, $R_L$ =50 $\Omega$ , $C_L$ = 10 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	-40 -40 -40	100
Feedthrough Noise, Control to Switch (Figure 7)	$V_{in} \le 1$ MHz Square Wave ( $t_r = t_f = 6$ ns) Adjust RL at Setup so that $t_S = 0$ A RL = 600 $\Omega$ , CL = 50 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	60 130 200	mVpp
Typical Oc Resistance, Vcc - Vg	of energia $_{L}=10~k\Omega,~C_{L}=10~pF$	2.25 4.50 6.00	-2.25 -4.50 -6.00	30 65 100	Figur
Crosstalk Between Any Two Switches (Figure 12)	$ \begin{aligned} f_{In} = & \text{Sine Wave} \\ & \text{Adjust } f_{In} \text{ Voltage to Obtain 0 dBm at V}_{IS} \\ & f_{In} = & 10 \text{ kHz, R}_{L} = & 600 \ \Omega, \ C_{L} = & 50 \text{ pF} \end{aligned} $	2.25 4.50 6.00	-2.25 -4.50 -6.00	-70 -70 -70	dB
	f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF		-2.25 -4.50 -6.00	-80 -80 -80	180
Total Harmonic Distortion (Figure 14)	$f_{in}$ = 1 kHz, $R_L$ = 10 k $\Omega$ , $C_L$ = 50 pF THD = THDMeasured - THDSource $V_{IS}$ = 4.0 Vpp sine wave $V_{IS}$ = 8.0 Vpp sine wave $V_{IS}$ = 11.0 Vpp sine wave	2.25 4.50 6.00	-2.25 -4.50 -6.00	0.10 0.06 0.04	%
	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)  Off-Channel Feedthrough Isolation (Figure 6)  Feedthrough Noise, Control to Switch (Figure 7)  Crosstalk Between Any Two Switches (Figure 12)		$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	Maximum On-Channel Bandwidth or   Minimum Frequency Response   Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>OS</sub>   4.50   -4.50   160   160   160

<sup>\*</sup>Limits not tested. Determined by design and verified by qualification.



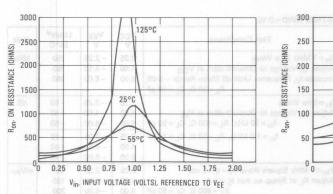


Figure 1a. Typical On Resistance, V<sub>CC</sub> - V<sub>EE</sub> = 2.0 V

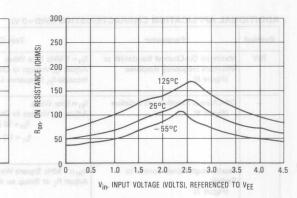


Figure 1b. Typical On Resistance, VCC - VEE = 4.5 V

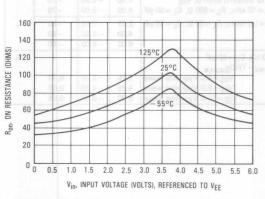


Figure 1c. Typical On Resistance,  $V_{CC} - V_{EE} = 6.0 \text{ V}$ 

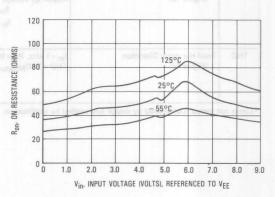


Figure 1d. Typical On Resistance, VCC - VEE = 9.0 V

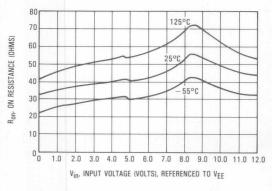


Figure 1e. Typical On Resistance, VCC - VEE = 12.0 V

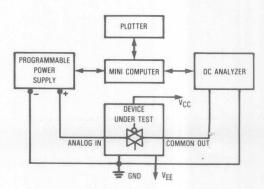


Figure 2. On Resistance Test Set-Up

Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

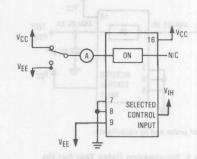
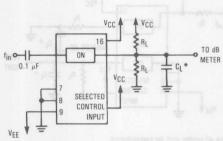
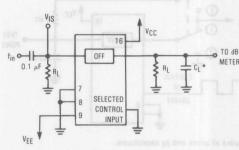


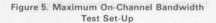
Figure 4. Maximum On Channel Leakage Current, Test Set-Up

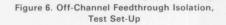


\*Includes all probe and jig capacitance.



\*Includes all probe and jig capacitance.





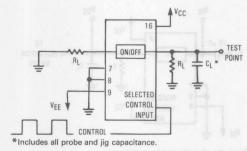


Figure 7. Feedthrough Noise, Control to Analog Out, Test Set-Up

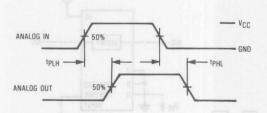
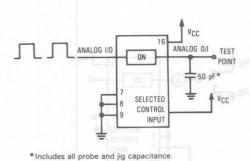


Figure 8. Propagation Delays, Analog in to Analog Out

### MC54/74HC4316



includes all probe and jig capacitation.

Figure 9. Propagation Delay Test Set-Up

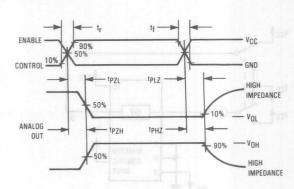
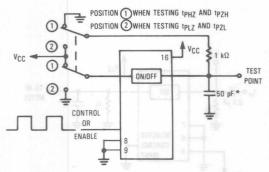
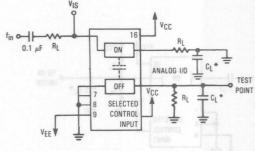


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



\*Includes all probe and jig capacitance.



\*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set-Up

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up (Adjacent Channels Used)

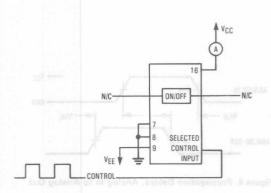
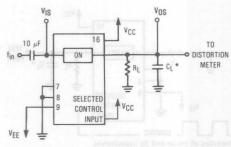


Figure 13. Power Dissipation Capacitance Test Set-Up



\*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set-Up

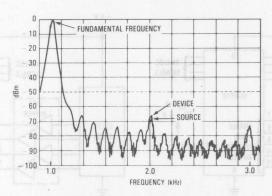


Figure 15. Plot, Harmonic Distortion

### APPLICATION INFORMATION

The Enable and Control pins should be at  $V_{CC}$  or GND logic levels,  $V_{CC}$  being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to  $V_{CC}$  or  $V_{EE}$  through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and  $V_{EE}$ . The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below  $V_{EE}$ . In the example below,

the difference between VCC and VEE is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above VCC and/or below VEE are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with MO•sorbs (Motorola high current surge protectors). MO•sorbs are fast turn-on devices ideally suited for precise dc protection with no inherent wear out mechanism.

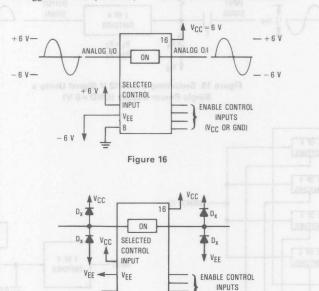


Figure 17. Transient Suppressor Application

(VCC OR GND)

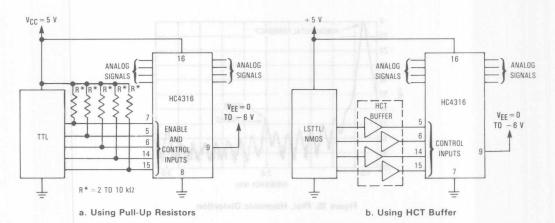


Figure 18. LSTTL/NMOS to HCMOS Interface

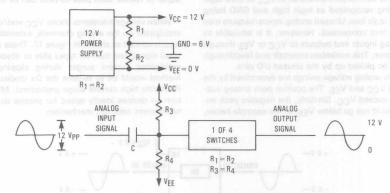


Figure 19. Switching a 0-to-12 V Signal Using a Single Power Supply (GND ≠0 V)

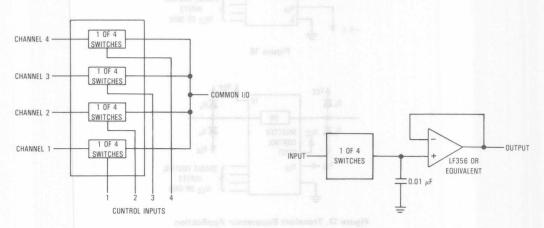


Figure 20. 4-Input Multiplexer

Figure 21. Sample/Hold Amplifier

# Advance Information

# **Analog Multiplexers/ Demultiplexers with Address** Latch

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC4351, MC54/74HC4352, and MC54/74HC4353 utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from VCC to VFF).

The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. The data at the Channel-Select inputs may be latched by using the active-low Latch Enable pin. When Latch Enable is high, the latch is transparent. When either Enable 1 (active low) or Enable 2 (active high) is inactive, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance (Ron) is more linear over input voltage than Ron of metal-gate CMOS analog switches.

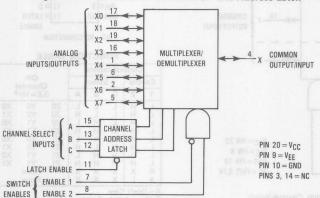
For multiplexers/demultiplexers without latches, see the HC4051, HC4052, and

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (VCC VEE) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range (VCC GND) = 2.0 to 6.0 V Improved Linearity and Lower ON Resistance than Metal-Gate Types
- Low Noise
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: HC4351-222 FETs or 55.5 Equivalent Gates HC4352 - 188 FETs or 47 Equivalent Gates

HC4353-186 FETs or 46.5 Equivalent Gates

### **BLOCK DIAGRAM** MC54/74HC4351

Single-Pole, 8-Position Plus Common Off and Address Latch



# MC54/74HC4351 MC54/74HC4352 MC54/74HC4353



### ORDERING INFORMATION

MC74HCXXXXX MC54HCXXXXJ MC74HCXXXXDW

Ceramic SOIC

SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### PIN ASSIGNMENT MC54/74HC4351

X4 □	1 •	20	b v <sub>cc</sub>
X6 □	2	19	□ X2
NC 🗆	3	18	□ X1
Χ□	4	17	□ X0
X7 🗆	5	16	□ X3
X5 🗆	6	15	□ A □
ENABLE 1	7	14	□ NC
ENABLE 2	8	13	⊐в
V <sub>EE</sub>	9	12	⊐ C
GND 🗆	10	11	LATCH
	0		ENABLE

NC = NO CONNECTION

#### **FUNCTION TABLE** MC54/74HC4351

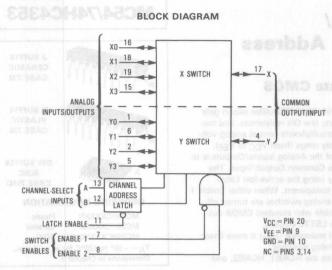
	Cont	Section 1			
Ena	ble	-12	Selec	t	ON Channel
1	2	С	В	Α	(LE = H)*
L	Н	L	L	L	X0
L	Н	L	L	H	X1
L	H	L	H	L	X2
L	H	L	H	H	X3
L	Н	Н	L	L	X4
L	H	Н	L	Н	X5
L	Н	Н	Н	L	X6
L	Н	Н	H	Н	X7
H	X	X	X	X	None
X	L	X	X	X	None

X = don't care

When Latch Enable is low, the Channel Selection is latched and the Channel Address Latch does not change states.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

### MC54/74HC4352 Double-Pole, 4-Position Plus Common Off and Address Latch



# PIN ASSIGNMENT 20 = V<sub>CC</sub> 19 = X2 Y0 -10

Y2 02 NC =3 18 - X1 17 - X Y = 4 Y3 = 5 16 - X0 Y1 0 6 15 X3 ENABLE 1 7 140 NC 13 - A 12 - B VEE = 9 11 LATCH GND = 10

NC = NO CONNECTION

### **FUNCTION TABLE**

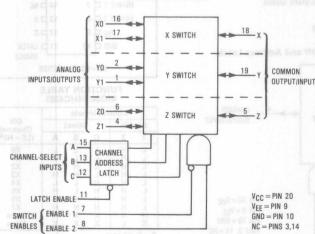
ENABLE

. (	Contro	Input	s	med Dire	41.70
Ena	able	Sel	ect		N
1	2	В	A		H)*
L	Н	- L	Lie	YO	X0
L	Н	L	Н	Y1	X1
L	H	H	L	Y2	X2
L	Н	H	H	Y3	X3
H	X	X	X	No	ne
X	L	X	X	No	ne

### MC54/74HC4353

Triple Single-Pole, Double-Position Plus Common Off and Address Latch

# **BLOCK DIAGRAM**



NOTE:

This device allows independent control of each switch. Channel-Select Input A controls the X Switch, Input B controls the Y Switch, and Input C controls the Z Switch.

PIN	ASSI	SNME	NI
YId	1 0	20	VCC
Y0 🗆	2	19	Y
NC =	3	18	X
Z1 🗆	4	17	X1
Z	5	16	XO
Z0 🗆	6	15	Α
ENABLE 1	7	140	NC
ENABLE 2	8	13	В
VEE	9	12 -	C
GND	10	11	LATCH
87			CALADIA

NC = NO CONNECTION

### **FUNCTION TABLE**

	Cont	rol li	puts	3	1 10100		
Ena	able		Selec	t		ON Channe	al
1	2	С	В	Α		LE = H)	
L	Н	L	L	L	Z0	YO	X0
L	Н	L	L	Н	Z0	Y0	X1
L	H	L	H	L	Z0	Y1	X0
L	Н	L	H	H	Z0	Y1	X1
L	H	H	L	L	Z1	YO	X0
L	H	Н	L	H	Z1	YO	X1
L	Н	Н	H	L	Z1	Y1	X0
L	Н	H	H	H	Z1	Y1	X1
H	X	X	X	X		None	
X	L	X	X	X		None	

X = Don't Care

\*When Latch Enable is low, the Channel
Selection is latched and the Channel Address Latch does not change states.

<sup>\*</sup>When Latch Enable is low, the Channel Selection is latched and the Channel Address Latch does not change states.

### **MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
Vcc	Positive DC Supply Voltage (Ref. to GND) (Ref. to VEE)	-0.5 to +7.0 -0.5 to 14.0	V
VEE	Negative DC Supply Voltage (Ref. to GND)	-7.0 to +0.5	V
VIS	Analog Input Voltage	V <sub>EE</sub> - 0.5 to V <sub>CC</sub> + 0.5	V
Vin	Digital Input Voltage (Ref. to GND)	-1.5 to V <sub>CC</sub> +1.5	٧
1	DC Current Into or Out of Any Pin	± 25	mA
PD	Power Dissipation in Still Air Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions. †Power Dissipation Temperature Derating:

Plastic "N" Package: - 10 mW/°C from 65° to 85°C
Ceramic "J" Package: - 10 mW/°C from 100° to 125°C
SOIC "D" Package: - 7 mW/°C from 65° to 85°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the ranges indicated in the Recommended Operating Conditions.

Unused digital input pins must be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused Analog I/O pins may be left open or terminated. See Applications Information.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	2 02	Min	Max	Unit
Vcc		ef. to GND)	2.0	6.0	. V
		lef. to V <sub>EE</sub> )	2.0	12.0	
VEE	Negative DC Supply Voltage (Re	ef. to GND)	-6.0	GND	V
VIS	Analog Input Voltage		VEE	Vcc	TOOV
Vin	Digital Input Voltage (Ref. to GN	ND)	GND	Vcc	V
VIO*	Static or Dynamic Voltage Acros	ss Switch	-	1.2	٧
TA	Operating Temperature, All Pack	kage Types	- 55	+ 125	°C
tr, tf		/CC=2.0 V	0	1000	ns
		/cc = 4.5 V	0	500	
	Inputs (Figure 9a)	$/_{CC} = 6.0 \text{ V}$	0	400	

<sup>\*</sup>For voltage drops across the switch greater than 1.2 V (switch on), excessive V<sub>CC</sub> current may be drawn; i.e., the current out of the switch may contain both V<sub>CC</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

# DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) VEE = GND, Except Where Noted

	58 73 87	4.5		Gua	aranteed L	imit	
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	R <sub>on</sub> = Per Spec	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	R <sub>on</sub> = Per Spec	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
lin	Maximum Input Leakage Current, Channel-Select or Enable Inputs	$V_{in} = V_{CC}$ or GND, $V_{EE} = -6.0 \text{ V}$	6.0	±0.1	±1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)		6.0	2	20	40	μΑ
		V <sub>EE</sub> = -6.0		8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

# DC ELECTRICAL CHARACTERISTICS Analog Section

	Trils device contains protection of	sint/ euleW			Gua	aranteed L	imit	Minne
Symbol	Parameter	Test Conditions	VCC	VEE	25°C to -55°C	≤85°C	≤125°C	Unit
Ron	Maximum "ON" Resistance	$V_{in} = V_{IL}$ or $V_{IH}$ $V_{IS} = V_{CC}$ to $V_{EE}$ $I_{S} \le 2.0$ mA (Figures 1, 2)	4.5 4.5 6.0	0.0 -4.5 -6.0	190 120 100	240 150 125	280 170 140	Ω
	and V <sub>ext</sub> should be constrained to ranges indicated in the Recorpor Operating Conditions.	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> or V <sub>EE</sub> (Endpoints) I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	4.5 4.5 6.0	0.0 -4.5 -6.0	150 100 80	190 125 100	230 140 115	9.0
ΔR <sub>on</sub>	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IL}$ or $V_{IH}$ $V_{IS} = 1/2 (V_{CC} - V_{EE})$ $I_S \le 2.0 \text{ mA}$	4.5 4.5 6.0	0.0 -4.5 -6.0	30 12 10	35 15 12	40 18 14	Ω
loff	Maximum Off-Channel Leakage Current, Any One Channel	V <sub>in</sub> =V <sub>IL</sub> or V <sub>IH</sub> V <sub>IO</sub> = V <sub>CC</sub> - V <sub>EE</sub> Switch Off (Figure 3)	6.0	-6.0	0.1	0.5	1.0	μΑ
	Maximum Off-Channel Leakage Current, Common Channel HC4351 HC4352	V <sub>in</sub> =V <sub>IL</sub> or V <sub>IH</sub> V <sub>IO</sub> =V <sub>CC</sub> -V <sub>EE</sub> Switch Off (Figure 4)	6.0	-6.0 -6.0	0.2	2.0	4.0	Plaster Carum
	HC4353		6.0	-6.0	0.1	1.0	2.0	-
lon	Maximum On-Channel Leakage Current, Channel to Channel HC4351	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> Switch to Switch = V <sub>CC</sub> - V <sub>EE</sub> (Figure 5)	6.0	-6.0	0.2	2.0	4.0	μΑ
	HC4352 HC4353	2.0 0.8 V. 0.8 0.8 V. 0.8 0.8 V. 0.8 0.8 V.	6.0	-6.0 -6.0	0.1	1.0	2.0	aav

# AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

	V sav	OWD   CNC	Guaranteed Limit			
Symbol	Parameter V S S S S S S S S S S S S S S S S S S	VCC	25°C to -55°C	≤85°C	≤125°C	Uni
tPLH, tPHL	Maximum Propagation Delay, Channel-Select to Analog Output (Figure 9)	2.0 4.5 6.0	370 74 63	465 93 79	550 110 94	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)		60 12 10	75 15 13	90 18 15	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Enable to Analog Output (Figure 12)		325 65 55	410 82 70	485 97 82	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Enable 1 or 2 to Analog Output (Figure 11)		290 58 49	365 73 62	435 87 74	ns
tPZL, tPZH	Maximum Propagation Delay, Enable 1 or 2 to Analog Output (Figure 11)	2.0 4.5 6.0	345 69 59	435 87 74	515 103 87	ns
Cin	Maximum Input Capacitance		10	10	10	pF
C <sub>I/O</sub>	Maximum Capacitance Analog I/O Enable 1 = V <sub>IH</sub> , Enable Common O/I: HC4351 HC4352	2=V <sub>IL</sub> -	35 130 80	35 130 80	35 130 80	pF
	HC4353 HC4353 Feedthrough	OMD to IDV=mi	50	50	50	

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) (Figure 14)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:	OU DES	
	PD=CPD VCC2f+ICC VCC	45 (HC4351)	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.	80 (HC4352)	
		45 (HC4353)	

TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

	7*			Gua			
Symbol	Parameter		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Channel-Select to Latch Enable (Figure 12)	2020	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>h</sub>	Minimum Hold Time, Latch Enable to Channel Select (Figure 12)	0.65	2.0 4.5 6.0	0 0 0	0 0 0	0 0 0	ns
t <sub>W</sub>	Minimum Pulse Width, Latch Enable (Figure 12)		2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times, Channel-Select, Latch Ena and Enables 1 and 2	ble,	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

# ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0.0 V)

			Vcc	V/	Limit*			
Symbol	Parameter	Test Condition		Parameter Test Condition		VEE	25°C 54/74HC	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 6)	$\begin{split} f_{in} = 1 & \text{ MHz Sine Wave} \\ & \text{Adjust } f_{in} & \text{ Voltage to Obtain 0 dBm at V}_{OS} \\ & \text{Increase } f_{in} & \text{ Frequency Until dB Meter} \\ & \text{Reads } - 3 & \text{dB} \\ & \text{R}_{L} = 50 & \Omega, \text{ C}_{L} = 10 \text{ pF} \end{split}$	2.25 4.50 6.00	-2.25 -4.50 -6.00	51 52 53 80 95 120 80 95 120 80 95 120	MH		
Trail	Off-Channel Feedthrough Isolation (Figure 7)	$\begin{split} f_{\text{In}} &\equiv \text{Sine Wave} \\ \text{Adjust } f_{\text{In}} &\text{ Voltage to Obtain 0 dBm at V}_{\text{IS}} \\ f_{\text{In}} &= 10 \text{ kHz}, \text{ R}_{\text{L}} = 600 \Omega, \text{ C}_{\text{L}} = 50 \text{ pF} \\ \end{split}$ $f_{\text{In}} &= 1.0 \text{ MHz}, \text{ R}_{\text{L}} = 50 \Omega, \text{ C}_{\text{L}} = 10 \text{ pF} \end{split}$	2.25 4.50 6.00 2.25 4.50 6.00	-2.25 -4.50 -6.00 -2.25 -4.50 -6.00	-50 -50 -50 -40 -40 -40	dB		
V 0.6	Feedthrough Noise, Channel Select Input to Common O/I (Figure 8)	$V_{in} \le 1$ MHz Square Wave $(t_f = t_f = 6 \text{ ns})$ Adjust $R_L$ at Setup so that $I_S = 0$ A Enable = GND $R_L = 600 \ \Omega$ , $C_L = 50 \ pF$ $R_L = 10 \ k\Omega$ , $C_L = 10 \ pF$	2.25 4.50 6.00 2.25 4.50 6.00	-2.25 -4.50 -6.00 -2.25 -4.50 -6.00	25 106 135 35 145 190	mVp		
masya	Crosstalk Between Any Two Switches (Figure 13) (Test does not apply to HC4351)	$\begin{split} f_{in} &= \text{Sine Wave} \\ \text{Adjust } f_{in} & \text{Voltage to Obtain 0 dBm at V}_{IS} \\ f_{in} &= 10 \text{ kHz}, \ R_L = 600 \ \Omega, \ C_L = 50 \text{ pF} \\ \end{split}$ $f_{in} &= 1 \text{ MHz}, \ R_L = 50 \ \Omega, \ C_L = 10 \text{ pF} \\ \end{split}$	2.25 4.50 6.00 2.25 4.50 6.00	-2.25 -4.50 -6.00 -2.25 -4.50 -6.00	-50 -50 -50 -60 -60	dB		
THD	Total Harmonic Distortion (Figure 15)	$\begin{array}{l} f_{1n} = 1 \text{ kHz, } R_L = 10 \text{ k}\Omega, \ C_L = 50 \text{ pF} \\ \text{THD} = \text{THD}_{Measured} - \text{THD}_{Source} \\ V_{IS} = 4.0 \text{ Vpp sine wave} \\ V_{IS} = 8.0 \text{ Vpp sine wave} \\ V_{IS} = 11.0 \text{ Vpp sine wave} \end{array}$	2.25 4.50 6.00	-2.25 -4.50 -6.00	0.10 0.08 0.05	%		

<sup>\*</sup>Limits not tested. Determined by design and verified by qualification.

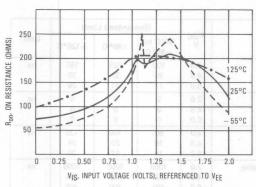


Figure 1a. Typical On Resistance, V<sub>CC</sub> - V<sub>EE</sub> = 2.0 V

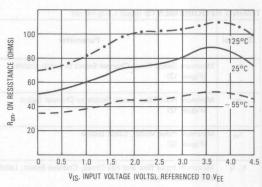


Figure 1b. Typical On Resistance, VCC - VEE = 4.5 V

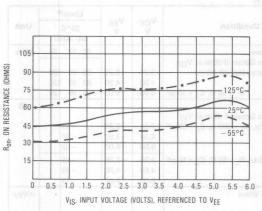


Figure 1c. Typical On Resistance, V<sub>CC</sub> - V<sub>EE</sub> = 6.0 V

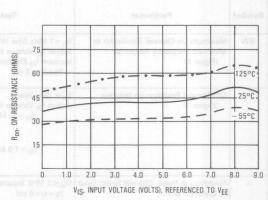


Figure 1d. Typical On Resistance, V<sub>CC</sub> - V<sub>EE</sub> = 9.0 V

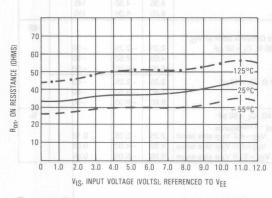


Figure 1e. Typical On Resistance,  $V_{CC} - V_{EE} = 12.0 \text{ V}$ 

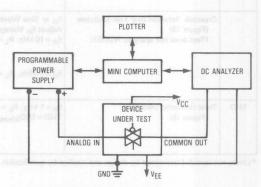


Figure 2. On Resistance Test Set-Up

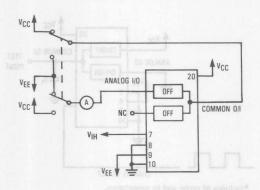


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

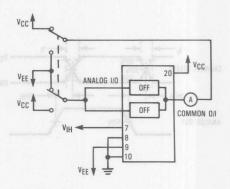


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

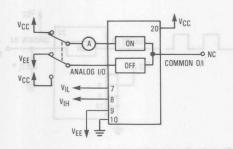
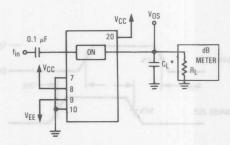


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



\*Includes all probe and jig capacitance.

Figure 6. Maximum On-Channel Bandwidth
Test Set-Up

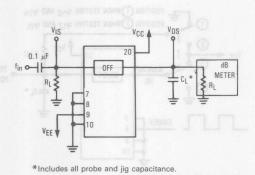
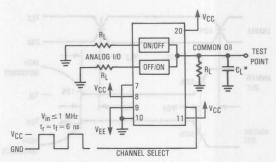


Figure 7. Off-Channel Feedthrough Isolation,

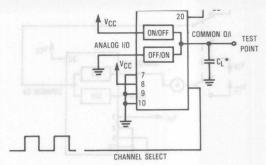
Test Set-Up



\*Includes all probe and jig capacitance.

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

Figure 9a. Propagation Delays, Channel Select to Analog Out



\*Includes all probe and jig capacitance.

Figure 9b. Propagation Delay, Test Set-Up Channel Select to Analog Out

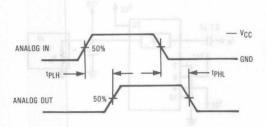
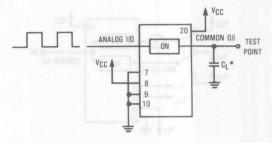


Figure 10a. Propagation Delays, Analog In to Analog Out



<sup>\*</sup>Includes all probe and jig capacitance.

Figure 10b. Propagation Delay, Test Set-Up
Analog In to Analog Out

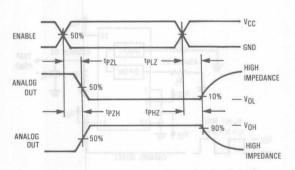
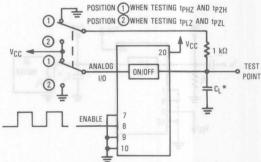
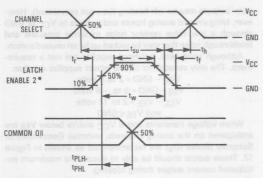


Figure 11a. Propagation Delay, Enable 1 or 2 to Analog Out



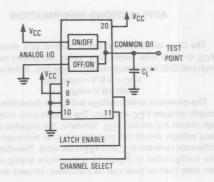
\*Includes all probe and jig capacitance.

Figure 11b. Propagation Delay, Test Set-Up Enable to Analog Out



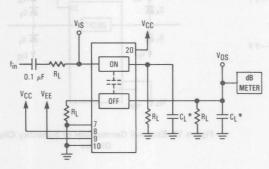
\*Latch Enable 1 is a similar waveform except the Latch Enable waveform is inverted.

Figure 12a. Propagation Delay, Latch Enable to **Analog Out** 



\*Includes all probe and jig capacitance.

Figure 12b. Propagation Delay, Test Set-Up Latch Enable to Analog Out



\*Includes all probe and jig capacitance.

Figure 13. Crosstalk Between Any Two Switches, Test Set-Up

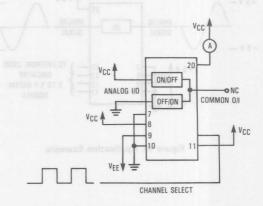


Figure 14. Power Dissipation Capacitance, Test Set-Up

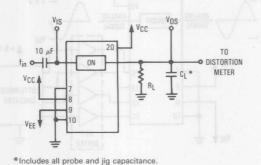
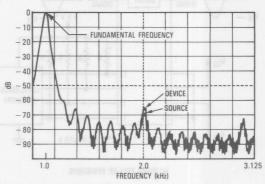


Figure 15a. Total Harmonic Distortion, Test Set-Up Figure 15b. Plot, Harmonic Distortion



### APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at VCC or GND logic levels. VCC being recognized as a logic high and GND being recognized as a logic low. In this example:

V<sub>CC</sub> = +5 V = logic high GND = 0 V = logic low

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and  $V_{EE}$ . The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below  $V_{EE}$ . In this example, the difference between  $V_{CC}$  and  $V_{EE}$  is ten volts. Therefore, using the configuration in Figure 16, a maximum analog signal of ten volts peak-to-peak can be controlled. Unused analog in

puts/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V<sub>CC</sub> or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

 $V_{CC}$  - GND = 2 to 6 volts  $V_{EE}$  - GND = 0 to -6 volts  $V_{CC}$  -  $V_{EE}$  = 2 to 12 volts and  $V_{EE}$   $\leq$  GND

When voltage transients above V<sub>CC</sub> and/or below V<sub>EE</sub> are anticipated on the analog channels, external Germanium or Schottky diodes (D<sub>X</sub>) are recommended as shown in Figure 17. These diodes should be able to absorb the maximum anticipated current surges during clipping.

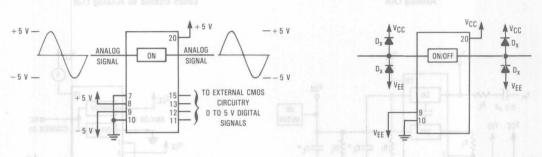


Figure 16. Application Example

Figure 17. External Germanium or Schottky Clipping
Diodes

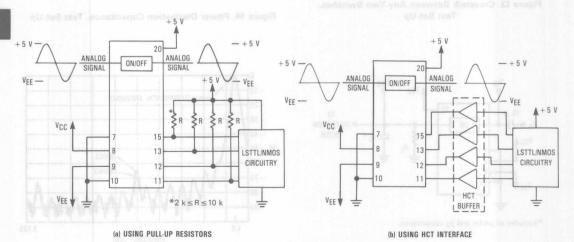
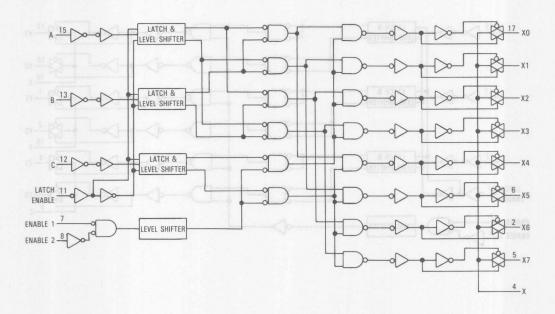
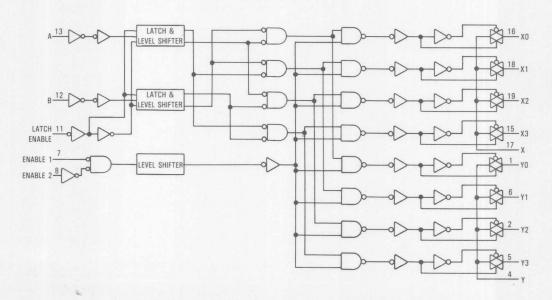


Figure 18. Interfacing LSTTL/NMOS to CMOS Inputs

### **FUNCTION DIAGRAM HC4351**



### **FUNCTION DIAGRAM HC4352**



# BCD-to-Seven-Segment Latch/ Decoder/Display Driver High-Performance Silicon-Gate CMOS

The MC54/74HC4511 is identical in pinout to the MC14511 metal-gate CMOS decoder/driver. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC4511 provides the functions of a 4-bit storage latch, a BCD-to-seven-segment decoder, and a display driver. It can be used either directly or indirectly with seven-segment light-emitting diode (LED), incandescent, fluorescent, gas discharge, or liquid-crystal readouts. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn off or pulse modulate the brightness of the display, and to store a BCD code, respectively.

- Latch Storage of BCD Inputs
- Blanking Input
- Lamp Test Input
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 264 FETs or 66 Equivalent Gates

# MC54/74HC4511



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648

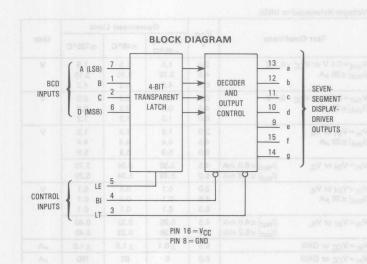


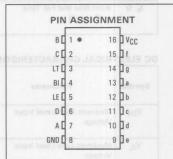
D SUFFIX SOIC CASE 751B-01

### ORDERING INFORMATION

MC74HCXXXXN MC54HCXXXXJ MC74HCXXXXD Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.







### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
a l <sub>in</sub>	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±70	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature, All Package Types		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>		V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0	1000 500 400	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub>	Guaranteed Limit			
				25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu \text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	٧
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
VOH	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
	C Leven	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 6.0 \text{ mA}$ $ I_{out}  \le 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
VOL	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1		V
	BEPESHO!	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
ICC	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions. †Derating — Plastic DIP:  $-10~\rm mW/^\circ C$  from 65° to 125°C

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter		Gua			
		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input A, B, C, or D to Output (Figures 1 and 6)	2.0 4.5 6.0	600 120 102	750 150 129	900 180 153	ns
tPLH, tPHL	Maximum Propagation Delay, Latch Enable to Output (Figures 2 and 6)	2.0 4.5 6.0	600 120 102	750 150 129	900 180 153	ns
tPLH, tPHL	Maximum Propagation Delay, Blanking Input to Output (Figures 3 and 6)	2.0 4.5 6.0	600 120 102	750 150 129	900 180 153	ns
tPLH, tPHL	Maximum Propagation Delay, Lamp Test to Output (Figures 4 and 6)	2.0 4.5 6.0	600 120 102	750 150 129	900 180 153	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 3 and 6)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	-	10	10	10	pF

### NOTES:

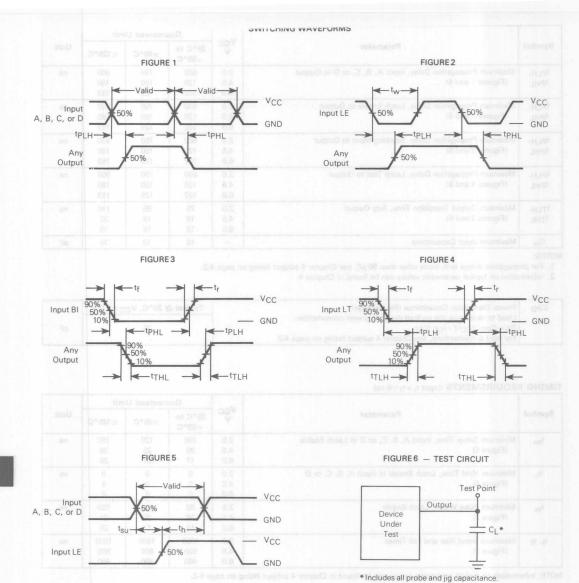
For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
 Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	16 Jugat
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC	70	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

### TIMING REQUIREMENTS (Input to = ta = 6 ms)

Symbol	Parameter	V <sub>CC</sub>	Gua	1			
			25°C to -55°C	≤85°C	≤125°C	Unit	
t <sub>su</sub>	Minimum Setup Time, Input A, B, C, or D to Latch Enable (Figure 5)		2.0 4.5	100 20	125 25	150 30	ns
th	Minimum Hold Time, Latch Enable to Input A, B, C, or D		6.0 2.0	17	0	26	ns
"	(Figure 5)		4.5 6.0	0	0	0	
t <sub>W</sub>	Minimum Pulse Width, Latch Enable (Figure 2)	OVID	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 3)	204	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.



		Inputs								(	Out	put	S	
LE	ВІ	LT	D	С	В	Α	a	b	С	d	е	f	g	Display
X	X	L	X	X	X	X	Н	Н	Н	Н	Н	Н	Н	8
X	L	Н	X	X	X	X	L	L	L	L	L	L	L	Blank
L	Н	Н	L	L	L	L	Н	Н	Н	Н	Н	Н	L	0
L	Н	Н	L	L	L	Н	L	Н	H	L	L	L	L	1
L	Н	Н	L	L	Н	L	Н	H	L	Н	Н	L	Н	2
L	Н	Н	L	L	Н	Н	Н	Н	Н	Н	L	L	Н	3
L	Н	Н	L	Н	L	L	L	Н	Н	L	L	Н	Н	4
L	Н	Н	L	H	L	Н	H	L	H	Н	L	Н	Н	5
L	H	Н	L	Н	Н	L	L	L	H	Н	H	H	Н	6
L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	L	L	L	7
L	Н	Н	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	8
L	Н	Н	H	L	L	Н	Н	Н	H	L	L	Н	H	9
L	Н	Н	H	L	Н	L	L	L	L	L	L	L	L	Blank
L	Н	Н	Н	L	Н	Н	L	L	L	L	L	L	L	Blank
L	Н	Н	Н	Н	L	L	L	L	L	L	L	L	L	Blank
L	Н	Н	H	Н	L	Н	L	L	L	L	L	L	L	Blank
L	Н	Н	Н	H	Н	L	L	L	L	L	L	L	L	Blank
L	Н	Н	Н	Н	Н	Н	L	L	L	L	L	L	L	Blank
Н	Н	Н	X	X	X	X				*			1	*

<sup>\* =</sup> Depends upon the BCD code previously applied while LE was at a low level.

## PIN DESCRIPTIONS

#### **INPUTS**

A, B, C, D (PINS 7, 1, 2, 6) — BCD inputs. A (pin 7) is the least significant bit and D (pin 6) is the most significant bit. Hexadecimal code A-F at these inputs causes the outputs to assume a low level, offering an alternate method of blanking the display.

### OUTPUTS

a, b, c, d, e, f, g (PINS 13, 12, 11, 10, 9, 15, 14) — Decoded, buffered seven-segment display-driver outputs. These outputs, unlike the MC14511, have CMOS drivers, which produce typical CMOS output voltage levels. These outputs are connected to various displays as shown in Figure 7.

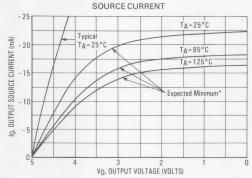
#### CONTROL INPUTS

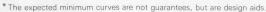
BI (PIN 4) — Active-low display blanking input. A low level on this input will cause all outputs to be held low, thereby blanking the display. LT is the only input that overrides the BI input.

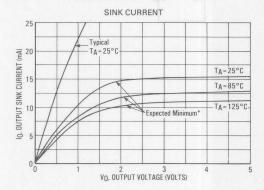
LT (PIN 3) — Active-low lamp test. A low level on this input causes all outputs to assume a high level. This input allows the user to test all segments of a display with a single control input. This input is independent of all other inputs.

LE (PIN 5) — Latch enable input. This input controls the 4-bit transparent latch. A high level on this input latches the code present at the A, B, C and D inputs; a low level allows the code to be transmitted through the latch to the decoder.

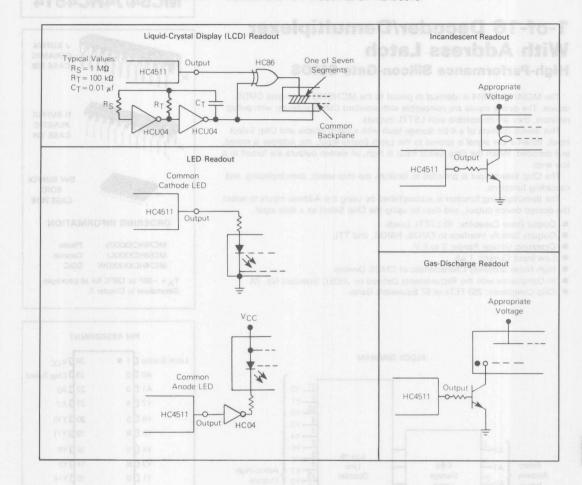
# OUTPUT CHARACTERISTIC CURVES (V<sub>CC</sub> = 5 V)







### FIGURE 7 - CONNECTIONS TO VARIOUS DISPLAY READOUTS



# **High-Performance Silicon-Gate CMOS**

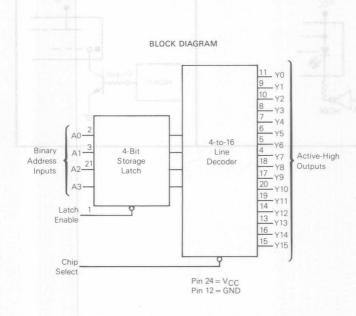
The MC54/74HC4514 is identical in pinout to the MC14514B metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

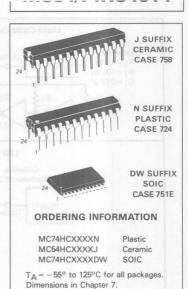
This device consists of a 4-bit storage latch with a Latch Enable and Chip Select input. When a low signal is applied to the Latch Enable input, the Address is stored, and decoded. When the Chip Select input is high, all sixteen outputs are forced to a low level.

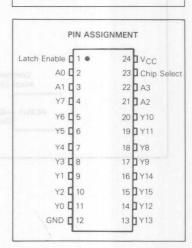
The Chip Select input is provided to facilitate the chip-select, demultiplexing, and cascading functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using the Chip Select as a data input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 268 FETs or 67 Equivalent Gates







# 5

#### MAXIMUM BATINGS\*

Symbol	Parameter Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
Vin	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	٧
lin	DC Input Current, per Pin	± 20	mA
lout	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP1 SOIC Package1	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{In}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)	DC Supply Voltage (Referenced to GND)		6.0	V
V <sub>in</sub> ,V <sub>out</sub>	DC Input Voltage, Output Voltage (Refer	enced to GND)	0	Vcc	V
TA	Operating Temperature, All Package Type	es	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> =2.0 V	0	1000	ns
	(Figure 1)	V <sub>CC</sub> = 4.5 V	0	500	
		$V_{CC} = 6.0 \text{ V}$	0	400	

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

			V	Gua			
Symbol	Parameter	Test Conditions	VCC	25°C to -55°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
Voн	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	14 17 20	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	11.4
VOL	Maximum Low-Level Output Voltage	$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

Symbol	This makes contains	Value Usir			Gua	Symbol		
	circuity to guard equito due to high stedle votage	Parameter (1) (1) (2) (3)		V <sub>CC</sub>	25°C to -55°C	≤85°C	≤125°C	Unit
tPLH,	Maximum Propagation Delay	, Chip Select to Output Y		2.0	175	220	265	ns
tPHL	(Figures 1 and 5)			4.5 6.0	35 30	44 37	53 45	
tPLH	Maximum Propagation Delay	, Input A to Output Y		2.0	230	290	345	ns
rtt of ber	(Figures 2 and 5)			4.5	46	58	69	
	range GND siV <sub>in</sub> of V <sub>ol</sub>			6.0	39	49	59	
tPHL	Unused Inputs multi alw			2.0	175	220	265	
	to an appropriete logic vi			4.5	35	44	53	
	10 V to UND 15/155 (0.0)			6.0	30	37	45	
tPLH	Maximum Propagation Delay	, Latch Enable to Output Y	Pagkagel	2.0	230	290	345	ns
	(Figures 3 and 5)			4.5	46	58	69	
				6.0	39	49	59	
tPHL				2.0	175	220	265	
				4.5	35	44	53	
				6.0	30	37 510	450	
tTLH,	Maximum Output Transition		2005	2.0	75	95	110	ns
THL	(Figures 1 and 5)			4.5	15	19	22	
				6.0	13	16	19	
Cin	Maximum Input Capacitance			DIA-NT	10	10	10	pF

### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package)	Typical @ 25°C, V <sub>CC</sub> =5.0 V	
	Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC	70 11 Stugill	pF
	For load considerations, see Chapter 4 subject listing on page 4-2.		

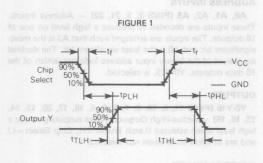
# TIMING REQUIREMENTS (Input $t_f = t_f = 6$ ns)

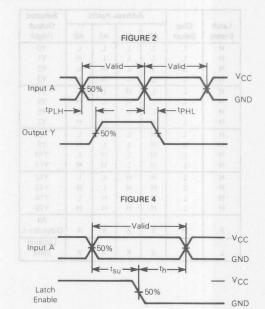
	Yest Candisions VCC 201C to		Gua	to deave		
		VCC	25°C to -55°C	≤85°C	≤125°C	Unit
t <sub>su</sub>	Minimum Setup Time, Input A to Latch Enable (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Latch Enable to Input A (Figure 4)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t <sub>w</sub>	Minimum Pulse Width, Latch Enable (Figure 3)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

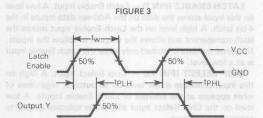
NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

# MC54/74HC4514

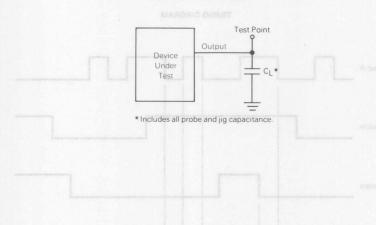
#### SWITCHING WAVEFORMS







#### FIGURE 5 - TEST CIRCUIT



h

		Address Inputs				Selected
Latch Enable	Chip Select	A3	A2	A1	A0	Output (High)
Н	L	L	L	L	L	YO
Н	L	L	L	L	Н	Y1-
Н	t-plisy	L	F	H	L	Y2
Н	L	L	L	Н	Н	Y3
Н	L	L	Н	L	L	Y4
Н		L	H	L	H	Y5
Н	1-0	L	Н	H	L	Y6
Н	L	L	Н	Н	Н	Y7
Н	L	Н	L	L	L	Y8
Н		H	L	L	H	Y9
Н	L	Н	L	Н	L	Y10
Н	L	Н	L	Н	Н	Y11
Н	L	Н	Н	L	L	Y12
Н	L	Н	Н	L	Н	Y13
Н	L	H	u.Her	Н	L	Y14
Н	L	Н	Н	Н	Н	Y15
X	Н	X	×	X	×	All Outputs = l
1	X	×	X	×	×	Latched Data

#### ADDRESS INPUTS

A0, A1, A2, A3 (PINS 2, 3, 21, 22) — Address Inputs. These inputs are decoded to produce a high level on one of 16 outputs. The inputs are arranged such that A3 is the most-significant bit and A0 is the least-significant bit. The decimal equivalent of the binary input address indicates which of the 16 data outputs, Y0-Y15, is selected.

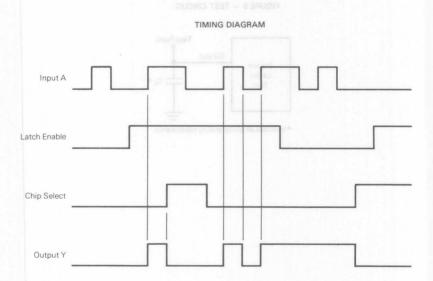
#### OUTPUTS

Y0-Y15 (PINS 11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15) — Active-High Outputs. These outputs produce a high level when selected (Latch Enable = H, Chip Select = L) and are at a low level when not selected.

#### CONTROL INPUTS

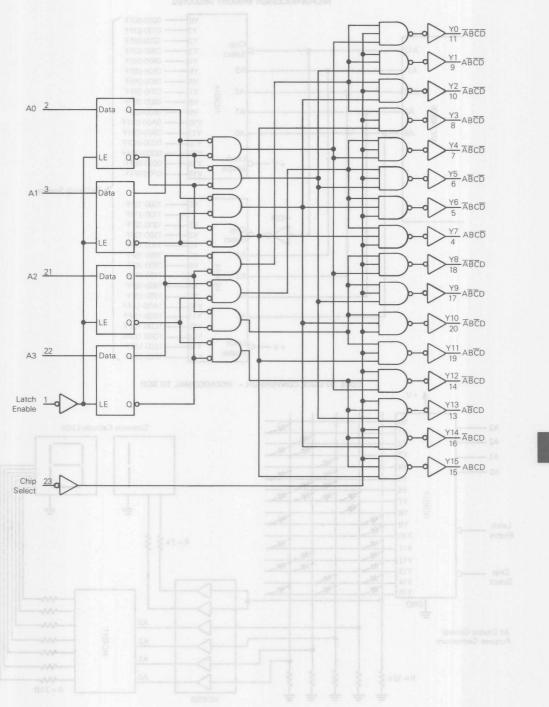
**LATCH ENABLE (PIN 1)** — Latch Enable Input. A low level on this input stores the data on the Address data inputs in the 4-bit latch. A high level on the Latch Enable input makes the latch transparent and allows the outputs to follow the inputs. Note that the data is latched only while the Latch Enable input is at a low level.

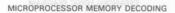
CHIP SELECT (PIN 23) — Chip Select Input. A high on this input produces a low level on all outputs, regardless of what appears at the address or Latch Enable inputs. A low level on the Chip Select input allows the selected output to produce a high level.

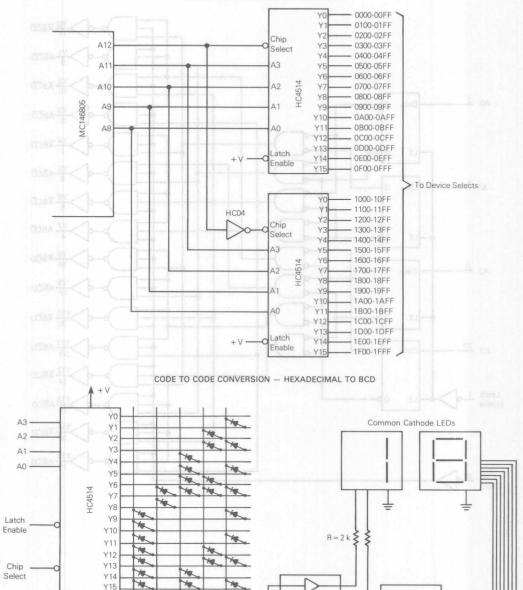


# MC54/74HC4514

EXPANDED LOGIC DIAGRAM







5

GND

R = 10 k

All Diodes General

Purpose Germanium

HC4050

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 $R = 2 k\Omega$ 

HC4511

A1

A0

# Dual Precision Monostable Multivibrator (Retriggerable, Resettable)

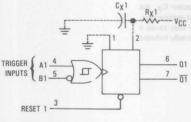
# **High-Performance Silicon-Gate CMOS**

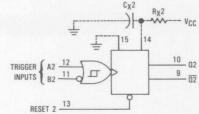
The MC54/74HC4538 is identical in pinout to the MC14538B and the MC14528B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This dual monostable multivibrator may be triggered by either the positive or the negative edge of an input pulse, and produces a precision output pulse over a wide range of pulse widths. Because the device has conditioned trigger inputs, there are no trigger-input rise and fall time restrictions. The output pulse width is determined by the external timing components,  $R_{\mbox{$\chi$}}$  and  $C_{\mbox{$\chi$}}$ . The device has a reset function which forces the Q output low and the  $\overline{\mbox{$\Omega$}}$  output high, regardless of the state of the output pulse circuitry.

- Unlimited Rise and Fall Times Allowed on the Trigger Inputs
- Output Pulse Width is Independent of the Trigger Pulse Width
- ± 10% Guaranteed Pulse Width Variation from Part to Part (Using the Same Test Jig)
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 145 FETs or 36 Equivalent Gates

### **BLOCK DIAGRAM**





PIN 16 = V<sub>CC</sub> PIN 8 = GND

R<sub>X</sub> AND C<sub>X</sub> ARE EXTERNAL COMPONENTS PIN 1 AND PIN 15 MUST BE HARD WIRED TO GND

# MC54/74HC4538



J SUFFIX CERAMIC CASE 620



N SUFFIX PLASTIC CASE 648



DW SUFFIX SOIC CASE 751G

#### ORDERING INFORMATION

MC74HCXXXXN Plastic MC54HCXXXXJ Ceramic MC74HCXXXXDW SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

### PIN ASSIGNMENT

|                 | 710011      | 7                       |    |
|-----------------|-------------|-------------------------|----|
| GND [           | 1 •         | 16 7 VCC                |    |
| CX1/RX1[        | 2           | 15 GND                  |    |
| RESET 1         | 3           | 14 CX2/R                | χ2 |
| A1 [            | 4           | 13 RESET                | 2  |
| B1 [            | 5           | 12 ] A2                 |    |
| 01 [            | 6           | 11 382                  |    |
| 01 [            | 7           | 10 02                   |    |
| GND [           | 8           | 9 ] 02                  |    |
| men re- Mer mel | Indicated V | Delta Marie Marie Cont. |    |

#### **FUNCTION TABLE**

|       | Inputs      | Outputs     |              |                  |
|-------|-------------|-------------|--------------|------------------|
| Reset | А           | В           | Q            | ā                |
| Н     | <u> </u>    | H /         | 7            | 7                |
| H     | Х           | L           |              | ggered<br>ggered |
| H     | L,H,∕∕<br>L | H<br>L,H,_/ |              | ggered<br>ggered |
| ~_    | ×           | X           | L<br>Not Tri | H<br>ggered      |

#### MAXIMUM RATINGS\*

| Symbol                  | Parameter                                                                                         | Value                        | Unit |
|-------------------------|---------------------------------------------------------------------------------------------------|------------------------------|------|
| Vcc                     | DC Supply Voltage (Referenced to GND)                                                             | -0.5 to $+7.0$               | V    |
| Vin                     | DC Input Voltage (Referenced to GND)                                                              | -1.5 to V <sub>CC</sub> +1.5 | V    |
| Vout                    | DC Output Voltage (Referenced to GND)                                                             | -0.5 to V <sub>CC</sub> +0.5 | V    |
| lin                     | DC Input Current, per Pin-A, B, Reset                                                             | ± 20                         | mA   |
| lin                     | DC Input Current, per Pin-C <sub>X</sub> /R <sub>X</sub>                                          | ±30                          | mA   |
| lout                    | DC Output Current, per Pin                                                                        | ± 25                         | mA   |
| Icc                     | DC Supply Current, VCC and GND Pins                                                               | ± 50                         | mA   |
| PD                      | Power Dissipation in Still Air, Plastic or Ceramic DIP1<br>SOIC Package1                          | 750<br>500                   | mW   |
| T <sub>stg</sub>        | Storage Temperature                                                                               | -65 to +150                  | °C   |
| SONC<br>SONC<br>CASE VI | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package)<br>(Ceramic DIP) | 260<br>300                   | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

| Symbol                            | Parameter                                      |                                                                               | Min  | Max                | Unit |
|-----------------------------------|------------------------------------------------|-------------------------------------------------------------------------------|------|--------------------|------|
| Vcc                               | DC Supply Voltage (Referenced to GN            | ID)                                                                           | 2.0  | 6.0                | ٧    |
| V <sub>in</sub> ,V <sub>out</sub> | DC Input Voltage, Output Voltage (Re           | ferenced to GND)                                                              | 0    | Vcc                | V    |
| TA                                | Operating Temperature, All Package T           | ypes                                                                          | - 55 | + 125              | °C   |
| t <sub>r</sub> , t <sub>f</sub>   | Input Rise and Fall Time — Reset<br>(Figure 5) | V <sub>CC</sub> = 2.0 V<br>V <sub>CC</sub> = 4.5 V<br>V <sub>CC</sub> = 6.0 V | 0 0  | 1000<br>500<br>400 | ns   |
| Gue G                             | A or B (Figure 5)                              |                                                                               | -    | no limit           |      |
| RX                                | External Timing Resistor                       | V <sub>CC</sub> < 4.5 V<br>V <sub>CC</sub> ≥ 4.5 V                            | 2.0  | *                  | kΩ   |
| CX                                | External Timing Capacitor                      |                                                                               | 0    | *                  | μF   |

\*The maximum allowable values of R<sub>X</sub> and C<sub>X</sub> are a function of the leakage of capacitor C<sub>X</sub>, the leakage of the HC4538, and leakage due to board layout and surface resistance. For most applications, C<sub>X</sub>/R<sub>X</sub> should be limited to a maximum value of 10  $\mu$ F/1 M $\Omega$ . Values of C<sub>X</sub>>1.0  $\mu$ F may cause a problem during power down (see Power-Down Considerations). Susceptibility to externally induced noise signals may occur for R<sub>X</sub>>1 M $\Omega$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions. †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

|        | Guaranteed Limit                                                   |                                                                                                                                                                      | V                 | Gua                | aranteed L         | imit               |      |
|--------|--------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|--------------------|--------------------|--------------------|------|
| Symbol | Parameter                                                          | Test Conditions                                                                                                                                                      | VCC               | 25°C to<br>-55°C   | ≤85°C              | ≤125°C             | Unit |
| VIH    | Minimum High-Level Input<br>Voltage                                | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \le 20 \mu\text{A}$                                                                               | 2.0<br>4.5<br>6.0 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V    |
| VIL    | Maximum Low-Level Input<br>Voltage                                 | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \le 20 \mu \text{A}$                                                                              | 2.0<br>4.5<br>6.0 | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | V    |
| Voн    | Minimum High-Level Output Voltage                                  | $V_{in} = V_{IH}$ or $V_{IL}$<br>$ I_{out}  \le 20 \mu A$                                                                                                            | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | ٧    |
|        | 80 120 120<br>16 20 24                                             | $V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$ $ I_{out}  \le 5.2 \text{ mA}$                                                                          | 4.5<br>6.0        | 3.98<br>5.48       | 3.84<br>5.34       | 3.70<br>5.20       |      |
| VOL    | Maximum Low-Level Output<br>Voltage                                | $V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$<br>$ I_{\text{out}}  \le 20 \ \mu\text{A}$                                                                 | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | V    |
|        | 400 400 400                                                        | $V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$<br>$ I_{out}  \le 5.2 \text{ mA}$                                                                       | 4.5<br>6.0        | 0.26<br>0.26       | 0.33<br>0.33       | 0.40<br>0.40       |      |
| lin    | Maximum Input Leakage Current (A, B, Reset)                        | V <sub>in</sub> = V <sub>CC</sub> or GND                                                                                                                             | 6.0               | ±0.1               | ± 1.0              | ±1.0               | μΑ   |
| lin    | Maximum Input Leakage Current (C <sub>X</sub> /R <sub>X</sub> )    | V <sub>in</sub> =V <sub>CC</sub> or GND                                                                                                                              | 6.0               | ± 50               | ± 500              | ± 500              | nA   |
| lcc    | Maximum Quiescent Supply<br>Current (per Package)<br>Standby State | $V_{in} = V_{CC}$ or GND Q1 and Q2 = Low $I_{out} = 0 \mu A$                                                                                                         | 6.0               | 130                | 220                | 350                | μΑ   |
| lcc    | Maximum Supply Current<br>(per Package)<br>Active State            | $\begin{array}{l} V_{in} = V_{CC} \text{ or GND} \\ \text{Q1 and Q2} = \text{High} \\ I_{out} = 0 \ \mu\text{A} \\ \text{Pins 2 and } 14 = 0.5 \ V_{CC} \end{array}$ | 6.0               | 150                | 250                | 400                | μΑ   |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### AC ELECTRICAL CHARACTERISTICS (C1 = 50 pF, Input tr = tf = 6 ns)

|                  |                                                                                      |                                                     |                   | Gua              | ranteed Li      | mit             |      |
|------------------|--------------------------------------------------------------------------------------|-----------------------------------------------------|-------------------|------------------|-----------------|-----------------|------|
| Symbol           | Parameter  Loupid of bound ad year X to solar ad                                     | erantiv <sub>ox</sub> Dydbl –                       | VCC               | 25°C to<br>-55°C | ≤85°C           | ≤125°C          | Unit |
| <sup>t</sup> PLH | Maximum Propagation Delay, Input A or B to Q (Figures 4 and 6)                       |                                                     | 2.0<br>4.5<br>6.0 | 250<br>50<br>43  | 315<br>63<br>54 | 375<br>75<br>64 | ns   |
| <sup>t</sup> PHL | Maximum Propagation Delay, Input A or B to $\overline{\mathbb{Q}}$ (Figures 4 and 6) |                                                     | 2.0<br>4.5<br>6.0 | 275<br>55<br>47  | 345<br>69<br>59 | 415<br>83<br>71 | ns   |
| <sup>t</sup> PHL | Maximum Propagation Delay, Reset to Q<br>(Figures 5 and 6)                           |                                                     | 2.0<br>4.5<br>6.0 | 250<br>50<br>43  | 315<br>63<br>54 | 375<br>75<br>64 | ns   |
| tPLH             | Maximum Propagation Delay, Reset to $\overline{\mathbb{Q}}$ (Figures 5 and 6)        |                                                     | 2.0<br>4.5<br>6.0 | 275<br>55<br>47  | 345<br>69<br>59 | 415<br>83<br>71 | ns   |
| tTLH,<br>tTHL    | Maximum Output Transition Time, Any Output<br>(Figures 5 and 6)                      |                                                     | 2.0<br>4.5<br>6.0 | 75<br>15<br>13   | 95<br>19<br>16  | 110<br>22<br>19 | ns   |
| Cin              | Maximum Input Capacitance                                                            | (A, B, Reset)<br>(C <sub>X</sub> , R <sub>X</sub> ) | Ξ                 | 10<br>25         | 10<br>25        | 10<br>25        | pF   |

# NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

| CPD | Power Dissipation Capacitance (Per Multivibrator)                                                                                                                    | Typical @ 25°C, V <sub>CC</sub> =5.0 V |    |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|----|
|     | Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2. | 150                                    | pF |

TIMING REQUIREMENTS (Input  $t_r = t_f = 6$  ns)

|                   | ricold      |             |             |           |                    |              | .,  | Guaranteed Limit |               |                |      |
|-------------------|-------------|-------------|-------------|-----------|--------------------|--------------|-----|------------------|---------------|----------------|------|
| Symbol            | 5*85F =     |             | Page Page   | ramete    | r = 0000(2%)       |              | VCC | 25°C to<br>-55°C | ≤85°C         | ≤125°C         | Unit |
| t <sub>rr</sub> * | Minimum Re  | trigger Tir | ne, Input A | or B      | V 1.0              | - ook to V 7 | 2.0 | _ ne             | of fine L-dpf | t (pu=loit))   | ns   |
|                   | (Figure 5)  |             |             |           |                    |              | 4.5 | -                | _             | aedlaV         |      |
|                   | 44          |             |             |           |                    |              | 6.0 | _                | _             | -              |      |
| t <sub>rec</sub>  | Minimum Re  | covery Tir  | ne, Reset I | nactive 1 | to A or B          | 33V to V.1   | 2.0 | 0                | 0.00          | 0              | ns   |
| 100               | (Figure 5)  |             |             |           |                    |              | 4.5 | 0                | 0             | 0              |      |
|                   | 1.2         |             |             |           |                    |              | 6.0 | 0                | 0             | 0              |      |
| tw                | Minimum Pu  | lse Width   | Input A o   | В         |                    | TiV to       | 2.0 | 80               | 100           | 120            | ns   |
|                   | (Figure 4)  |             | 1.3         |           |                    |              | 4.5 | 16               | 20            | 24             |      |
|                   | 8.8         |             |             |           |                    |              | 6.0 | 14               | 17            | 20             |      |
| tw                | Minimum Pu  | lse Width   | Reset       | 4.5       | Am G.A.z. Iron/I   | or Vir       | 2.0 | 80               | 100           | 120            | ns   |
|                   | (Figure 5)  |             |             |           |                    |              | 4.5 | 16               | 20            | 24             |      |
|                   | 1.0         |             |             |           |                    |              | 6.0 | 14               | 17            | 20             |      |
| tr, tf            | Maximum Inj | out Rise a  | nd Fall Tim | es, Rese  | et                 | Aud          | 2.0 | 1000             | 1000          | 1000           | ns   |
| 100               | (Figure 5)  |             |             |           |                    |              | 4.5 | 500              | 500           | 500            |      |
|                   | ds.0        | EE.0        |             |           |                    |              | 6.0 | 400              | 400           | 400            |      |
|                   | A or B      | 0.33        | 05.0        | 0.0       | Avn S. a.a. Incell |              | 2.0 |                  |               |                |      |
|                   | (Figure 5)  |             |             |           |                    |              | 4.5 | Consists I       | No Limit      | Level constant |      |
|                   | 77.2        |             |             |           |                    |              | 6.0 |                  |               | SHEET R ASS    |      |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

### OUTPUT PULSE WIDTH CHARACTERISTICS (CL = 50 pF)

|                | 5.0 190 280 466                                        | Conditions                                           |                                         | G an early a say |        | Temperature  |      |               |      | mal  |
|----------------|--------------------------------------------------------|------------------------------------------------------|-----------------------------------------|------------------|--------|--------------|------|---------------|------|------|
| Symbol         | Parameter                                              | Timing Components                                    | Vcc                                     | 25°C             |        | -40° to 85°C |      | -55° to 125°C |      | Unit |
|                |                                                        | Timing Components                                    | V                                       | Min              | Max    | Min          | Max  | Min           | Max  |      |
| τ              | Output Pulse Width* (Figures 4 and 6)                  | $R_X = 10 \text{ k}\Omega$ , $C_X = 0.1 \mu\text{F}$ | 5.0                                     | 0.63             | 0.77   | 0.60         | 0.80 | 0.59          | 0.81 | ms   |
| , <del>-</del> | Pulse Width Match Between Circuits in the Same Package | -and-u-d                                             | PLAN CHANAGE REFICE ICL - 80.0 . I- u I |                  | ASHITO | %            |      |               |      |      |
| -              | Pulse Width Match Variation (Part to Part)             | W                                                    | -                                       | 1000000          | 2000   |              | ± 10 |               |      | %    |

<sup>\*</sup>For output pulse widths greater than 100  $\mu$ s, typically  $\tau = kR\chi C\chi$ , where the value of k may be found in Figure 1.



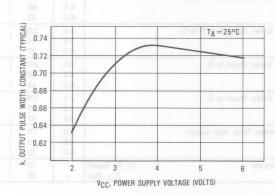


Figure 1. Typical Output Pulse Width Constant, k, versus Supply Voltage (For output pulse widths ≥100 μs: τ= kRχCχ)

<sup>\*</sup> $t_{rr}$  (ns)  $\approx 72 + \frac{V_{CC} \text{ (volts)} \cdot C_X \text{ (pF)}}{30.5}$ 

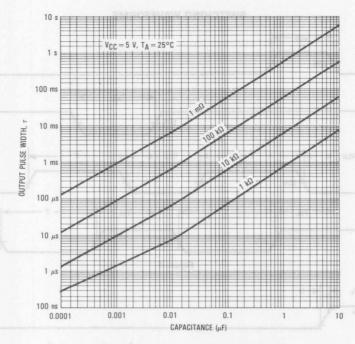


Figure 2. Output Pulse Width vs. Timing Capacitance

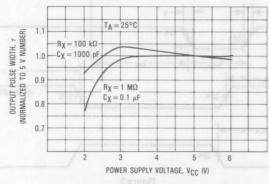
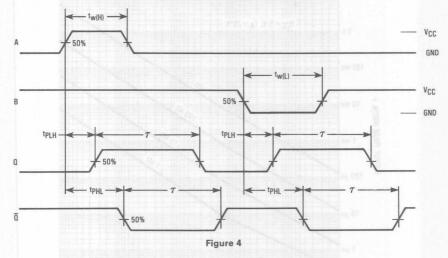
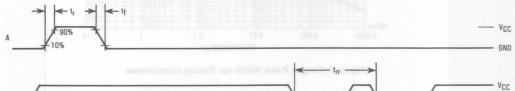


Figure 3. Normalized Output Pulse Width versus Power Supply Voltage







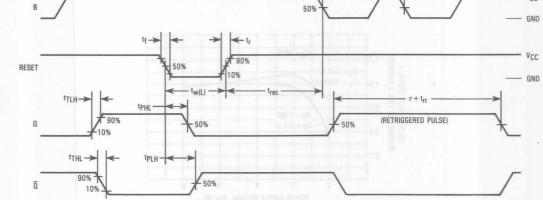
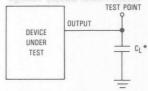


Figure 5



\*Includes all probe and jig capacitance.

Figure 6. Test Circuit

## INPUTS

A1, A2 (PINS 4, 12) — Positive-edge trigger inputs. A rising-edge signal on either of these pins triggers the corresponding multivibrator when there is a high level on the B1 or B2 input.

B1, B2 (PINS 5, 11) — Negative-edge trigger inputs. A falling-edge signal on either of these pins triggers the corresponding multivibrator when there is a low level on the A1 or A2 input.

**RESET 1, RESET 2 (PINS 3, 13)** — Reset inputs (active low). When a low level is applied to one of these pins, the  $\Omega$  output of the corresponding multivibrator is reset to a low level and the  $\overline{\Omega}$  output is set to a high level.

C<sub>X</sub>1/R<sub>X</sub>1 and C<sub>X</sub>2/R<sub>X</sub>2 (PINS 2 and 14) — External timing components. These pins are tied to the common points of the external timing resistors and capacitors (see the Block Diagram). Polystyrene capacitors are recommended for optimum

pulse width control. Electrolytic capacitors are not recommended due to high leakages associated with these type capacitors.

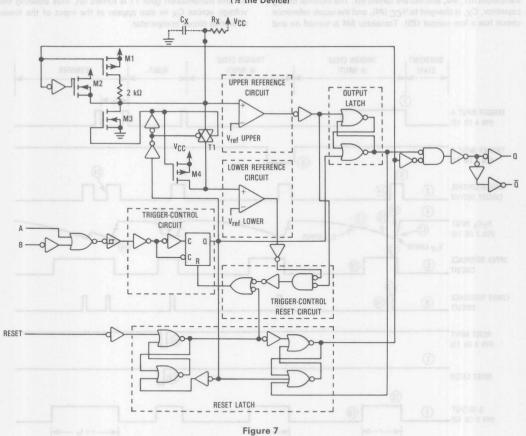
GND (PINS 1 and 15) — External ground. The external timing capacitors discharge to ground through these pins.

#### OUTPUTS

Q1, Q2 (PINS 6, 10) — Noninverted monostable outputs. These pins (normally low) pulse high when the multivibrator is triggered at either the A or the B input. The width of the pulse is determined by the external timing components, R<sub>X</sub> and C<sub>Y</sub>.

 $\overline{\text{O1}}$ ,  $\overline{\text{O2}}$  (PINS 7, 9) — Inverted monostable outputs. These pins (normally high) pulse low when the multivibrator is triggered at either the A or the B input. These outputs are the inverse of Q1 and Q2.

# LOGIC DETAIL



5

Figure 10 shows the HC4538 configured in the retriggerable mode. Briefly, the device operates as follows (refer to Figure 7): In the quiescent state, the external timing capacitor, Cx, is charged to VCC. When a trigger occurs, the Q output goes high and Cx discharges quickly to the lower reference voltage (Vref Lower  $\approx 1/3$  VCC). Cx then charges, through Rx, back up to the upper reference voltage (Vref Upper  $\approx 2/3$  VCC), at which point the one-shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the logic detail (Figure 7) and the timing diagram (Figure 8).

#### QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in Figure 8). Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, Figure 8).

The output of the trigger-control circuit is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor,  $C_{X}$ , is charged to  $V_{CC}$  (#4), and the upper reference circuit has a low output (#5). Transistor M4 is turned on and

transmission gate T1 is turned off. Thus the lower reference circuit has V<sub>CC</sub> at the noninverting input and a resulting low output (#6).

In addition, the output of the trigger-control reset circuit is low.

#### TRIGGER OPERATION

The HC4538 is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

The trigger-control circuit going high simultaneously initiates three events. First, the output latch goes low, thus taking the Q output of the HC4538 to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, C $\chi$ , to rapidly discharge toward ground (#11). (Note that the voltage across C $\chi$  appears at the input of the upper reference circuit comparator). Third, transistor M4 is turned off and transmission gate T1 is turned on, thus allowing the voltage across C $\chi$  to also appear at the input of the lower reference circuit comparator.

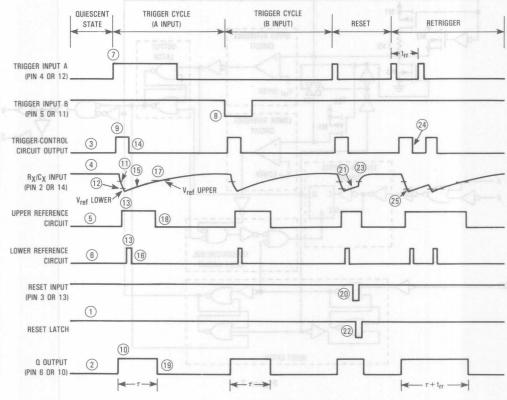


Figure 8. Timing Diagram

When C $\chi$  discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flip-flop to a low state (#14). This turns transistor M3 off again, allowing C $\chi$  to begin to charge back up toward V $_{CC}$ , with a time constant  $t=R\chi C\chi$  (#15). In addition, transistor M4 is turned on and transmission gate T1 is turned off. Thus a high voltage level is applied to the input of the lower reference circuit comparator, causing its output to go low (#16). The monostable multivibrator may be retriggered at any time after the trigger-control circuit goes low.

When  $C_X$  charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the HC4538 to a low state (#19), and completing the time-out cycle.

#### POWER-DOWN CONSIDERATIONS

Large values of C<sub>X</sub> may cause problems when powering down the HC4538 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V<sub>CC</sub> through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 30 mA; therefore, the turn-off time of the V<sub>CC</sub> power supply must not be faster than t = V<sub>CC</sub> •C<sub>X</sub>/(30 mA). For example, if V<sub>CC</sub> = 5 V and C<sub>X</sub> = 15  $\mu$ F, the V<sub>CC</sub> supply must turn off no faster than t = (5 V) • (15  $\mu$ F)/30 mA = 2.5 ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of  $V_{CC}$  to zero volts occurs, the HC4538 may sustain damage. To avoid this possibility, use an external damping diode,  $D_{X}$ , connected as shown in Figure 9. Best results can be achieved if diode  $D_{X}$  is chosen to be a germanium or Schottky type diode able to withstand large current surges.

#### RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the HC4538 to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while  $C_X$  is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus  $C_X$  is allowed to quickly charge up to  $V_{CC}$  (#23) to await the next trigger signal.

#### RETRIGGER OPERATION

When used in the retriggerable mode (Figure 10), the HC4538 may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24). Because the trigger-control circuit flip-flop resets shortly after  $C_X$  has discharged to the reference voltage of the lower reference circuit (#25), the minimum retrigger time,  $t_{rr}$  (Figure 5) is a function of internal propagation delays and the discharge time of  $C_X$ :

$$t_{rr}$$
 (ns)  $\cong$  72 +  $\frac{V_{CC}$  (volts)  $\cdot$  C $\chi$  (pF) , at room temperature

Figure 11 shows the device configured in the nonretriggerable mode.

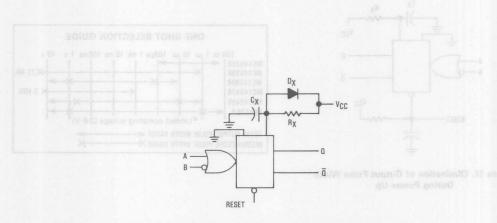


Figure 9. Discharge Protection During Power Down

# DO SHOW OVER OF DO V TO SEEMOND DIGGS OF TYPICAL APPLICATIONS

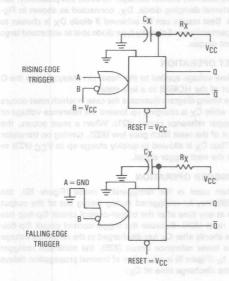


Figure 10. Retriggerable Monostable Circuitry

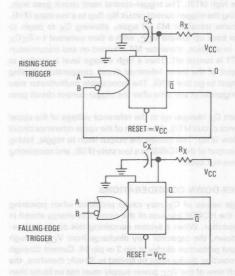


Figure 11. Nonretriggerable Monostable Circuitry

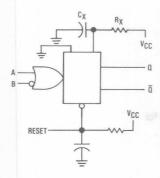
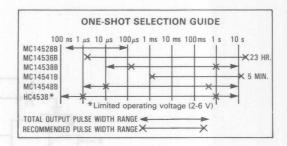


Figure 12. Elimination of Output Pulse Width During Power-Up

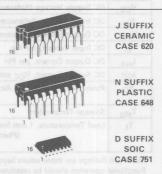


# MC54/74HC4543

# BCD-to-Seven-Segment Latch/ Decoder/Display Driver for LCDs High-Performance Silicon-Gate CMOS

The MC54/74HC4543 is compatible in both function and pinout with the MC14543B metal-gate CMOS decoder/driver. This device is designed for use with liquid-crystal display (LCD) readouts. The HC4543 provides a 4-bit storage latch, a BCD-to-seven-segment decoder, and an LCD driver. The blanking input (BI) and latch enable (LE, active low) are used to blank the display and store the BCD code, respectively. A square wave is applied to the phase input (Ph) of the HC4543 and electrically common backplane of the LCD.

- Latch Storage of BCD Inputs
- Blanking Input
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 252 FETs or 63 Equivalent Gates

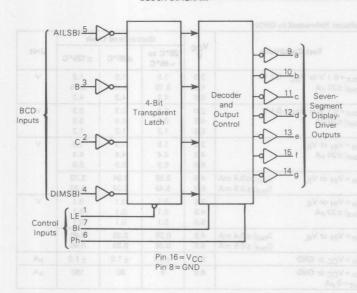


### ORDERING INFORMATION

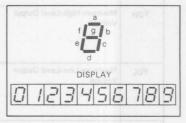
MC74HCXXXXN Plastic MC54HCXXXXJ Ceramic MC74HCXXXXD SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.





| LEC   | 1 • | 16 VCC        |
|-------|-----|---------------|
| CI    | 2   | 15 <b>1</b> f |
| В     | 3   | 14 <b>1</b> g |
| DI    | 4   | 13 <b>2</b> e |
| A     | 5   | 12 <b>3</b> d |
| Ph [  | 6   | 11 c          |
| BI    | 7   | 10 о в        |
| GND [ | 8   | 9 <b>1</b> a  |



F

| h   | r |            |  |
|-----|---|------------|--|
| -01 | ı |            |  |
|     | k | <b>a</b> ' |  |

| -                | I MANUAL I                                                                                        |                              |    |
|------------------|---------------------------------------------------------------------------------------------------|------------------------------|----|
| Vcc              | DC Supply Voltage (Referenced to GND)                                                             | -0.5 to +7.0                 | V  |
| Vin              | DC Input Voltage (Referenced to GND)                                                              | -1.5 to V <sub>CC</sub> +1.5 | ٧  |
| Vout             | DC Output Voltage (Referenced to GND)                                                             | -0.5 to V <sub>CC</sub> +0.5 | ٧  |
| lin              | DC Input Current, per Pin                                                                         | ±20                          | mA |
| lout             | DC Output Current, per Pin                                                                        | ± 25                         | mA |
| Icc              | DC Supply Current, V <sub>CC</sub> and GND Pins                                                   | ± 50                         | mA |
| PD               | Power Dissipation in Still Air, Plastic or Ceramic DIP†<br>SOIC Package†                          | 750<br>500                   | mW |
| T <sub>stg</sub> | Storage Temperature                                                                               | -65 to +150                  | °C |
| TL<br>SEUS O     | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package)<br>(Ceramic DIP) | 260<br>300                   | °C |

circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND  $\leq$  (V<sub>in</sub> or V<sub>out</sub>)  $\leq$  VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

| Symbol                            | Parameter                         |                          | Min  | Max   | Unit |
|-----------------------------------|-----------------------------------|--------------------------|------|-------|------|
| VCC                               | DC Supply Voltage (Referenced to  | GND)                     | 2.0  | 6.0   | V    |
| V <sub>in</sub> ,V <sub>out</sub> | DC Input Voltage, Output Voltage  | (Referenced to GND)      | 0    | Vcc   | V    |
| TA                                | Operating Temperature, All Packag | ge Types                 | - 55 | + 125 | °C   |
| t <sub>r</sub> , t <sub>f</sub>   | Input Rise and Fall Time          | V <sub>CC</sub> = 2.0 V  | 0    | 1000  | ns   |
|                                   | (Figure 3)                        | $V_{CC} = 4.5 \text{ V}$ | 0    | 500   |      |
|                                   | and the second second             | V <sub>CC</sub> = 6.0 V  | 0    | 400   |      |

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

|        | de Nee                                            |                                                                                                             |                                                                  |                   | Gua                | imit               |                    |      |
|--------|---------------------------------------------------|-------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------|-------------------|--------------------|--------------------|--------------------|------|
| Symbol | Parameter                                         | Test Conditions                                                                                             |                                                                  | VCC               | 25°C to<br>-55°C   | ≤85°C              | ≤125°C             | Unit |
| VIH    | Minimum High-Level Input<br>Voltage               | $V_{\text{out}} = 0.1 \text{ V or } V_{\text{CC}} = 0.1 \text{ V}$<br>$ I_{\text{out}}  \le 20 \mu\text{A}$ | 1 V                                                              | 2.0<br>4.5<br>6.0 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V    |
| VIL    | Maximum Low-Level Input<br>Voltage                | $V_{\text{out}} = 0.1 \text{ V or } V_{\text{CC}} = 0.1 \text{ V}$<br>$ I_{\text{out}}  \le 20 \mu\text{A}$ | 1 V Juque                                                        | 2.0<br>4.5<br>6.0 | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | Vac  |
| VOH    | Minimum High-Level Output<br>Voltage              | V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>  ≤20 μA                            | 3                                                                | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | V    |
|        | 100                                               |                                                                                                             | $ I_{out}  \le 0.4 \text{ mA}$<br>$ I_{out}  \le 0.5 \text{ mA}$ | 4.5<br>6.0        | 3.98<br>5.48       | 3.84<br>5.34       | 3.70<br>5.20       |      |
| VOL    | Maximum Low-Level Output<br>Voltage               | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \le 20 \mu A$                                            | T                                                                | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | V    |
| 1-41   | 20-18 18-1-215 [34]                               |                                                                                                             | $ I_{out}  \le 0.4 \text{ mA}$<br>$ I_{out}  \le 0.5 \text{ mA}$ | 4.5<br>6.0        | 0.26<br>0.26       | 0.33<br>0.33       | 0.40<br>0.40       |      |
| lin    | Maximum Input Leakage Current                     | Vin=VCC or GND                                                                                              |                                                                  | 6.0               | ±0.1               | ± 1.0              | ± 1.0              | μΑ   |
| Icc    | Maximum Quiescent Supply<br>Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA                                         |                                                                  | 6.0               | 8                  | 80                 | 160                | μΑ   |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

|               |                                                                            |                   | Gua               |                   |                   |      |
|---------------|----------------------------------------------------------------------------|-------------------|-------------------|-------------------|-------------------|------|
| Symbol        | Parameter                                                                  | VCC               | 25°C to<br>-55°C  | ≤85°C             | ≤125°C            | Unit |
| tPLH,<br>tPHL | Maximum Propagation Delay, Input A, B, C, or D to Output (Figures 1 and 5) | 2.0<br>4.5<br>6.0 | 600<br>120<br>102 | 750<br>150<br>130 | 900<br>180<br>153 | ns   |
| tPLH,<br>tPHL | Maximum Propagation Delay, LE to Output (Figures 2 and 5)                  | 2.0<br>4.5<br>6.0 | 600<br>120<br>102 | 750<br>150<br>130 | 900<br>180<br>153 | ns   |
| tPLH,<br>tPHL | Maximum Propagation Delay, BI or Ph to Output (Figures 3 and 5)            | 2.0<br>4.5<br>6.0 | 600<br>120<br>102 | 750<br>150<br>130 | 900<br>180<br>153 | ns   |
| tTLH,<br>tTHL | Maximum Output Transition Time, Any Output (Figures 3 and 5)               | 2.0<br>4.5<br>6.0 | 600<br>120<br>102 | 750<br>150<br>130 | 900<br>180<br>153 | ns   |
| Cin           | Maximum Input Capacitance                                                  | -                 | 10                | 10                | 10                | pF   |

## NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

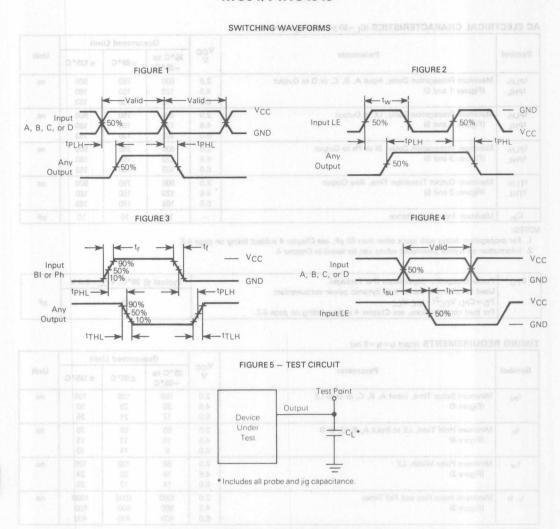
| CPD | Power Dissipation Capacitance (Per Package)                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Typical @ 25°C, V <sub>CC</sub> =5.0 V |    |
|-----|---------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|----|
|     | Used to determine the no-load dynamic power consumption:            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                        |    |
|     | PD = CPD VCC2f + ICC VCC                                            | Landa Companya Compan | 40                                     | pF |
|     | For load considerations, see Chapter 4 subject listing on page 4-2. |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 800 A                                  |    |

# TIMING RECUIREMENTS (Input t - tr-6 ns)

|                                 | PIGURES - TEST CIRCUIT                                   |               |                   | Gua                |                    |                    |    |
|---------------------------------|----------------------------------------------------------|---------------|-------------------|--------------------|--------------------|--------------------|----|
| Symbol                          | Parameter                                                | VCC           | 25°C to<br>-55°C  | ≤85°C              | ≤125°C             | Unit               |    |
| t <sub>su</sub>                 | Minimum Setup Time, Input A, B, C, or D to LE (Figure 4) | Davice        | 2.0<br>4.5<br>6.0 | 100<br>20<br>17    | 125<br>25<br>21    | 150<br>30<br>26    | ns |
| th                              | Minimum Hold Time, LE to Input A, B, C, or D (Figure 4)  | inbnQ<br>izeT | 2.0<br>4.5<br>6.0 | 50<br>10<br>9      | 65<br>13<br>11     | 75<br>15<br>13     | ns |
| t <sub>W</sub>                  | Minimum Pulse Width, LE (Figure 2)                       | ng Ra gabulan | 2.0<br>4.5<br>6.0 | 80<br>16<br>14     | 100<br>20<br>17    | 120<br>24<br>20    | ns |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times<br>(Figure 3)          |               | 2.0<br>4.5<br>6.0 | 1000<br>500<br>400 | 1000<br>500<br>400 | 1000<br>500<br>400 | ns |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

# MC54/74HC4543



|    |    | Inputs |   |   |   |   |   |   |    | ( | Out         | put | S |                        |
|----|----|--------|---|---|---|---|---|---|----|---|-------------|-----|---|------------------------|
| LE | ВІ | Ph*    | D | C | В | Α | а | b | С  | d | е           | f   | g | Display                |
| X  | Н  | L      | X | X | X | X | L | L | L  | L | L           | L   | L | Blank                  |
| Н  | L  | L      | L | L | L | L | Н | Н | Н  | Н | Н           | Н   | L | 0                      |
| H  | L  | L      | L | L | L | Н | L | H | H  | L | L           | L   | L | 1                      |
| Н  | L  | L      | L | L | H | L | Н | H | L  | H | H           | L   | H | 2                      |
| H  | L  | L      | L | L | Н | H | Н | H | H  | H | L           | L   | Н | 3                      |
| Н  | L  | L      | L | Н | L | L | L | H | Н  | L | L           | Н   | Н | 4                      |
| Н  | L  | L      | L | Н | L | H | Н | L | H  | H | L           | Н   | Н | 5                      |
| Н  | L  | L      | L | Н | H | L | Н | L | H  | H | Н           | H   | Н | 6                      |
| Н  | L  | L      | L | Н | Н | Н | H | Н | Н  | L | L           | L   | L | 7                      |
| Н  | L  | L      | Н | L | L | L | Н | Н | H  | Н | H           | H   | Н | 8                      |
| Н  | L  | L      | H | L | L | Н | H | Н | Н  | H | L           | Н   | H | 9                      |
| Н  | L  | L      | H | L | Н | L | L | L | L  | L | L           | L   | L | Blank                  |
| Н  | L  | L      | Н | L | Н | H | L | L | L  | L | L           | L   | L | Blank                  |
| Н  | L  | L      | Н | Н | L | L | L | L | L  | L | L           | L   | L | Blank                  |
| Н  | L  | L      | Н | Н | L | Н | L | L | L  | L | L           | L   | L | Blank                  |
| Н  | L  | L      | H | Н | H | L | L | L | L  | L | L           | L   | L | Blank                  |
| Н  | L  | L      | Н | H | H | H | L | L | L  | L | L           | L   | L | Blank                  |
| L  | L  | L      | X | X | X | X |   |   | 1  |   |             |     |   | ••                     |
| t  | t  | н      | 1 |   | t |   |   |   | om |   | Ou<br>ation |     | t | Display<br>as<br>above |

X = Don't care

t = Above Combinations

\* = For liquid crystal readouts, apply a square wave to Ph.

\*\* = Depends upon the code previously applied when LE = H

#### PIN DESCRIPTIONS

## INPUTS

A, B, C, D (PINS 5, 3, 2, 4) — BCD inputs. These are the inputs to be decoded. The data on these pins is decoded to a seven-segment output when the LE pin is high and is latched when LE is low. For inputs greater than hexadecimal 9 or for BI input high, the output is blanked. A (pin 5) is the least-significant data bit and D (pin 4) is the most-significant data bit.

### **OUTPUTS**

a, b, c, d, e, f, g (PINS 9, 10, 11, 12, 13, 15, 14) — Decoded seven-segment display-driver outputs. For liquid-crystal displays (LCD's), these outputs are tied directly to the LCD segment pins. For other type displays, see Figure 6.

#### CONTROL INPUTS

LE (PIN 1) — Latch Enable input (active-low). A falling-edge signal on this pin latches the code on the A, B, C, and D pins. The code remains latched until a rising-edge signal is applied to this pin. A high level on this pin allows the code to be transferred thru the latch to the decoder.

Ph (PIN 6) — Phase input. This input is used to invert the output level. For liquid-crystal displays (LCD), a square wave is applied to this input (typically 100 Hz) and to the common backplane of the LCD. For light-emitting diode (LED), incandescent, or gas-discharge displays, the phase input is tied to the appropriate level as shown in Figure 6.

BI (PIN 7) — Blanking input pin. A high level on this pin causes the outputs to follow the phase input, thereby blanking the display (no voltage drop across LCD segments).



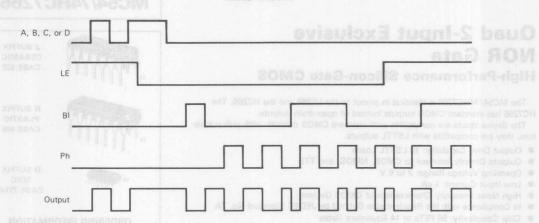
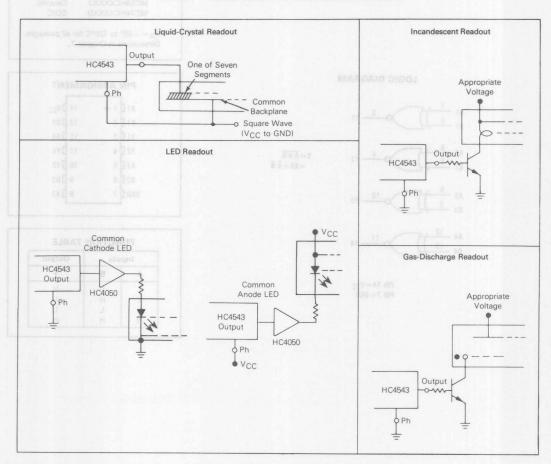


FIGURE 6 - CONNECTIONS TO VARIOUS DISPLAY READOUTS



The MC54/74HC7266 is identical in pinout to the LS266 and the HC266. The HC7266 has standard CMOS outputs instead of open-drain outputs.

The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 56 FETs or 14 Equivalent Gates

14

J SUFFIX CERAMIC CASE 632



N SUFFIX PLASTIC CASE 646



D SUFFIX SOIC CASE 751A

## ORDERING INFORMATION

..... 1/ TI IV/ 6UU

MC74HCXXXXN MC54HCXXXXJ MC74HCXXXXD

Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAM

PIN 14 = V<sub>CC</sub> PIN 7 = GND

#### PIN ASSIGNMENT

|       | 19.0 |    |                  |
|-------|------|----|------------------|
| A1 [  | 1 •  | 14 | o v <sub>C</sub> |
| B1 [  | 2    | 13 | B4               |
| Y1 [  | 3    | 12 | ] A4             |
| Y2 [  | 4    | 11 | ] Y4             |
| A2 [  | 5    | 10 | ] Y3             |
| B2 [  | 6    | 9  | <b>B</b> 3       |
| GND [ | 7    | 8  | 1 A3             |
|       |      |    | 1                |

# **FUNCTION TABLE**

| Inp | uts | Output |
|-----|-----|--------|
| Α   | В   | Υ      |
| L   | L   | Н      |
| L   | Н   | L      |
| H   | L   | L      |
| Н   | Н   | Н      |

 $Y = \overline{A \oplus B}$  $= AB + \overline{A} \overline{B}$ 

| Symbol           | finial bearage Parameter                                                                          | Value                        | Unit |
|------------------|---------------------------------------------------------------------------------------------------|------------------------------|------|
| Vcc              | DC Supply Voltage (Referenced to GND)                                                             | -0.5 to +7.0                 | V    |
| Vin              | DC Input Voltage (Referenced to GND)                                                              | -1.5 to V <sub>CC</sub> +1.5 | V    |
| Vout             | DC Output Voltage (Referenced to GND)                                                             | $-0.5$ to $V_{CC} + 0.5$     | V    |
| lin              | DC Input Current, per Pin                                                                         | ± 20                         | mA   |
| lout             | DC Output Current, per Pin                                                                        | ± 25                         | mA   |
| ICC              | DC Supply Current, V <sub>CC</sub> and GND Pins                                                   | ± 50                         | mA   |
| PD               | Power Dissipation in Still Air, Plastic or Ceramic DIP1<br>SOIC Package1                          | 750<br>500                   | mW   |
| T <sub>stg</sub> | Storage Temperature                                                                               | -65 to +150                  | °C   |
| TL               | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package)<br>(Ceramic DIP) | 260<br>300                   | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level

(e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

| Symbol                            | Parameter                               |                                                                               | Min | Max                | Unit |
|-----------------------------------|-----------------------------------------|-------------------------------------------------------------------------------|-----|--------------------|------|
| Vcc                               | DC Supply Voltage (Referenced to GND    | )                                                                             | 2.0 | 6.0                | V    |
| V <sub>in</sub> ,V <sub>out</sub> | DC Input Voltage, Output Voltage (Refer | renced to GND)                                                                | 0   | Vcc                | V    |
| TA                                | Operating Temperature, All Package Typ  | Operating Temperature, All Package Types                                      |     | + 125              | °C   |
| t <sub>r</sub> , t <sub>f</sub>   | Input Rise and Fall Time<br>(Figure 1)  | V <sub>CC</sub> = 2.0 V<br>V <sub>CC</sub> = 4.5 V<br>V <sub>CC</sub> = 6.0 V | 0 0 | 1000<br>500<br>400 | ns   |

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

|        |                                                   |                                                                            |                                                                                |                   | Gua                | imit               |                    |    |
|--------|---------------------------------------------------|----------------------------------------------------------------------------|--------------------------------------------------------------------------------|-------------------|--------------------|--------------------|--------------------|----|
| Symbol | Parameter Test Conditions                         |                                                                            | V <sub>CC</sub>                                                                | 25°C to<br>-55°C  | ≤85°C              | ≤125°C             | Unit               |    |
| VIH    | Minimum High-Level Input<br>Voltage               | V <sub>out</sub> =0.1 V or V <sub>CC</sub><br> I <sub>out</sub>   ≤20 μA   | -0.1 V                                                                         | 2.0<br>4.5<br>6.0 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V  |
| VIL    | Maximum Low-Level Input<br>Voltage                | V <sub>out</sub> = 0.1 V or V <sub>CC</sub><br> I <sub>out</sub>   ≤ 20 μA | -0.1 V                                                                         | 2.0<br>4.5<br>6.0 | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | V  |
| VOH    | Minimum High-Level Output<br>Voltage              | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \le 20 \mu A$           |                                                                                | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | ٧  |
|        | 1-0                                               | Vin=VIH or VIL                                                             | I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA                    | 4.5<br>6.0        | 3.98<br>5.48       | 3.84<br>5.34       | 3.70<br>5.20       |    |
| VOL    | Maximum Low-Level Output<br>Voltage               | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \le 20 \mu A$           |                                                                                | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | V  |
|        |                                                   | Vin=VIH or VIL                                                             | $ I_{\text{out}}  \le 4.0 \text{ mA}$<br>$ I_{\text{out}}  \le 5.2 \text{ mA}$ | 4.5<br>6.0        | 0.26<br>0.26       | 0.33<br>0.33       | 0.40<br>0.40       |    |
| lin    | Maximum Input Leakage Current                     | Vin=VCC or GND                                                             |                                                                                | 6.0               | ± 0.1              | ±1.0               | ±1.0               | μΑ |
| Icc    | Maximum Quiescent Supply<br>Current (per Package) | $V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$                               |                                                                                | 6.0               | 2                  | 20                 | 40                 | μΑ |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

| Symbol        | Vals clevios contiens                                |                              |           | Gua               | Symbo            |                 |                 |      |
|---------------|------------------------------------------------------|------------------------------|-----------|-------------------|------------------|-----------------|-----------------|------|
|               | display or yeard again<br>due to high static voltage | Parameter                    |           | VCC               | 25°C to<br>-55°C | ≤85°C           | ≤125°C          | Unit |
| tPLH,<br>tPHL | Maximum Propagation Dela<br>(Figures 1 and 2)        | ay, Input A or B to Output Y |           | 2.0<br>4.5<br>6.0 | 120<br>24<br>20  | 150<br>30<br>26 | 180<br>36<br>31 | ns   |
| tTLH,<br>tTHL | Maximum Output Transitio<br>(Figures 1 and 2)        | n Time, Any Output           | 1980 pine | 2.0<br>4.5<br>6.0 | 75<br>15<br>13   | 95<br>19<br>16  | 110<br>22<br>19 | ns   |
| Cin           | Maximum Input Capacitano                             | ce Date                      | Tegs/359  | 0.08              | 10               | 10              | 10              | pF   |

#### NOTES

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

| CPD | Power Dissipation Capacitance (Per Gate)                            | Typical @ 25°C, V <sub>CC</sub> =5.0 V           | northern. |
|-----|---------------------------------------------------------------------|--------------------------------------------------|-----------|
|     | Used to determine the no-load dynamic power consumption:            | as 600 years developed by a second as useful as  | miero.    |
|     | PD = CPD VCC <sup>2</sup> f + ICC VCC                               | 33                                               | pF        |
|     | For load considerations, see Chapter 4 subject listing on page 4-2. | a COSt and and Cold Glasses Common and Cold Cold |           |

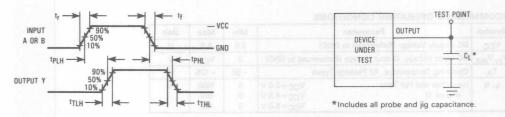
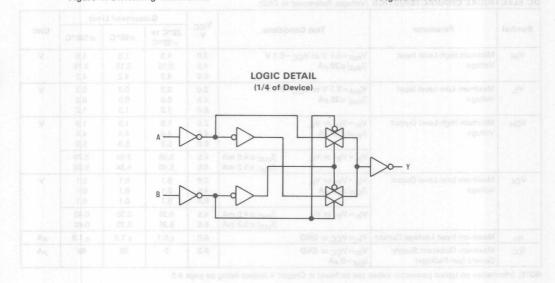


Figure 1. Switching Waveforms

Figure 2. Test Circuit



#### APPLICATION INFORMATION

Bi  $\phi$ -L is defined as biphase-level code. Also known as Manchester Code, this technique utilizes binary phase shift keying (PSK). The Bi  $\phi$ -L output shown in Figure 3 carries both data and synchronization information; therefore, separate data and clock lines are not required to transfer information. A positive-going transition in the middle of the bit interval

indicates a logic zero; a negative-going transition indicates a logic one (see Figure 4).

NRZ-L shown in Figure 3 is non-return-to-zero level code. This is simply serial data out of a shift register, such as the HC597.

The Bi  $\phi$ -L signal must be phase coherent (i.e., no glitches). Therefore, NRZ-L and clock transitions must be coincident.

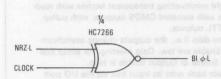


Figure 3. Biphase-Level Encoder (Manchester Encoder)

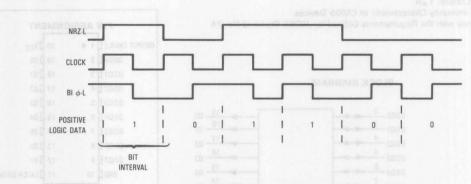


Figure 4. Timing Diagram

# **Octal 3-State Noninverting Transparent Latch with** Readback

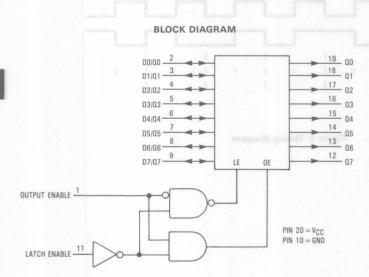
# **High-Performance Silicon-Gate CMOS**

The MC54/74HC7793 consists of eight noninverting transparent latches with readback. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable and Output Enable are low. Data meeting the setup and hold time is latched when either Latch Enable or Output Enable is high.

The HC7793 can enable its output data back onto its input bus via the I/O port configuration. Output Enable and Latch Enable determine how pins D0/Q0-D7/Q7 are configured. When Output Enable is high and Latch Enable is low, the outputs of the latches are enabled on D0/Q0-D7/Q7, configuring D0/Q0-D7/Q7 as an output bus so that the output data can be read back by the host.

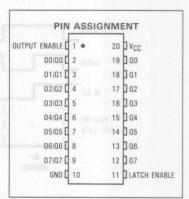
- Output Drive Capability: 10 LSTTL Loads (Q0-Q7) 15 LSTTL Loads (D0/Q0-D7/Q7)
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A





MC54HCXXXXJ Ceramic MC74HCXXXXDW SOIC

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.



#### **FUNCTION TABLE**

|                  | Inputs          |        | Outpu | uts |
|------------------|-----------------|--------|-------|-----|
| Output<br>Enable | Latch<br>Enable | D/Q    | D/Q   | Q   |
| L                | L               | L      | Input | L   |
| L                | L               | Н      | Input | Н   |
| L                | Н               | X      | Input | 0*  |
| Н                | L               | Output | Q*    | Q*  |
| Н                | Н               | X      | Input | 0*  |

\*Q represents the previous latched state.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

|                  |                                                                                                   |                              | _    |
|------------------|---------------------------------------------------------------------------------------------------|------------------------------|------|
| Symbol           | Parameter                                                                                         | Value                        | Unit |
| Vcc              | DC Supply Voltage (Referenced to GND)                                                             | -0.5 to $+7.0$               | V    |
| Vin              | DC Input Voltage (Referenced to GND)                                                              | -1.5 to V <sub>CC</sub> +1.5 | V    |
| Vout             | DC Input Voltage (Referenced to GND)                                                              | -0.5 to V <sub>CC</sub> +0.5 | V    |
| lin              | DC Input Current, per Pin (Pins 1, 11)                                                            | ± 20                         | mA   |
| lout             | DC Output Current, per Pin (Pins 12-19)                                                           | ± 25                         | mA   |
| 1/0              | DC Output Current, per Pin (Pins 2-9)                                                             | ± 35                         | mA   |
| Icc              | DC Supply Current, VCC and GND Pins                                                               | ± 75                         | mA   |
| PD               | Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†                             | 750<br>500                   | mW   |
| T <sub>stg</sub> | Storage Temperature                                                                               | -65 to +150                  | °C   |
| TL               | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package)<br>(Ceramic DIP) | 260<br>300                   | °C   |

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

| Symbol                            | Parameter                                                                                     |                                                       | Min  | Max        | Unit |
|-----------------------------------|-----------------------------------------------------------------------------------------------|-------------------------------------------------------|------|------------|------|
| Vcc                               | DC Supply Voltage (Referenced to GND)                                                         |                                                       | 2.0  | 6.0        | V    |
| V <sub>in</sub> ,V <sub>out</sub> | DC Input Voltage, Output Voltage (Referenced to GND) Operating Temperature, All Package Types |                                                       | 0    | Vcc        | V    |
| TA                                |                                                                                               |                                                       | - 55 | + 125      | °C   |
| t <sub>r</sub> , t <sub>f</sub>   | Input Rise and Fall Time                                                                      | V <sub>CC</sub> =2.0 V                                | 0    | 1000       | ns   |
|                                   | (Figure 1)                                                                                    | $V_{CC} = 4.5 \text{ V} $<br>$V_{CC} = 6.0 \text{ V}$ | 0    | 500<br>400 |      |

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol                     |                                                   | Test Conditions                                                                         |                                                                                | V <sub>CC</sub>   | Guaranteed Limit   |                    |                    | -    |
|----------------------------|---------------------------------------------------|-----------------------------------------------------------------------------------------|--------------------------------------------------------------------------------|-------------------|--------------------|--------------------|--------------------|------|
|                            | Parameter                                         |                                                                                         |                                                                                |                   | 25°C to<br>-55°C   | ≤85°C              | ≤125°C             | Unit |
| VIH                        | Minimum High-Level Input<br>Voltage               | V <sub>out</sub> =0.1 V or V <sub>CC</sub> −<br> I <sub>out</sub>   ≤20 μA              | 0.1 V                                                                          | 2.0<br>4.5<br>6.0 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V    |
| VIL                        | Maximum Low-Level Input<br>Voltage                | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \le 20 \mu \text{A}$ |                                                                                | 2.0<br>4.5<br>6.0 | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | V    |
| Vон                        | Minimum High-Level Output<br>Voltage              | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \le 20 \ \mu\text{A}$                | east t                                                                         | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | V    |
| en                         | 1000 1000 1000<br>800 800 800                     | V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub><br>Pins 2-9                         | $ I_{out}  \le 6.0 \text{ mA}$<br>$ I_{out}  \le 7.8 \text{ mA}$               | 4.5<br>6.0        | 3.98<br>5.48       | 3.84<br>5.34       | 3.70<br>5.20       |      |
|                            | 009 000 008                                       | V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub><br>Pins 12-19                       | $ I_{\text{out}}  \le 4.0 \text{ mA}$<br>$ I_{\text{out}}  \le 5.2 \text{ mA}$ | 4.5<br>6.0        | 3.98<br>5.48       | 3.84<br>5.34       | 3.70<br>5.20       |      |
| VOL Maximum Low<br>Voltage | Maximum Low-Level Output<br>Voltage               | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \le 20 \ \mu\text{A}$                |                                                                                | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | V    |
|                            |                                                   | V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub><br>Pins 2-9                         | $ I_{out}  \le 6.0 \text{ mA}$<br>$ I_{out}  \le 7.8 \text{ mA}$               | 4.5<br>6.0        | 0.26<br>0.26       | 0.33<br>0.33       | 0.40<br>0.40       |      |
|                            |                                                   | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>Pins 12-19                      | $ I_{out}  \le 4.0 \text{ mA}$<br>$ I_{out}  \le 5.2 \text{ mA}$               | 4.5<br>6.0        | 0.26<br>0.26       | 0.33<br>0.33       | 0.40<br>0.40       |      |
| lin                        | Maximum Input Leakage Current                     | Vin=VCC or GND                                                                          |                                                                                | 6.0               | ±0.1               | ±1.0               | ±1.0               | μΑ   |
| loz                        | Maximum Three-State Leakage<br>Current            | Output in High-Impedance State  Vin = VIL or VIH  Vout = VCC or GND                     |                                                                                | 6.0               | ±0.5               | ±5.0               | ±10.0              | μΑ   |
| Icc                        | Maximum Quiescent Supply<br>Current (per Package) | V <sub>in</sub> =V <sub>CC</sub> or GND<br>I <sub>out</sub> =0 μA                       |                                                                                | 6.0               | 8                  | 80                 | 160                | μΑ   |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$  VCC.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

Functional operation should be restricted to the Recommended Operating Conditions.

<sup>†</sup>Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

AC ELECTRICAL CHARACTERISTICS ( $C_1 = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

| Symbol               | apitatos solvida adT inti eu                      | 107                    | Guaranteed Limit |          |          | ledmy  |
|----------------------|---------------------------------------------------|------------------------|------------------|----------|----------|--------|
|                      | Parameter 0.7 L of 8.04                           | V                      | 25°C to<br>-55°C | ≤85°C    | ≤125°C   | Unit   |
| tPLH,                | Maximum Propagation Delay, Input Data to Q        | 0.0- 2.0               | 150              | 190      | 225      | ns     |
| tPHL                 | (Figures 1 and 5)                                 | 4.5<br>6.0             | 30<br>26         | 38<br>33 | 45<br>38 |        |
| tPLH,                | Maximum Propagation Delay, Latch Enable or Output | it Enable to Q 2.0     | 175              | 220      | 265      | ns     |
| tPHL                 | (Figures 2 and 5)                                 | 4.5                    | 35               | 44       | 53       |        |
| V) = UM              | 28 niA constrained to the range O                 | 6.0                    | 30               | 37       | 45       | 100    |
| tpLZ, Maximum Propag | Maximum Propagation Delay, Latch Enable or Output | it Enable to 2.0       | 150              | 190      | 225      | ns     |
| tPHZ                 | D0/Q0-D7/Q7                                       | 4.5                    | 30               | 38       | 45       |        |
| egus, ravi           | (Figures 3 and 6)                                 | 6.0                    | 26               | 33       | 38       | T area |
| tPZL,                | Maximum Propagation Delay, Latch Enable or Output | it Enable to 2.0       | 150              | 190      | 225      | ns     |
| tPZH                 | D0/Q0-D7/Q7                                       | 4.5                    | 30               | 38       | 45       |        |
|                      | (Figures 3 and 6)                                 | (910) simus 6.0        | 26               | 33       | 38       |        |
| tTLH,                | Maximum Output Transition Time, D0/Q0-D7/Q7       | 2.0                    | 60               | 75       | 90       | ns     |
| tTHL                 | nesinded Operating Conditions.                    | O primaryO beamana 4.5 | 12               | 15       | 18       |        |
|                      |                                                   | 6.0                    | 10               | 13       | 15       | gnuare |
| tTLH,                | Maximum Output Transition Time. Q0-Q7             | 2.0                    | 75               | 95       | 110      | ns     |
| THL                  | (Figures 1 and 5)                                 | 4.5                    | 15               | 19       | 22       |        |
|                      |                                                   | 6.0                    | 13               | 16       | 19       | dant n |
| Cin                  | Maximum Input Capacitance (Pins 1, 11)            | \$17011                | 10               | 10       | 10       | pF     |
| Cout                 | Maximum I/O Capacitance (I/O in High-Impedance    | State) -               | 15               | 15       | 15       | o pFy  |

#### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2. How might be approved to the control of the

2. Information on typical parametric values can be found in Chapter 4.

| CPD | Power Dissipation Capacitance (Per Latch)                                                                    | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |    |
|-----|--------------------------------------------------------------------------------------------------------------|-----------------------------------------|----|
|     | Used to determine the no-load dynamic power consumption:                                                     | TOO                                     | -  |
|     | PD = CPD VCC <sup>2</sup> f + ICC VCC<br>For load considerations, see Chapter 4 subject listing on page 4-2. | MICAT CHY (ALL MICE AND TADIN           | pF |

## TIMING REQUIREMENTS (Input t, = tf = 6 ns)

| Symbol                          | 8.1 8.1 8.1 8.8 V1.0-33V to V1.0-32V to V1 |                   | Guaranteed Limit   |                    |                    | HELV |
|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|--------------------|--------------------|--------------------|------|
|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | VCC               | 25°C to<br>-55°C   | ≤85°C              | ≤125°C             | Unit |
| t <sub>su</sub>                 | Minimum Setup Time, Input Data to Latch Enable (Figure 4)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 2.0<br>4.5<br>6.0 | 100<br>20<br>17    | 125<br>25<br>21    | 150<br>30<br>26    | ns   |
| th                              | Minimum Hold Time, Latch Enable to Input Data<br>(Figure 4)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 2.0<br>4.5<br>6.0 | 5<br>5<br>5        | 5<br>5<br>5        | 5<br>5<br>5        | ns   |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times<br>(Figure 1)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 2.0<br>4.5<br>6.0 | 1000<br>500<br>400 | 1000<br>500<br>400 | 1000<br>500<br>400 | ns   |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

# **SWITCHING WAVEFORMS**

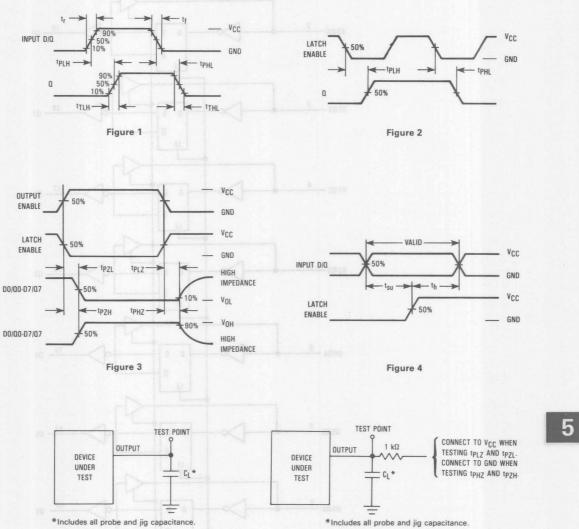
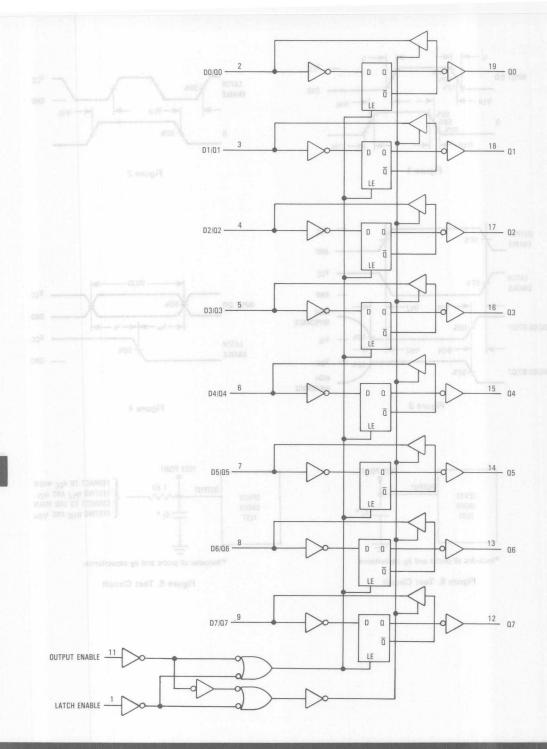


Figure 6. Test Circuit

Figure 5. Test Circuit





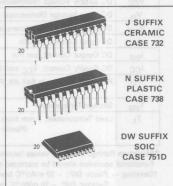
# Product Preview

# Programmable Timer High-Performance Silicon-Gate CMOS

The MC54/74HC9000 is a precision programmable timer that, when used in conjunction with a 32 kHz to 20 MHz crystal, can provide time durations from 4.2 minutes to 100 ns. Using the on-chip oscillator function and external RC components, even longer time durations can be obtained. Both true and complementary outputs are available for use with the edge-sensitive oscillator control and count control. These control pins facilitate several timer and "one-shot" type configurations (see Application Information).

- Has On-Chip Crystal or RC Oscillator Capability; or may be Driven by External Frequency Source
- More Accurate than Monostable Multivibrators when used with a Crystal
- Low Power Consumption Characteristic of CMOS Devices
- Wide Operating Voltage Range: 2.5 to 6 Volts
- OUT and OUT Drive Capability: 10 LSTTL Loads
- High Noise Immunity Characteristics of CMOS Devices
- Very Low Power Consumption in Standby Mode
- Double Diode Protection on all Inputs
- Divide Range of 2 to 224
- Select Inputs (S0, S1, S2, S3, S4) Facilitate Programming and Incoming Inspection
- Mode Inputs (M0, M1, M2) for Functional Versatility
- Chip Complexity: 923 FETs or 231 Equivalent Gates

# MC54/74HC9000



#### ORDERING INFORMATION

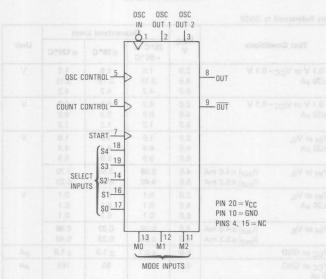
| MC74HCXXXXN  | Plastic |
|--------------|---------|
| MC54HCXXXXJ  | Ceramic |
| MC74HCXXXXDW | SOIC    |

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### PIN ASSIGNMENT OSC IN [ 1 . 20 7 VCC 19 S3 OSC OUT 2 13 18 3 S4 NC 04 17 D SO OSC CONTROL 5 16 3 S1 COUNT CONTROL 6 15 NC START D 14 D S2 13 MO OUT 6 OUT de 12 M1 11 M2 GND 0 10

NC = NO CONNECTION

#### LOGIC DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

#### MAXIMUM RATINGS\*

| Symbol                   | Parameter                                                                                         | Value                        | Unit |
|--------------------------|---------------------------------------------------------------------------------------------------|------------------------------|------|
| Vcc                      | DC Supply Voltage (Referenced to GND)                                                             | -0.5 to +7.0                 | V    |
| Vin                      | DC Input Voltage (Referenced to GND)                                                              | -1.5 to V <sub>CC</sub> +1.5 | V    |
| Vout                     | DC Output Voltage (Referenced to GND)                                                             | -0.5 to V <sub>CC</sub> +0.5 | V    |
| lin                      | DC Input Current, per Pin                                                                         | ± 20                         | mA   |
| lout                     | DC Output Current, per Pin                                                                        | ± 25                         | mA   |
| Icc                      | DC Supply Current, V <sub>CC</sub> and GND Pins                                                   | ± 50                         | mA   |
| PD                       | Power Dissipation in Still Air, Plastic or Ceramic DIP1<br>SOIC Package1                          | 750<br>500                   | mW   |
| T <sub>stg</sub>         | Storage Temperature                                                                               | -65 to +150                  | °C   |
| T <sub>L</sub><br>Bua Wa | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package)<br>(Ceramic DIP) | 260<br>300                   | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

| Symbol                            | Parameter                                    | Min                                 | Max         | Unit               |    |
|-----------------------------------|----------------------------------------------|-------------------------------------|-------------|--------------------|----|
| Vcc                               | DC Supply Voltage (Referenced to GND)        |                                     | 2.5*        | 6.0                | V  |
| V <sub>in</sub> ,V <sub>out</sub> | DC Input Voltage, Output Voltage (Referenced | 0                                   | Vcc         | V                  |    |
| TA                                | Operating Temperature, All Package Types     | STREET, STREET                      | - 55        | + 125              | °C |
| t <sub>r</sub> , t <sub>f</sub>   | Except OSC IN and START Vo                   | C = 2.0 V<br>C = 4.5 V<br>C = 6.0 V | 0<br>0<br>0 | 1000<br>500<br>400 | ns |
|                                   | Input Rise and Fall Time (OSC IN o           | 0                                   | No<br>Limit |                    |    |

<sup>\*</sup>The oscillator is guaranteed to function at 2.5 V minimum. However, parametrics are tested at 2.0 V by driving Pin 1 with an external clock source.

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

|        | ST 30Kellin nee at                                |                                                                                  |                                                                                | V                  | Gua                | imit               |                   |    |
|--------|---------------------------------------------------|----------------------------------------------------------------------------------|--------------------------------------------------------------------------------|--------------------|--------------------|--------------------|-------------------|----|
| Symbol | Parameter                                         | Test Cor                                                                         | VCC                                                                            | 25°C to<br>-55°C   | ≤85°C              | ≤125°C             | Uni               |    |
| VIH    | Minimum High-Level Input<br>Voltage               | V <sub>out</sub> =0.1 V or V <sub>CC</sub><br> I <sub>out</sub>   ≤20 μA         | 2.0<br>4.5<br>6.0                                                              | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V                 |    |
| VIL    | Maximum Low-Level Input<br>Voltage                | V <sub>out</sub> =0.1 V or V <sub>CC</sub><br> I <sub>out</sub>  ≤20 μA          | 2.0<br>4.5<br>6.0                                                              | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | V                 |    |
| VOH    | Minimum High-Level Output<br>Voltage (OUT, OUT)   | V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>  ≤20 μA |                                                                                | 2.0<br>4.5<br>6.0  | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9 | V  |
|        |                                                   | Vin=VIH or VIL                                                                   | $ I_{out}  \le 4.0 \text{ mA}$<br>$ I_{out}  \le 5.2 \text{ mA}$               | 4.5<br>6.0         | 3.98<br>5.48       | 3.84<br>5.34       | 3.70<br>5.20      |    |
| VOL    | Maximum Low-Level Output<br>Voltage (OUT, OUT)    | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \le 20 \mu A$                 | 30X = 01 MH                                                                    | 2.0<br>4.5<br>6.0  | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1 | V  |
|        |                                                   | Vin=VIH or VIL                                                                   | $ I_{\text{out}}  \le 4.0 \text{ mA}$<br>$ I_{\text{out}}  \le 5.2 \text{ mA}$ | 4.5<br>6.0         | 0.26<br>0.26       | 0.33<br>0.33       | 0.40<br>0.40      |    |
| lin    | Maximum Input Leakage Current                     | Vin=VCC or GND                                                                   |                                                                                | 6.0                | ±0.1               | ± 1.0              | ±1.0              | μΑ |
| Icc    | Maximum Quiescent Supply<br>Current (per Package) | $V_{in} = V_{CC}$ or GND.<br>$I_{out} = 0 \mu A$                                 |                                                                                | 6.0                | 8                  | 80                 | 160               | μА |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

#### MC54/74HC9000

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input  $t_f = t_f = 6 \text{ ns}$ )

|                  | District Avillen delin by one or me seemen of the                                      |                                     |                   | Pr                |                   |                   |      |
|------------------|----------------------------------------------------------------------------------------|-------------------------------------|-------------------|-------------------|-------------------|-------------------|------|
| Symbol           | Parameter                                                                              | nspanenta,                          | V <sub>CC</sub>   | 25°C to<br>-55°C  | ≤85°C             | ≤125°C            | Unit |
| fmax             | Maximum Clock Frequency (Modes 1-7) (50% Duty Cycle) (Figures 1 and 2)                 | edi perma<br>permentipe<br>permanal | 2.0<br>4.5<br>6.0 | 4.0<br>20<br>24   | 3.2<br>16<br>19   | 2.6<br>13<br>15   | MHz  |
| f <sub>max</sub> | Maximum Clock Frequency (Mode 0) (50% Duty Cycle) (Figures 1 and 2)                    | and should<br>2 must be             | 2.0<br>4.5<br>6.0 | 2.0<br>10<br>11.8 | 1.6<br>8.0<br>9.4 | 1.3<br>6.7<br>7.9 | MHz  |
| tPLH,<br>tPHL    | Maximum Propagation Delay, OSC IN to OUT or OUT (One Stage Selected) (Figures 1 and 2) | -nego fiet                          | 2.0<br>4.5<br>6.0 | 250<br>50<br>43   | 315<br>63<br>54   | 375<br>75<br>64   | ns   |
| tPLH,<br>tPHL    | Maximum Propagation Delay, START to OUT or OUT (One Shot Mode) (Figures 3 and 2)       | not A low-                          | 2.0<br>4.5<br>6.0 | 250<br>50<br>43   | 315<br>63<br>54   | 375<br>75<br>64   | ns   |
| tTLH,<br>tTHL    | Maximum Output Transition Time, Any Output (Figures 1 and 2)                           | nurs stun<br>er stundby             | 2.0<br>4.5<br>6.0 | 75<br>15<br>13    | 95<br>19<br>16    | 110<br>22<br>19   | ns   |
| Cin              | Maximum Input Capacitance                                                              |                                     | -                 | 10                | 10                | 10.               | pF   |

#### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2. In 1987, and the propagation on typical parametric values can be found in Chapter 4.

| CPD | Power Dissipation Capacitance (Per Package)                                                   | Typical @ 25°C, V <sub>CC</sub> =5.0 V |           |
|-----|-----------------------------------------------------------------------------------------------|----------------------------------------|-----------|
|     | Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC | TBD                                    | pF        |
|     | For load considerations, see Chapter 4 subject listing on page 4-2.                           | aut salates aid aut un unterant us.    | M-WEGIL / |

#### TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            | Projected Limit  |          |          |      |  |
|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------------------|----------|----------|------|--|
| Symbol                          | Parameter polymeter who M sugged . I                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | VCC        | 25°C to<br>-55°C | ≤85°C    | ≤125°C   | Unit |  |
| t <sub>su</sub>                 | Minimum Setup Time, S0-S4 or M0-M2 to START                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 2.0        | 100              | 125      | 150      | ns   |  |
|                                 | (Figure 3)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 4.5<br>6.0 | 20<br>17         | 25<br>21 | 30<br>26 |      |  |
| td                              | Minimum Delay Time, START to OUT or OUT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 2.0        | 500              | 625      | 750      | ns   |  |
|                                 | (Figure 3)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 4.5        | 100              | 125      | 150      |      |  |
|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 6.0        | 85               | 106      | 128      |      |  |
| tb                              | Minimum Burst Time, Count Control                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 2.0        | 500              | 625      | 750      | ns   |  |
|                                 | (Figure 3) magnification and address                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 4.5        | 100              | 125      | 150      |      |  |
|                                 | At the state of th | 6.0        | 85               | 106      | 128      |      |  |
| tw                              | Minimum Pulse Width, START                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 2.0        | 80               | 100      | 120      | ns   |  |
|                                 | (Figure 3)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 4.5        | 16               | 20       | 24       |      |  |
|                                 | entid fatter (150 = 347) texten = Trainer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 6.0        | 14               | 17       | 20       |      |  |
| tw                              | Minimum Pulse Width, OSC IN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 2.0        | 80               | 100      | 120      | ns   |  |
|                                 | (Figure 1)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 4.5        | 16               | 20       | 24       |      |  |
|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 6.0        | 14               | 17       | 20       |      |  |
| tw                              | Minimum Pulse Width, OUT or OUT (One-Shot Mode)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 2.0        | 500              | 625      | 750      | ns   |  |
|                                 | (Figure 3)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 4.5        | 100              | 125      | 150      |      |  |
| J. Com                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 6.0        | 85               | 106      | 128      |      |  |
| tw                              | Minimum Pulse Width, OUT or OUT (Delayed Multiple Pulse Mode)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 2.0        | 125              | 155      | 190      | ns   |  |
|                                 | (Figure 3)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 4.5        | 25               | 31       | 38       |      |  |
|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 6.0        | 21               | 26       | 32       |      |  |
| tr, tf                          | Maximum Input Rise and Fall Times, Except OSC IN or START                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 2.0        | 1000             | 1000     | 1000     | ns   |  |
|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 4.5        | 500              | 500      | 500      |      |  |
|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 6.0        | 400              | 400      | 400      |      |  |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times, OSC IN or START (Figure 1)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | -          |                  | No Limit |          | -    |  |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

These pins, used in conjunction with external components, form an on-chip reference oscillator. The frequency of this oscillator and the number of counters selected determines the amount of time-out desired (see Figures 7 and 8). An external generator may be used instead of the internal oscillator. In this case, the signal should swing from ground to V<sub>CC</sub> and should be fed into OSC IN. OSC OUT 1 and OSC OUT 2 must be left floating (see Figure 9). With the crystal oscillator configuration shown in Figure 7, OSC OUT 2 must be left opencircuited.

#### OSC CONTROL (Pin 5)

This pin is used to enable or disable the oscillator. A low-to-high transition on this pin resets all counters and shuts down the oscillator. This puts the device into a low-power standby condition.

#### **COUNT CONTROL (Pin 6)**

A low-to-high transition on this pin also resets all counters. The oscillator continues to run, but the counters do not increment. This condition eliminates oscillator start-up delay time.

#### START (Pin 7)

A low-to-high transition on this pin causes the oscillator to start up, if previously disabled, and timing begins. The START

recommended that an external time base, synchronized with the start pulse, be used. With no synchronization, a start pulse occurring when the clock is high produces a different initial delay than when the start pulse occurs when the clock is low. This effect causes less error as more delay stages are selected.

#### M0, M1, M2 (Pins 13, 12, 11)

Mode inputs. These pins determine the timer's mode of operation (see Table 1).

#### S0, S1, S2, S3, S4 (Pins 17, 16, 14, 19, 18)

Select inputs. These pins select the exact divide ratio desired (see Table 2).

#### OUT (Pin 8)

This pin is the output of the timer. OUT can be fed back to either OSC CONTROL or COUNT CONTROL to inhibit counting.

## OUT (Pin 9) and has senter potentials also put no matterpools . S.

OUT is the complement of OUT. OUT can also be fed back to OSC CONTROL or COUNT CONTROL to inhibit counting.

#### NC (Pins 4, 15)

No connect pins. These pins are not connected internally.

Table 1. Output Mode Selection Table

| 081  | M  | ode Inp | uts  | to Time, 60-94 or M9-M2 to START                                                    | işinrum Bot |
|------|----|---------|------|-------------------------------------------------------------------------------------|-------------|
| Mode | M2 | M1      | MO   | Output Pulse Description                                                            | Figure      |
| 0    | 0  | 0       | 0    | Delayed Pulse (t <sub>W</sub> = 1/2f)                                               | 11, 13      |
| 91   | 0  | 0       | 0F 1 | Delayed Pulse (t <sub>W</sub> = 2/f)                                                | 11, 13      |
| 2    | 0  | 1       | 0    | Delayed Pulse (t <sub>W</sub> = 8/f)                                                | 11, 13      |
| 3    | 0  | 1       | 01 1 | Monostable Multivibrator                                                            | 10 10       |
| 4    | 1  | 0       | 0    | Delayed Burst Pulse (t <sub>W</sub> = 1/2f) t <sub>delay</sub> = t <sub>burst</sub> | 14          |
| 5    | 1  | 0       | 1    | Delayed Burst Pulse (t <sub>W</sub> = 2/f) t <sub>delay</sub> = t <sub>burst</sub>  | 14          |
| 6    | 1  | 1       | 0    | Delayed Burst Pulse (t <sub>W</sub> = 8/f) t <sub>delay</sub> = t <sub>burst</sub>  | 14          |
| 7    | 1  | 1       | 1    | Programmable Counter or Test Mode (50% Output Duty Cycle)                           | 12, 15, 17  |

Table 2. Select Divide Range

|    | Se | lect Inp | Number of Counter |   |                             |
|----|----|----------|-------------------|---|-----------------------------|
| S4 | S3 | S2       | S1 S0             |   | Stages Selected, N<br>(÷2N) |
| 0  | 0  | 0        | 0                 | 0 | 1                           |
| 0  | 0  | 0        | 0                 | 1 | 2                           |
| 0  | 0  | 0        | 1                 | 0 | 3 - 3 -                     |
| 0  | 0  | 0        | 1                 | 1 | 4                           |
| 0  | 0  | 1        | 0                 | 0 | 5                           |
| 0  | 0  | 1        | 0                 | 1 | 6                           |
| 0  | 0  | 1        | 1                 | 0 | 7                           |
| 0  | 0  | 1        | 1                 | 1 | 8                           |
| 0. | 1  | 0        | 0                 | 0 | 9                           |
| 0  | 1  | 0        | 0                 | 1 | 10                          |
| 0  | 1  | 0        | 1                 | 0 | 11                          |
| 0  | 1  | 0        | 1                 | 1 | 12                          |
| 0  | 1  | 1        | 0                 | 0 | 13                          |
| 0  | 1  | 1        | 0                 | 1 | 14                          |
| 0  | 1  | 1        | 1                 | 0 | 15                          |
| 0  | 1  | 1        | 1                 | 1 | 16                          |

|    | Se | lect Inp | uts |    | Number of Counter                          |
|----|----|----------|-----|----|--------------------------------------------|
| S4 | S3 | S2       | S1  | S0 | Stages Selected, N<br>( ÷ 2 <sup>N</sup> ) |
| 1  | 0  | 0        | 0   | 0  | 17                                         |
| 1  | 0  | 0        | 0   | 1  | 18                                         |
| 1  | 0  | 0        | 1   | 0  | 19                                         |
| 1  | 0  | 0        | 1   | 1  | 20                                         |
| 1  | 0  | 1        | 0   | 0  | 21                                         |
| 1  | 0  | 1        | 0   | 1  | 22                                         |
| 1  | 0  | 1        | 1   | 0  | 23                                         |
| 1  | 0  | 1        | 1   | 1  | 24                                         |
| 1  | 1  | 0        | 0   | 0  | 100 1*                                     |
| 1  | 1  | 0        | 0   | 1  | 2*                                         |
| 1  | 1  | 0        | 1   | 0  | 3*                                         |
| 1  | 1  | 0        | 1   | 1  | 4*                                         |
| 1  | 1  | 1        | 0   | 0  | 5*                                         |
| 1  | 1  | 1        | 0   | 1  | 6*                                         |
| 1  | 1  | 1        | 1   | 0  | 7*                                         |
| 1  | 1  | 1        | 1   | 1  | 8*                                         |

<sup>\*</sup>Configured internally such that the 24 stage counter is parallel clocked as three 8-bit counters. This allows for shorter incoming inspection testing times.

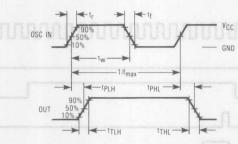


Figure 1. Switching Waveforms

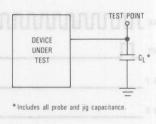
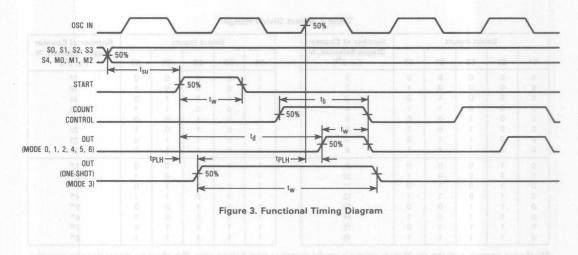


Figure 2. Test Circuit



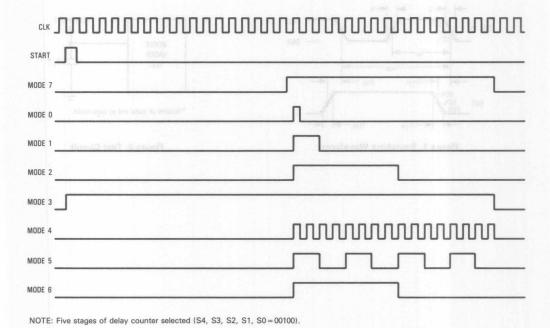


Figure 4. Timing Diagram Using Feedback

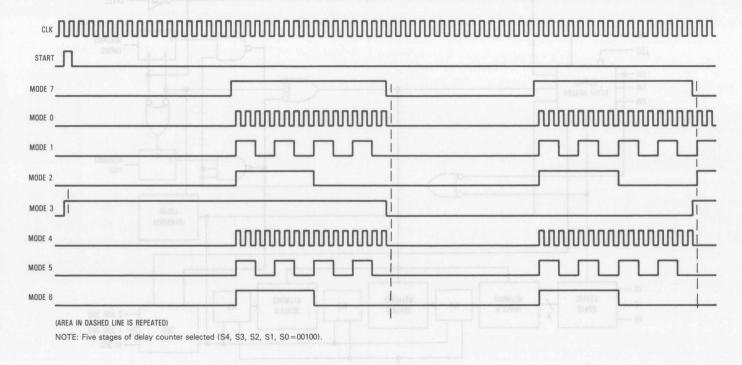


Figure 5. Timing Diagram Using No Feedback

5-638

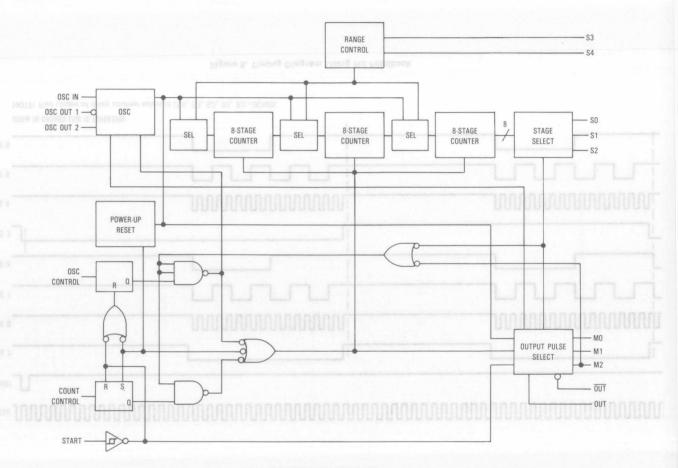


Figure 6. Block Diagram

#### OSCILLATOR DESIGN INFORMATION

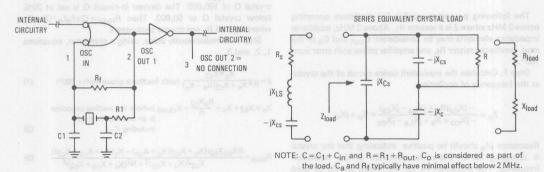
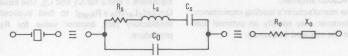


Figure 7. Pierce Oscillator

EQUIVALENT CIRCUIT FOR CRYSTAL NEAR RESONANCE



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

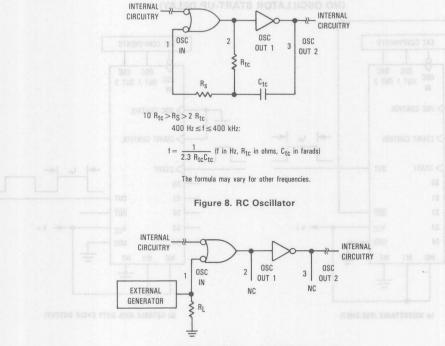


Figure 9. External Generator

#### DESIGN PROCEDURE

The following procedure applies for oscillators operating below 2 MHz where Z is a resistor R<sub>1</sub>. Above 2 MHz, additional impedance elements may be considered:  $C_{out}$  and  $C_a$  of the amp, feedback resistor R<sub>f</sub>, and amplifier phase shift error from  $180^\circ$ 

Step 1: Calculate the equivalent series circuit of the crystal at the frequency of oscillation.

$$Z_{e} = \frac{-jX_{CO}(R_{S} + jX_{LS} - jX_{CS})}{-jX_{CO} + R_{S} + jX_{LS} - jX_{CS}} = R_{e} + jX_{e}$$

Reactance  $jX_e$  should be positive, indicating that the crystal is operating as an inductive reactance at the oscillation frequency. The maximum  $R_{\rm S}$  for the crystal should be used in the equation.

Step 2: Determine  $\beta$ , the attenuation, of the feedback network. For a closed loop gain of 2,  $A_V\beta = 2$ ,  $\beta = 2/A_V$  where  $A_V$  is the gain of the HC9000 amplifier.

Step 3: Determine the manufacturer's loading capacitance. For example: a manufacturer may specify an external load capacitance of 32 pF at the required frequency.

Step 4: Determine the required Q of the system, and calculate R<sub>load</sub>. For example: a manufacturer specifies a crystal Q of 100,000. The desired in-circuit Q is set at 20% below crystal Q or 80,000. Then R<sub>load</sub> =  $(2\pi f_0 L_S/Q) - R_S$  where  $L_S$  and  $R_S$  are crystal parameters.

Step 5: Simultaneously solve, using a computer, equations 1, 2, and 3.

$$\beta = \frac{X_C * X_{C2}}{R * R_e + X_{C2}(X_e - X_C)} \text{ (with feedback phase shift = 180°)}$$
 (1)

$$X_e = X_{c2} + X_c + \frac{R_e X_{c2}}{R} = X_{cload}$$
 (where the loading capacitor is an external load not including  $C_o$ ) (2)

$$R_{load} = \frac{RX_{co}X_{c2}[(X_c + X_{c2})(X_c + X_{co}) - X_c(X_c + X_{co} + X_{c2})]}{X_{c2}^2(X_c + X_{co})^2 + R^2(X_c + X_{co} + X_{c2})^2}$$
(3)

Here  $R = R_{out} + R_1$ .  $R_{out}$  is amp output resistance,  $R_1$  is Z. The C corresponding to  $X_C$  is given by  $C = C_1 + C_{in}$ .

Alternately, pick a value for  $R_1$  (i.e. let  $R_1=R_s).$  Solve Equations 1 and 2 for  $C_1$  and  $C_2.$  Use Equation 3 and the fact  $Q=2\pi f_0 L_s/(R_s+R_{load})$  to find in-circuit Q. If Q is not satisfactory pick another value for  $R_1$  and repeat the procedure.

# APPLICATIONS INFORMATION APPLICATIONS WITH FREE-RUN OSCILLATOR (NO OSCILLATOR START-UP DELAY)

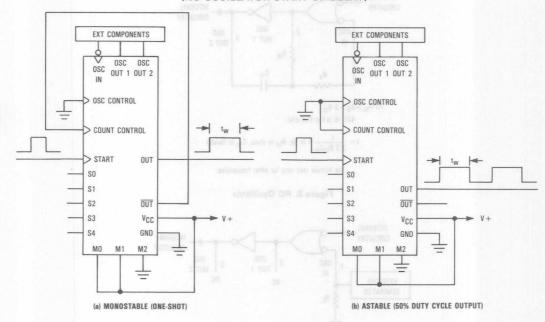
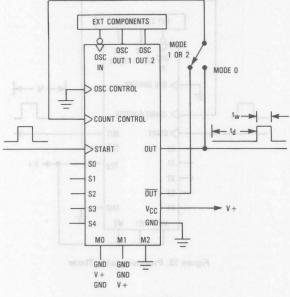


Figure 10. Multivibrator Configurations





(a) DELAYED SINGLE PULSE

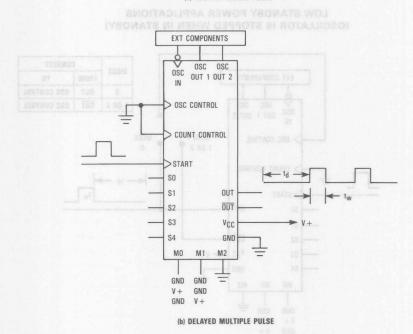


Figure 11. Delayed Pulse Configurations

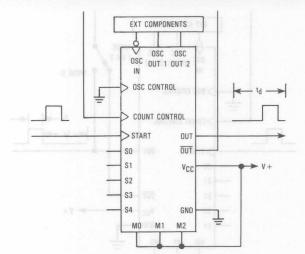


Figure 12. Programmable Timer

#### LOW STANDBY POWER APPLICATIONS (OSCILLATOR IS STOPPED WHEN IN STANDBY)

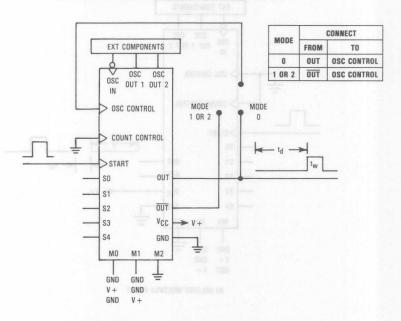


Figure 13. Delayed Single-Pulse Configuration

## MC54/74HC9000

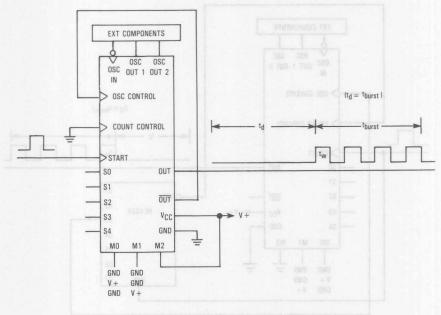


Figure 14. Burst Delayed-Pulse Configuration

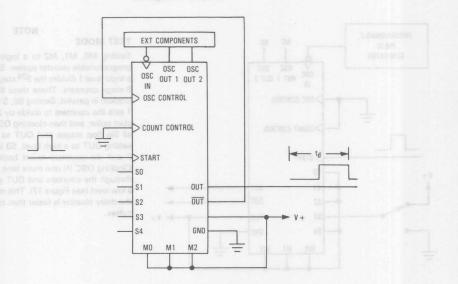


Figure 15. Programmable Timer

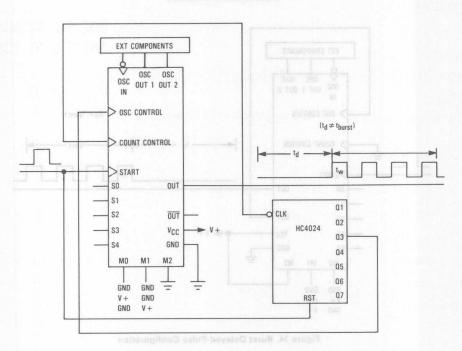


Figure 16. Delayed Multiple Pulse Configuration (4-Pulse Configured)

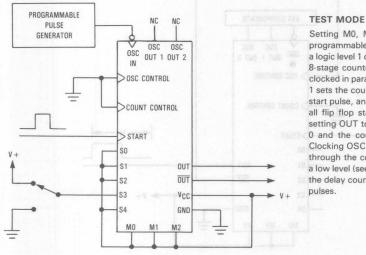


Figure 17. Test Mode (28 Divider Configuration)

NOTE

#### IODE

Setting M0, M1, M2 to a logic level 1 selects the programmable counter option. Setting S3 and S4 to a logic level 1 divides the 2<sup>24</sup> stage counter into three 8-stage counters. These three 8-stage counters are clocked in parallel. Setting S0, S1, S2, to a logic level 1 sets the counters to divide by 2<sup>8</sup> (256). Applying a start pulse, and then clocking OSC IN 255 times sets all flip flop stages and OUT to a high level. After setting OUT to a high level, S3 is set to a logic level 0 and the counters revert back to 2<sup>24</sup> operation. Clocking OSC IN one more time causes a 0 to ripple through the counters and OUT goes from a high to a low level (see Figure 17). This method of exercising the delay counter is faster than clocking in 2<sup>24</sup> clock nulses

# Product Preview

# Nine-Wide Schmitt-Trigger **Buffers**

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC9014 consists of nine inverting Schmitt-Trigger Buffers, and the MC54/74HC9015 consists of nine noninverting Schmitt-Trigger Buffers. Both devices have inputs that are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices have hysteresis and can, therefore, be used to enhance noise immunity or to square up slowly changing waveforms.

Using 9-Wide buffers, instead of standard hex buffers, decreases component count and increases system reliability.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V

HC9014

- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 90 FETs or 22.5 Equivalent Gates (HC9014) 108 FETs or 27 Equivalent Gates (HC9015)

# MC54/74HC9014 MC54/74HC9015



J SUFFIX CERAMIC **CASE 732** 



N SUFFIX PLASTIC **CASE 738** 



DW SUFFIX SOIC CASE 751D

#### ORDERING INFORMATION

| MC74HCXXXXN  |
|--------------|
| MC54HCXXXXJ  |
| MC74HCXXXXDW |

Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAMS

|      |   | HC9014 |    |      |                    |      |    | HC9015 |    |         |
|------|---|--------|----|------|--------------------|------|----|--------|----|---------|
| A1 - | 1 | -170-  | 19 | - Y1 |                    | A1 - | 1_ | (A)    | 19 | - Y1    |
| A2 - | 2 | -100   | 18 | - Y2 |                    | A2 - | 2  |        |    | – Y2    |
| A3 - | 3 | -00    | 17 | - Y3 |                    | A3 - | 3  |        | 17 | - Y3    |
| A4 - | 4 | -      | 16 | - Y4 |                    | A4 - | 4  |        |    | - Y4    |
| A5 - | 5 | -      | 15 |      | $Y = \overline{A}$ | A5 - | 5  |        | 15 | - Y5 Y= |
| A6 - | 6 | -170   | 14 | - Y6 |                    | A6 - | 6  | - D    | 14 | - Y6    |
| A7 - | 7 | -170   |    | - Y7 |                    | A7 - | 7  |        | 13 | - Y7    |
| A8 - | 8 | -170   | 12 | - Y8 |                    | A8 - | 8  |        | 12 | - Y8    |
| А9   | 9 | -      | 11 |      |                    | A9 - | 9  |        | 11 | - Y9    |
|      |   |        |    |      |                    |      |    |        |    |         |

DINI ACCIONIMENT

| A1 [  | 1 . | 20    | VCC  |
|-------|-----|-------|------|
| A2 [  | 2   | 19    | ] Y1 |
| A3 [  | 3   | 18    | ] Y2 |
| A4 [  | 4   | 17    | ] Y3 |
| A5 [  | 5   | 16    | ] Y4 |
| A6 [  |     |       | ] Y5 |
| A7 [  | 7   | 14    | ] Y6 |
| A8 [  | 8   | 13    | ] Y7 |
| A9 [  | 9   | 12    | ] Y8 |
| GND D | 10  | xe 11 | 1 Y9 |

**FUNCTION TABLE** 

| Α      | Y Outputs |        |  |  |
|--------|-----------|--------|--|--|
| Inputs | HC9014    | HC9015 |  |  |
| L      | Н         | L      |  |  |
| Н      | L         | Н      |  |  |

PIN 20 = V<sub>CC</sub> PIN 10 = GND

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

HC0015

| в | PRI |
|---|-----|
| L | -   |
| ĸ | -   |
|   |     |

| Symbol           | Parameter                                                                                         | Value                        | Unit             |
|------------------|---------------------------------------------------------------------------------------------------|------------------------------|------------------|
| Vcc              | DC Supply Voltage (Referenced to GND)                                                             | -0.5  to  +7.0               | V                |
| Vin              | DC Input Voltage (Referenced to GND)                                                              | -1.5 to V <sub>CC</sub> +1.5 | V                |
| Vout             | DC Output Voltage (Referenced to GND)                                                             | $-0.5$ to $V_{CC} + 0.5$     | V                |
| lin              | DC Input Current, per Pin                                                                         | ± 20                         | mA               |
| lout             | DC Output Current, per Pin                                                                        | ± 25                         | mA               |
| Icc              | DC Supply Current, V <sub>CC</sub> and GND Pins                                                   | ±75                          | mA               |
| PD               | Power Dissipation in Still Air, Plastic or Ceramic DIP1<br>SOIC Package1                          | 750<br>500                   | mW               |
| T <sub>stg</sub> | Storage Temperature                                                                               | -65 to +150                  | °C               |
| TLAS             | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package)<br>(Ceramic DIP) | 260<br>300                   | nolata<br>nolata |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP:  $-10 \text{ mW/}^{\circ}\text{C}$  from  $100^{\circ}$  to  $125^{\circ}\text{C}$ 

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

| Symbol                            | Parameter                                            | Min   | Max          | Unit |
|-----------------------------------|------------------------------------------------------|-------|--------------|------|
| Vcc                               | DC Supply Voltage (Referenced to GND)                | 2.0   | 6.0          | V    |
| V <sub>in</sub> ,V <sub>out</sub> | DC Input Voltage, Output Voltage (Referenced to GND) | 0     | Vcc          | V    |
| TA                                | Operating Temperature, All Package Types             | - 55  | + 125        | °C   |
| t <sub>r</sub> , t <sub>f</sub>   | Input Rise and Fall Time (Figure 1)                  | 21005 | no<br>limit* | ns   |

<sup>\*</sup>When  $V_{in} = 0.5 V_{CC}$ ,  $I_{CC} >$  quiescent current.

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

|                              | 1202                                                            | 01                                                                                     | 2                 | Gu                   | aranteed L           | imit                  |      |
|------------------------------|-----------------------------------------------------------------|----------------------------------------------------------------------------------------|-------------------|----------------------|----------------------|-----------------------|------|
| Symbol                       | Parameter Test Conditions                                       | Test Conditions                                                                        | V <sub>CC</sub>   | 25°C                 | -40°C<br>to<br>+85°C | -55°C<br>to<br>+125°C | Unit |
| V <sub>T +</sub> max         | Maximum Positive-Going<br>Input Threshold Voltage<br>(Figure 3) | V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V<br> I <sub>out</sub>  ≤20 μA         | 2.0<br>4.5<br>6.0 | 1.50<br>3.15<br>4.20 | 1.50<br>3.15<br>4.20 | 1.50<br>3.15<br>4.20  | ٧    |
| V <sub>T+</sub> min          | Minimum Positive-Going<br>Input Threshold Voltage<br>(Figure 3) | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \le 20 \mu\text{A}$ | 2.0<br>4.5<br>6.0 | 1.00<br>2.30<br>3.00 | 0.95<br>2.25<br>2.95 | 0.95<br>2.25<br>2.95  | V    |
| V <sub>T —</sub> max         | Maximum Negative-Going<br>Input Threshold Voltage<br>(Figure 3) | V <sub>out</sub> =V <sub>CC</sub> -0.1 V or 0.1 V<br> l <sub>out</sub>  ≤20 μA         | 2.0<br>4.5<br>6.0 | 0.90<br>2.00<br>2.60 | 0.95<br>2.05<br>2.65 | 0.95<br>2.05<br>2.65  | ٧    |
| V <sub>T</sub> _min          | Minimum Negative-Going<br>Input Threshold Voltage<br>(Figure 3) | V <sub>out</sub> =V <sub>CC</sub> − 0.1 V or 0.1 V<br> I <sub>out</sub>   ≤20 μA       | 2.0<br>4.5<br>6.0 | 0.30<br>0.90<br>1.20 | 0.30<br>0.90<br>1.20 | 0.30<br>0.90<br>1.20  | ٧    |
| V <sub>H</sub> max<br>Note 2 | Maximum Hysteresis Voltage<br>(Figure 3)                        | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> − 0.1 V<br> I <sub>out</sub>   ≤20 μA      | 2.0<br>4.5<br>6.0 | 1.20<br>2.25<br>3.00 | 1.20<br>2.25<br>3.00 | 1.20<br>2.25<br>3.00  | ٧    |
| V <sub>H</sub> min<br>Note 2 | Minimum Hysteresis Voltage<br>(Figure 3)                        | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \le 20 \mu\text{A}$ | 2.0<br>4.5<br>6.0 | 0.20<br>0.40<br>0.50 | 0.20<br>0.40<br>0.50 | 0.20<br>0.40<br>0.50  | V    |

#### NOTES:

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2.  $V_H min > (V_{T+} min) (V_{T} max)$ ;  $V_H max = (V_{T+} max) (V_{T-} min)$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

|                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                    | Vcc               | Gua               |                   |                   |         |
|--------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-------------------|-------------------|-------------------|---------|
| Symbol                               | Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Test Conditions                                                                                                                                                    |                   | 25°C to<br>-55°C  | ≤85°C             | ≤125°C            | Unit    |
| Vон                                  | Minimum High-Level Output<br>Voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | $V_{in} \le V_{T-min}$ or $V_{in} \ge V_{T+max}$<br>$ I_{out}  \le 20 \mu A$                                                                                       | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | A IV    |
|                                      | AND THE PARTY OF T | $V_{in} \le V_T$ min or $V_{in} \ge V_T$ max $\begin{vmatrix} I_{out} \end{vmatrix} \le 4.0 \text{ mA}$ $\begin{vmatrix} I_{out} \end{vmatrix} \le 5.2 \text{ mA}$ | 4.5<br>6.0        | 3.98<br>5.48      | 3.84<br>5.34      | 3.70<br>5.20      | Y TUSTE |
| VOL Maximum Low-Level Output Voltage |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | $V_{in} \ge V_{T+} \max \text{ or } V_{in} \le V_{T-} \min $ $ I_{out}  \le 20 \mu A$                                                                              | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | ٧       |
|                                      | Figure 18, HQ8016                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | $V_{in} \ge V_{T+} \max \text{ or } V_{in} \le V_{T-} \min \  I_{out}  \le 4.0 \text{ mA} \  I_{out}  \le 5.2 \text{ mA}$                                          | 4.5<br>6.0        | 0.26<br>0.26      | 0.33<br>0.33      | 0.40<br>0.40      |         |
| I <sub>in</sub>                      | Maximum Input Leakage Current                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Vin=VCC or GND                                                                                                                                                     | 6.0               | ±0.1              | ±1.0              | ±1.0              | μΑ      |
| Icc                                  | Maximum Quiescent Supply<br>Current (per Package)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | V <sub>in</sub> =V <sub>CC</sub> or GND 1187771<br>I <sub>out</sub> =0 μA                                                                                          | 6.0               | 2                 | 20                | 40                | μΑ      |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C1 = 50 pF, Input tr = tf = 6 ns)

|        |                                                                  |                                | Vcc        | Pr               | ojected Lir | nit       |      |
|--------|------------------------------------------------------------------|--------------------------------|------------|------------------|-------------|-----------|------|
| Symbol | Parameter 145163 tes                                             | Parameter 110010 2007 S 511017 |            | 25°C to<br>-55°C | ≤85°C       | ≤125°C    | Unit |
| tPLH,  | Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2) | HC9014                         | 2.0<br>4.5 | 85<br>17         | 105<br>21   | 130<br>26 | ns   |
|        |                                                                  |                                | 6.0        | 14               | 18          | 22        |      |
|        |                                                                  | HC9015                         | 2.0        | 95               | 120         | 145       |      |
|        |                                                                  |                                | 4.5        | 19               | 24          | 29        |      |
|        |                                                                  |                                | 6.0        | 16               | 20          | 25        |      |
| tTLH,  | Maximum Output Transition Time, Any Output                       | No.                            | 2.0        | 75               | 95          | 110       | ns   |
| tTHL   | (Figures 1 and 2)                                                |                                | 4.5        | 15               | 19          | 22        |      |
|        |                                                                  |                                | 6.0        | 13               | 16          | 19        |      |
| Cin    | Maximum Input Capacitance                                        |                                |            | 10               | 10          | 10        | pF   |

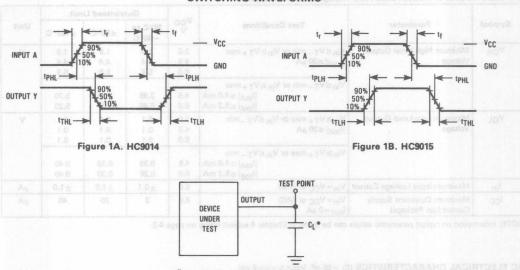
#### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.

2. Information on typical parametric values can be found in Chapter 4.

| CPD | Power Dissipation Capacitance (Per Buffer)                                                                                                                         | Typical @ 25°C, V <sub>CC</sub> =5.0 V |    |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|----|
|     | Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f+ICC VCC  For load considerations, see Chapter 4 subject listing on page 4-2. | 30                                     | pF |

#### SWITCHING WAVEFORMS



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

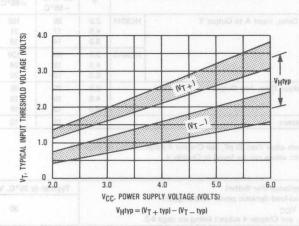


Figure 3. Typical Input Threshold, V<sub>T+</sub>, V<sub>T-</sub> Versus Power Supply Voltage

#### **EXPANDED LOGIC DIAGRAMS**



# Advance Information

# **Nine-Wide Buffers High-Performance Silicon-Gate CMOS**

The MC54/74HC9034 consists of nine inverting buffers and the MC54/74HC9035 consists of nine noninverting buffers. Both devices have inputs that are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL

These devices find primary use as interfaces between microprocessors and peripheral hardware such as keyboards, memory arrays, displays, etc. They are especially useful when 8 bits of data are needed and an extra bit is required for parity, control,

Using 9-Wide buffers, instead of standard hex buffers, decreases component count and increases system reliability.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 54 FETs or 13.5 Equivalent Gates (HC9034) 72 FETs or 18 Equivalent Gates (HC9035)

# MC54/74HC9034 MC54/74HC9035



#### ORDERING INFORMATION

| MC74HCXXXXN  | Plastic |
|--------------|---------|
| MC54HCXXXXJ  | Ceran   |
| MC74HCXXXXDW | SOIC    |

nic

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAMS

|        | HC9034  |                    |                    | нс | 9035 |               |
|--------|---------|--------------------|--------------------|----|------|---------------|
| A1 1   |         |                    | A1-                | 1  | >    | 19Y1          |
| A22    | 18 Y2   |                    | A2 —               | 2  | >    | 18 Y2         |
| A3 — 3 | — 17 y3 |                    | 0 A3 —             | 3  | >    | 17 Y3         |
| A4 4   | 16 Y4   |                    | A4 —               | 4  |      | 16 Y4         |
| A55    | 15 Y5   | $Y = \overline{A}$ | 8 A5 —             | 5  | >-   | 15 Y5 Y       |
| A6 — 6 | 14 Y6   |                    | A6 —               | 6  |      | 14 J/V 16 HIV |
| A7 7   | 13 Y7   |                    | 8 A7 —             | 7  | >-   | 77 052        |
| A88    | 12 Y8   |                    | A8 -               | 8  | > 1  | 2Y8           |
| A9 9   |         |                    | 0.8<br>0.8<br>49 — | 9  | >-   | 1 Y9 30V      |

PIN 20 = VCC PIN 10 = GND

# PIN ASSIGNMENT

| A1 D  | 1 •        | 20 7 VCC |
|-------|------------|----------|
| A2 [  | 2          | 19 71    |
| A3 [  | 3          | 18 72    |
| A4 [  | 4          | 17 73 Y3 |
| A5 [  | 5 408110   | 16 74    |
| A6 [  | 6          | 15 75    |
| A7 [  | 7          | 14 76    |
| A8 🗖  | 8          | 13 TY7   |
| A9 [  | 9H muminit | 12 Y8    |
| GND [ | 10         | 11 Y9    |

#### **FUNCTION TABLE**

| Α         | Y Ou         | tputs  |
|-----------|--------------|--------|
| Input     | HC9034       | HC9035 |
| L         | Н            | L      |
| put H rug | Managroom 1s | Н      |

This document contains information on a new product. Specifications and information herein are subject to change without notice.

= A

| Ľ | á | h | 3 |  |
|---|---|---|---|--|
| r | ٦ | p |   |  |
| ь |   | 3 | d |  |

|                  |                                                                                                   | varuo                          | Unit |
|------------------|---------------------------------------------------------------------------------------------------|--------------------------------|------|
| Vcc              | DC Supply Voltage (Referenced to GND)                                                             | -0.5 to $+7.0$                 | V    |
| Vin              | DC Input Voltage (Referenced to GND)                                                              | - 1.5 to V <sub>CC</sub> + 1.5 | V    |
| Vout             | DC Output Voltage (Referenced to GND)                                                             | $-0.5$ to $V_{CC} + 0.5$       | V    |
| lin              | DC Input Current, per Pin                                                                         | ±20                            | mA   |
| lout             | DC Output Current, per Pin                                                                        | ± 25                           | mA   |
| Icc              | DC Supply Current, V <sub>CC</sub> and GND Pins                                                   | ± 75                           | mA   |
| PD               | Power Dissipation in Still Air, Plastic or Ceramic DIP1<br>SOIC Package1                          | 750<br>500                     | mW   |
| T <sub>stg</sub> | Storage Temperature                                                                               | -65 to +150                    | °C   |
| т                | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package)<br>(Ceramic DIP) | 260<br>300                     | °C   |

Inis device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{In}$  and  $V_{out}$  should be constrained to the range  $GND \le (V_{in}$  or  $V_{out}) \le V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

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\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

| Symbol                            | Parameter                                | edand No. 7A             | Min  | Max   | Unit |
|-----------------------------------|------------------------------------------|--------------------------|------|-------|------|
| Vcc                               | DC Supply Voltage (Referenced to GND)    |                          | 2.0  | 6.0   | V    |
| V <sub>in</sub> ,V <sub>out</sub> | DC Input Voltage, Output Voltage (       | Referenced to GND)       | 0    | Vcc   | V    |
| TA                                | Operating Temperature, All Package Types |                          | - 55 | + 125 | °C   |
| tr, tf                            | Input Rise and Fall Time                 | V <sub>CC</sub> = 2.0 V  | 0    | 1000  | ns   |
|                                   | (Figure 1)                               | V <sub>CC</sub> = 4.5 V  | 0    | 500   |      |
|                                   |                                          | $V_{CC} = 6.0 \text{ V}$ | 0    | 400   |      |

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

|        | e shex                                            | 17-01                                                                                          | V                 | Gua                | 14                 |                    |        |
|--------|---------------------------------------------------|------------------------------------------------------------------------------------------------|-------------------|--------------------|--------------------|--------------------|--------|
| Symbol | Parameter                                         | Test Conditions                                                                                | VCC               | 25°C to<br>-55°C   | ≤85°C              | ≤125°C             | Unit   |
| VIH    | Minimum High-Level Input<br>Voltage               | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \le 20 \mu \text{A}$        | 2.0<br>4.5<br>6.0 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | ٧      |
| VIL    | Maximum Low-Level Input<br>Voltage                | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \le 20 \mu\text{A}$         | 2.0<br>4.5<br>6.0 | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | V      |
| Voн    | Minimum High-Level Output<br>Voltage              | V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>  ≤20 μA               | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | V      |
|        |                                                   | $V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$<br>$ I_{out}  \le 5.2 \text{ mA}$ | 4.5<br>6.0        | 3.98<br>5.48       | 3.84<br>5.34       | 3.70<br>5.20       | ē - 8/ |
| VOL    | Maximum Low-Level Output<br>Voltage               | V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>  ≤20 μA               | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | V      |
| HCBD3  | input RCS03A                                      | $V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \le 4.0 \text{ mA}$<br>$ I_{out}  \le 5.2 \text{ mA}$ | 4.5<br>6.0        | 0.26<br>0.26       | 0.33<br>0.33       | 0.40<br>0.40       | 9      |
| lin    | Maximum Input Leakage Current                     | Vin=VCC or GND                                                                                 | 6.0               | ± 0.1              | ± 1.0              | ± 1.0              | μΑ     |
| lcc    | Maximum Quiescent Supply<br>Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA                            | 6.0               | 2                  | 20                 | 40                 | μΑ     |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

#### AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

|               | AND ARREST OF ASSESSED IN                                              |                      | Gu               |                 |                 |      |
|---------------|------------------------------------------------------------------------|----------------------|------------------|-----------------|-----------------|------|
| Symbol        | Parameter                                                              | Vcc                  | 25°C to<br>-55°C | ≤85°C           | ≤125°C          | Unit |
| tPLH,<br>tPHL | Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)  HC90 | 2.0<br>4.5<br>6.0    | 80<br>16<br>14   | 100<br>20<br>17 | 120<br>24<br>20 | ns   |
|               | HC90                                                                   | 35 2.0<br>4.5<br>6.0 | 90<br>18<br>15   | 115<br>23<br>20 | 135<br>27<br>23 |      |
| tTLH,<br>tTHL | Maximum Output Transition Time, Any Output (Figures 1 and 2)           | 2.0<br>4.5<br>6.0    | 75<br>15<br>13   | 95<br>19<br>16  | 110<br>22<br>19 | ns   |
| Cin           | Maximum Input Capacitance                                              | _                    | 10               | 10              | 10              | pF   |

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
  - 2. Information on typical parametric values can be found in Chapter 4.

| CPD | Power Dissipation Capacitance (Per Buffer)                                                      | Typical @ 25°C, V <sub>CC</sub> =5.0 V | ri brus ann |
|-----|-------------------------------------------------------------------------------------------------|----------------------------------------|-------------|
|     | Used to determine the no-load dynamic power consumption:  PD = CPD VCC <sup>2</sup> f + ICC VCC | wive Cecabilly 06 0 LSTTL Leaus        | pF          |
|     | For load considerations, see Chapter 4 subject listing on page 4-2.                             | OS-Compatible Input Lavels             | MINTE       |

#### **SWITCHING WAVEFORMS**

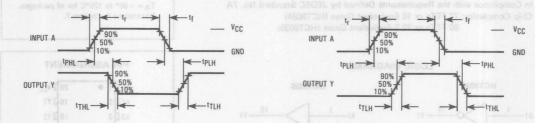
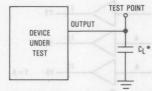


Figure 1A. HC9034

Figure 1B. HC9035



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

# EXPANDED LOGIC DIAGRAMS (1/9 of the Device)



# Advance Information

# Nine Wide Buffers with LSTTL Compatible Inputs

# **High-Performance Silicon-Gate CMOS**

The MC54/74HCT9034 and MC54/74HCT9035 may be used as level converters for interfacing TTL or NMOS outputs to CMOS inputs.

The HCT9034 consists of nine inverting buffers, and the HCT9035 consists of nine noninverting buffers.

These devices find primary use as interfaces between microprocessors and peripheral hardware such as keyboards, memory arrays, displays, etc. They are especially useful when 8 bits of data is needed and an extra bit is required for parity, control

Using Nine Wide buffers, instead of standard hex buffers, decreases component count and increases system reliability.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates (HCT9034) 90 FETs or 22.5 Equivalent Gates (HCT9035)

# MC54/74HCT9034 MC54/74HCT9035



J SUFFIX CERAMIC **CASE 732** 



PLASTIC **CASE 738** 



DW SUFFIX SOIC CASE 751D

#### ORDERING INFORMATION

MC74HCTXXXXN MC54HCTXXXXJ MC74HCTXXXXDW SOIC

Ceramic

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

#### LOGIC DIAGRAMS

|      | НСТ9034 |       |                        |      | н | T9035       |         |             |              |
|------|---------|-------|------------------------|------|---|-------------|---------|-------------|--------------|
| A1-  | 1       | 19 Y1 | - M-10                 | A1-  | 1 | <b>&gt;</b> | 19      | — Y1        |              |
| A2 - | 2       | 18 Y2 |                        | A2 - | 2 | >           | 18      | — Y2        |              |
| A3 - | 3       | 17 Y3 |                        | A3 - | 3 | >           | 17      | _ Y3        |              |
| A4 - | 4       | 16 Y4 |                        | A4 - | 4 | >           | 16      | — Y4        |              |
| A5 - | 5       | 15 Y5 | $Y=\overline{A}$       | A5 - | 5 | >           | 15      | – Y5        | Y = <i>I</i> |
| A6 - | 6       | 14Y6  |                        | A6 - | 6 | /           | 14      |             |              |
| A7 - | 7       | Y7    |                        | A7 - | 7 | >           | 13      | —Y7         |              |
| A8 - | 8       | 12Y8  |                        | A8 - | 8 | >           | 12      | —Y8         |              |
| A9 - | 9       | 11 Y9 |                        | A9 - | 9 |             | 11<br>A | <b>—</b> Y9 |              |
|      |         | PII   | N 20 = V <sub>CC</sub> |      |   | 1           |         |             |              |

PIN 10 = GND

#### PIN ASSIGNMENT

| JOS Lagranage Contraction |     |                     |   |  |
|---------------------------|-----|---------------------|---|--|
| A1 [                      | 1 • | 20 0 V <sub>C</sub> | C |  |
| A2 [                      | 2   | 19 Y1               |   |  |
| A3 [                      | 3   | 18 72               |   |  |
| A4 [                      | 4   | 17 7 Y3             |   |  |
| A5 🗖                      | 5   | 16 74               |   |  |
| A6 C                      | 6   | 15 75               |   |  |
| A7 [                      | 7   | 14 76               |   |  |
| A8 [                      | 8   | 13 77               |   |  |
| A9 [                      | 9   | 12 Y8               |   |  |
| GND [                     | 10  | 11 Y9               |   |  |
|                           |     |                     |   |  |

#### **FUNCTION TABLE**

|   | Δ     | Y Outputs |         |  |  |
|---|-------|-----------|---------|--|--|
|   | Input | HCT9034   | HCT9035 |  |  |
| T | L     | Н         | L       |  |  |
|   | Н     | L         | Н       |  |  |

This document contains information on a new product. Specifications and information herein are subject to change without notice

#### **MAXIMUM RATINGS\***

| Symbol           | Parameter                                                                                         | Value                        | Unit |
|------------------|---------------------------------------------------------------------------------------------------|------------------------------|------|
| Vcc              | DC Supply Voltage (Referenced to GND)                                                             | -0.5 to +7.0                 | V    |
| Vin              | DC Input Voltage (Referenced to GND)                                                              | -1.5 to V <sub>CC</sub> +1.5 | ٧    |
| Vout             | DC Output Voltage (Referenced to GND)                                                             | -0.5 to V <sub>CC</sub> +0.5 | V    |
| lin              | DC Input Current, per Pin                                                                         | ±20                          | mA   |
| lout             | DC Output Current, per Pin                                                                        | ±25                          | mA   |
| Icc              | DC Supply Current, V <sub>CC</sub> and GND Pins                                                   | ±75                          | mA   |
| PD               | Power Dissipation in Still Air, Plastic or Ceramic DIP1<br>SOIC Package1                          | 750<br>500                   | mW   |
| T <sub>stg</sub> | Storage Temperature                                                                               | -65 to +150                  | °C   |
| TL               | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package)<br>(Ceramic DIP) | 260<br>300                   | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND≤(Vin or Vout)≤VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

| Symbol                            | Parameter                                            | Min  | Max   | Unit |
|-----------------------------------|------------------------------------------------------|------|-------|------|
| Vcc                               | DC Supply Voltage (Referenced to GND)                | 4.5  | 5.5   | V    |
| V <sub>in</sub> ,V <sub>out</sub> | DC Input Voltage, Output Voltage (Referenced to GND) | 0    | Vcc   | V    |
| TA                                | Operating Temperature, All Package Types             | - 55 | + 125 | °C   |
| t <sub>r</sub> , t <sub>f</sub>   | Input Rise and Fall Time (Figure 1)                  | 0    | 500   | ns   |

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

|        |                                                   |                                                                                                      |            | Guaranteed Limit |            |            | 171  |
|--------|---------------------------------------------------|------------------------------------------------------------------------------------------------------|------------|------------------|------------|------------|------|
| Symbol | Parameter                                         | Test Conditions                                                                                      | VCC        | 25°C to<br>-55°C | ≤85°C      | ≤125°C     | Unit |
| VIH    | Minimum High-Level Input<br>Voltage               | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \le 20 \mu\text{A}$               | 4.5<br>5.5 | 2.0<br>2.0       | 2.0<br>2.0 | 2.0<br>2.0 | ٧    |
| VIL    | Maximum Low-Level Input<br>Voltage                | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \le 20 \mu\text{A}$               | 4.5<br>5.5 | 0.8              | 0.8<br>0.8 | 0.8<br>0.8 | ٧    |
| VOH    | Minimum High-Level Output<br>Voltage              | $V_{in} = V_{IH}$ or $V_{IL}$ 131030 $ I_{out}  \le 20 \mu A$                                        | 4.5<br>5.5 | 4.4<br>5.4       | 4.4<br>5.4 | 4.4<br>5.4 | ٧    |
|        |                                                   | $V_{in} = V_{IH}$ or $V_{IL}$<br>$ I_{out}  \le 4.0$ mA                                              | 4.5        | 3.98             | 3.84       | 3.70       |      |
| VOL    | Maximum Low-Level Output<br>Voltage               | $V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$<br>$ I_{\text{out}}  \le 20 \ \mu\text{A}$ | 4.5<br>5.5 | 0.1<br>0.1       | 0.1<br>0.1 | 0.1<br>0.1 | ٧    |
|        |                                                   | $V_{in} = V_{IH}$ or $V_{IL}$<br>$ I_{out}  \le 4.0 \text{ mA}$                                      | 4.5        | 0.26             | 0.33       | 0.40       |      |
| lin    | Maximum Input Leakage Current                     | Vin=VCC or GND                                                                                       | 5.5        | ±0.1             | ± 1.0      | ±1.0       | μΑ   |
| Icc    | Maximum Quiescent Supply<br>Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 µA                                  | 5.5        | 2                | 20         | 40         | μΑ   |

| ΔICC | Additional Quiescent Supply | V <sub>in</sub> =2.4 V, Any One Input                      |     | ≥ -55°C | 25°C to 125°C |    |
|------|-----------------------------|------------------------------------------------------------|-----|---------|---------------|----|
| y    | Current                     | $V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0 \mu A$ | 5.5 | 2.9     | 2.4           | mA |

#### NOTES:

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

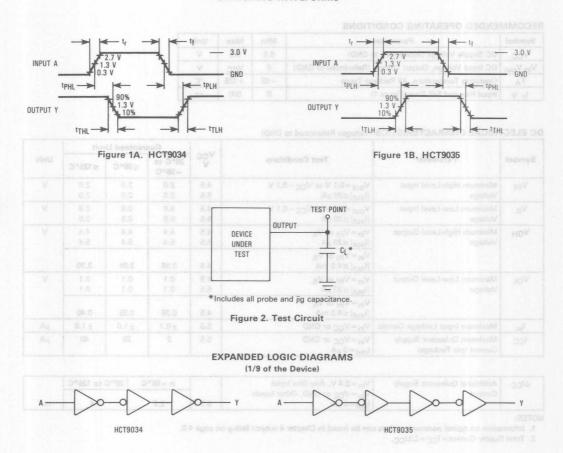
|               | Value (User ) this onvious or                     |                     | Gua     | 10dmy8 |           |        |    |
|---------------|---------------------------------------------------|---------------------|---------|--------|-----------|--------|----|
| Symbol        | empeties of the depth of sub V   8.1 = 20V of 8.1 | CMDI                | 25°C to | 0500   | Viqqu8 00 | Unit   |    |
|               |                                                   |                     | (10)    | -55°C  | ≤85°C     | ≤125°C |    |
| tPLH,<br>tPHL | Maximum Propagation Delay,<br>(Figures 1 and 2)   | Input A to Output Y | (CND)   | 23     | 29        | 35 00  | ns |
| tTLH,<br>tTHL | Maximum Output Transition (Figures 1 and 2)       | Fime, Any Output    |         | 15     | 19        | 22     | ns |
| Cin           | Maximum Input Capacitance                         | 2011                |         | 10     | 10        | 10     | pF |

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

| CPD | Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: | Typical @ 25°C, V <sub>CC</sub> = 5.0 V     |    |
|-----|-----------------------------------------------------------------------------------------------------|---------------------------------------------|----|
|     | PD = CPD VCC <sup>2</sup> f + ICC VCC                                                               | ett ar en mort om war 38 sig strates        | pF |
|     | For load considerations, see Chapter 4 subject listing on page 4-2.                                 | Carponia Offic 10 retti 197 Julies 1999 to. |    |

#### SWITCHING WAVEFORMS



# Nine-Wide Schmitt-Trigger Buffers with Open-Drain Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC9114 consists of nine inverting Schmitt-Trigger Buffers, and the MC54/74HC9115 consists of nine noninverting Schmitt-Trigger Buffers. Both devices have inputs that are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

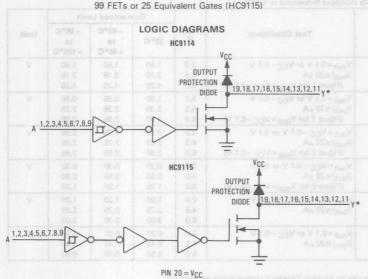
These devices have hysteresis and can, therefore, be used to enhance noise immunity or to square up slowly changing waveforms.

Primary use for these devices are as interfaces between microprocessors and peripheral hardware such as keyboards, memory arrays, displays, etc. They are especially useful when 8 bits of data are needed and an extra bit is required for parity, control, or handshake.

Each of the HC9114 and HC9115 outputs are fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable output pullup resistor, these gates can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

Using 9-Wide buffers, instead of standard hex buffers, decreases component count and increases system reliability.

- Output Drive Capability: 10 LSTTL Loads with Suitable Pullup Resistor
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 81 FETs or 20 Equivalent Gates (HC9114)



PIN 10 = GND
\*Denotes open-drain outputs

MC54/74HC9114 MC54/74HC9115



J SUFFIX CERAMIC CASE 732



N SUFFIX PLASTIC CASE 738



DW SUFFIX SOIC CASE 751D

#### ORDERING INFORMATION

MC74HCXXXXN MC54HCXXXXJ MC74HCXXXXDW Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

## PIN ASSIGNMENT

| A1 [  | 1 • | 20 | 1 vcc       |
|-------|-----|----|-------------|
| A2 [  | 2   | 19 | 1 Y 1       |
| A3 [  | 3   | 18 | 1 Y2        |
| A4 [  | 4   | 17 | ] Y3        |
| A5 [  | 5   | 16 | 1 Y4        |
| A6 [  | 6   | 15 | <b>1</b> Y5 |
| A7 [  | 7   | 14 | 1 Y6        |
| A8 [  | 8   | 13 | 1 Y7        |
| A9 [  | 9   | 12 | 1 Y8        |
| GND [ | 10  | 11 | 1 Y9        |

#### **FUNCTION TABLE**

| A      | Y Outputs |        |  |  |  |
|--------|-----------|--------|--|--|--|
| Inputs | HC9114    | HC9115 |  |  |  |
| L      | Z         | L      |  |  |  |
| Н      | mungodi   | Z      |  |  |  |

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| Symbol           | Parameter                                                                                         | Value                          | Unit |
|------------------|---------------------------------------------------------------------------------------------------|--------------------------------|------|
| VCC              | DC Supply Voltage (Referenced to GND)                                                             | -0.5 to +7.0                   | ٧    |
| Vin              | DC Input Voltage (Referenced to GND)                                                              | - 1.5 to V <sub>CC</sub> + 1.5 | ٧    |
| Vout             | DC Output Voltage (Referenced to GND)                                                             | -0.5 to V <sub>CC</sub> +0.5   | V    |
| nil st           | DC Input Current, per Pin                                                                         | ± 20                           | mA   |
| lout             | DC Output Current, per Pin                                                                        | ± 25                           | mA   |
| Icc              | DC Supply Current, V <sub>CC</sub> and GND Pins                                                   | ± 75                           | mA   |
| PD               | Power Dissipation in Still Air, Plastic or Ceramic DIP1<br>SOIC Package1                          | 750<br>500                     | mW   |
| T <sub>stg</sub> | Storage Temperature                                                                               | -65 to +150                    | °C   |
| TASI             | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package)<br>(Ceramic DIP) | 260<br>300                     | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\mathsf{GND} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

| Symbol                            | Parameter                                            | Min  | Max          | Unit |
|-----------------------------------|------------------------------------------------------|------|--------------|------|
| Vcc                               | DC Supply Voltage (Referenced to GND)                | 2.0  | 6.0          | V    |
| V <sub>in</sub> ,V <sub>out</sub> | DC Input Voltage, Output Voltage (Referenced to GND) | 0    | Vcc          | ٧    |
| TA                                | Operating Temperature, All Package Types             | - 55 | + 125        | °C   |
| t <sub>r</sub> , t <sub>f</sub>   | Input Rise and Fall Time (Figure 1)                  | _    | no<br>limit* | ns   |

<sup>\*</sup>When  $V_{in} = 0.5 V_{CC}$ ,  $I_{CC} >$  quiescent current.

#### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

|                              | Parameter                                                       |                                                                                                                                                                                 |                   | Guaranteed Limit     |                      |                       |      |
|------------------------------|-----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|----------------------|----------------------|-----------------------|------|
| Symbol                       |                                                                 | Test Conditions                                                                                                                                                                 | VCC<br>V          | 25°C                 | -40°C<br>to<br>+85°C | -55°C<br>to<br>+125°C | Unit |
| V <sub>T+</sub> max          | Maximum Positive-Going<br>Input Threshold Voltage<br>(Figure 3) | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \le 20 \mu\text{A}$<br>(Figure 2 for $V_{out} = V_{CC} - 0.1 \text{ V}$ )                                    | 2.0<br>4.5<br>6.0 | 1.50<br>3.15<br>4.20 | 1.50<br>3.15<br>4.20 | 1.50<br>3.15<br>4.20  | V    |
| V <sub>T+</sub> min          | Minimum Positive-Going<br>Input Threshold Voltage<br>(Figure 3) | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> l <sub>out</sub>   ≤ 20 μA<br>(Figure 2 for V <sub>out</sub> = V <sub>CC</sub> - 0.1 V)                                 | 2.0<br>4.5<br>6.0 | 1.00<br>2.30<br>3.00 | 0.95<br>2.25<br>2.95 | 0.95<br>2.25<br>2.95  | ٧    |
| V <sub>T</sub> _ max         | Maximum Negative-Going<br>Input Threshold Voltage<br>(Figure 3) | $V_{\text{out}} = V_{\text{CC}} - 0.1 \text{ V or } 0.1 \text{ V}$<br>$ I_{\text{out}}  \le 20 \mu\text{A}$<br>(Figure 2 for $V_{\text{out}} = V_{\text{CC}} - 0.1 \text{ V}$ ) | 2.0<br>4.5<br>6.0 | 0.90<br>2.00<br>2.60 | 0.95<br>2.05<br>2.65 | 0.95<br>2.05<br>2.65  | ٧    |
| V <sub>T</sub> _ min         | Minimum Negative-Going<br>Input Threshold Voltage<br>(Figure 3) | $V_{\text{out}} = V_{\text{CC}} - 0.1 \text{ V or } 0.1 \text{ V}$<br>$ I_{\text{out}}  \le 20 \mu\text{A}$<br>(Figure 2 for $V_{\text{out}} = V_{\text{CC}} - 0.1 \text{ V}$ ) | 2.0<br>4.5<br>6.0 | 0.30<br>0.90<br>1.20 | 0.30<br>0.90<br>1.20 | 0.30<br>0.90<br>1.20  | ٧    |
| V <sub>H</sub> max<br>Note 2 | Maximum Hysteresis Voltage<br>(Figure 3)                        | $V_{\text{out}} = 0.1 \text{ V or } V_{\text{CC}} = 0.1 \text{ V}$<br>$ I_{\text{out}}  \le 20 \mu\text{A}$                                                                     | 2.0<br>4.5<br>6.0 | 1.20<br>2.25<br>3.00 | 1.20<br>2.25<br>3.00 | 1.20<br>2.25<br>3.00  | ٧    |
| V <sub>H</sub> min<br>Note 2 | Minimum Hysteresis Voltage<br>(Figure 3)                        | V <sub>out</sub> =0.1 V or V <sub>CC</sub> −0.1 V<br> I <sub>out</sub>  ≤20 μA                                                                                                  | 2.0<br>4.5<br>6.0 | 0.20<br>0.40<br>0.50 | 0.20<br>0.40<br>0.50 | 0.20<br>0.40<br>0.50  | V    |

#### NOTES:

- 1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- 2.  $V_H min > (V_T + min) (V_T max); V_H max = (V_T + max) (V_T min).$

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.

## MC54/74HC9114•MC54/74HC9115

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

|                 | Parameter                                                                                        |                                                                                               | .,                | Gua               | aranteed L        | imit              | Unit |
|-----------------|--------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|-------------------|-------------------|-------------------|-------------------|------|
| Symbol          |                                                                                                  | Test Conditions                                                                               | VCC               | 25°C to<br>-55°C  | ≤85°C             | ≤125°C            |      |
| V <sub>OL</sub> | Maximum Low-Level Output<br>Voltage                                                              | $V_{in} \ge V_{T+} \max \text{ or } V_{in} \le V_{T-} \min $ $ I_{out}  \le 20 \mu A$         | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | A Y  |
| -102t FEB TON   | $V_{in} \ge V_{T+}$ max or $V_{in} \le V_{T-}$ min $ I_{out}  \le 4.0$ mA $ I_{out}  \le 5.2$ mA | 4.5<br>6.0                                                                                    | 0.26<br>0.26      | 0.33<br>0.33      | 0.40<br>0.40      |                   |      |
| lin             | Maximum Input Leakage Current                                                                    | Vin=VCC or GND                                                                                | 6.0               | ±0.1              | ± 1.0             | ±1.0              | μΑ   |
| lcc             | Maximum Quiescent Supply<br>Current (per Package)                                                | V <sub>in</sub> =V <sub>CC</sub> or GND<br>I <sub>out</sub> =0 μA                             | 6.0               | 2<br>MIROH A      | 20                | 40                | μΑ   |
| loz             | Maximum Output Leakage<br>Current                                                                | A = V <sub>T +</sub> min or V <sub>T -</sub> max<br>V <sub>out</sub> = V <sub>CC</sub> or GND | 6.0               | ±0.5              | ±5.0              | ± 10.0            | μΑ   |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

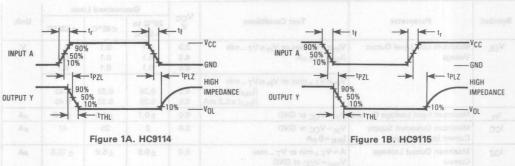
# AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

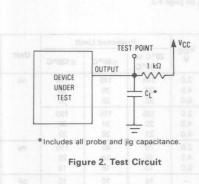
|                  |                                                                       |        | Vcc                | Pr               |                 |                 |      |
|------------------|-----------------------------------------------------------------------|--------|--------------------|------------------|-----------------|-----------------|------|
| Symbol           | Parameter                                                             | neter  |                    | 25°C to<br>-55°C | ≤85°C           | ≤125°C          | Unit |
| tPLZ,            | Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)      | HC9114 | .2.0<br>4.5<br>6.0 | 115<br>23<br>20  | 145<br>29<br>25 | 175<br>35<br>30 | ns   |
|                  |                                                                       | HC9115 | 2.0<br>4.5<br>6.0  | 125<br>25<br>21  | 155<br>31<br>26 | 190<br>38<br>32 |      |
| <sup>†</sup> THL | Maximum Output Transition Time, Any Output (Figures 1 and 2)          |        | 2.0<br>4.5<br>6.0  | 75<br>15<br>13   | 95<br>19<br>16  | 110<br>22<br>19 | ns   |
| Cin              | Maximum Input Capacitance                                             |        | -                  | 10               | 10              | 10              | pF   |
| Cout             | Maximum Three-State Output Capacitance (Output in High-Impe<br>State) | edance | -                  | 10               | 10              | 10              | pF   |

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

| CPD | Power Dissipation Capacitance (Per Buffer)                                                    | Typical @ 25°C, V <sub>CC</sub> =5.0 V |    |
|-----|-----------------------------------------------------------------------------------------------|----------------------------------------|----|
|     | Used to determine the no-load dynamic power consumption:  PD = CPD Vcc <sup>2</sup> f+Icc Vcc | 16                                     | -5 |
|     | For load considerations, see Chapter 4 subject listing on page 4-2.                           | 15                                     | pF |





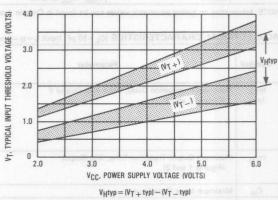
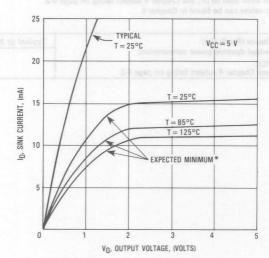


Figure 3. Typical Input Threshold, V<sub>T+</sub>, V<sub>T-</sub> Versus Power Supply Voltage



\*The expected minimum curves are not guarantees, but are design aids.

Figure 4. Open-Drain Output Characteristics

# Nine-Wide Buffers with Open-**Drain Outputs**

# **High-Performance Silicon-Gate CMOS**

The MC54/74HC9134 consists of nine inverting buffers and the MC54/74HC9135 consists of nine noninverting buffers. Both devices have inputs that are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices find primary use as interfaces between microprocessors and peripheral hardware such as keyboards, memory arrays, displays, etc. They are especially useful when 8 bits of data are needed and an extra bit is required for parity, control, or handshake.

Each of the HC9134 and HC9135 outputs are fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable pullup resistor, these gates can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

Using 9-Wide buffers, instead of standard hex buffers, decreases component count and increases system reliability.

- Output Drive Capability: 10 LSTTL Loads with Suitable Pullup Resistor
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 45 FETs or 11.25 Equivalent Gates (HC9134) 63 FETs or 15.75 Equivalent Gates (HC9135)

# HC9134 OUTPUT PROTECTION 4 DIODE 19,18,17,16,15,14,13,12,11 1,2,3,4,5,6,7,8,9 HC9135 OUTPUT PROTECTION 19,18,17,16, DIODE

LOGIC DIAGRAMS

PIN 20 = VCC PIN 10 = GND \*Denotes open-drain outputs.

# MC54/74HC9134 MC54/74HC9135



J SUFFIX CERAMIC **CASE 732** 

N SUFFIX PLASTIC **CASE 738** 



DW SUFFIX SOIC CASE 751D

#### ORDERING INFORMATION

MC74HCXXXXN MC54HCXXXXJ MC74HCXXXXDW Plastic Ceramic SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages. Dimensions in Chapter 7.

# PIN ASSIGNMENT

| - 1   |     |    | 1    |
|-------|-----|----|------|
| A1 [  | 1 . | 20 | DVCC |
| A2 [  | 2   | 19 | ] Y1 |
| A3 [  | 3   | 18 | ] Y2 |
| A4 [  | 4   | 17 | 1 Y3 |
| A5 [  | 5   | 16 | ] Y4 |
| A6 [  | 6   | 15 | ] Y5 |
| A7 [  | 7   | 14 | 1 Y6 |
| A8 [  | 8   | 13 | ] Y7 |
| A9 [  | 9   | 12 | ] Y8 |
| GND [ | 10  | 11 | ] Y9 |
|       |     |    |      |

#### **FUNCTION TABLE**

| A     | Y Outputs |        |  |
|-------|-----------|--------|--|
| Input | HC9134    | HC9135 |  |
| L     | Z         | O L    |  |
| H     | L         | Z      |  |

Z = high impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

#### MAXIMUM BATINGS\*

| Symbol           | Parameter                                                                                         | Value                        | Unit |
|------------------|---------------------------------------------------------------------------------------------------|------------------------------|------|
| Vcc              | DC Supply Voltage (Referenced to GND)                                                             | -0.5 to +7.0                 | V    |
| Vin              | DC Input Voltage (Referenced to GND)                                                              | -1.5 to V <sub>CC</sub> +1.5 | V    |
| Vout             | DC Output Voltage (Referenced to GND)                                                             | -0.5 to V <sub>CC</sub> +0.5 | V    |
| lin              | DC Input Current, per Pin                                                                         | ± 20                         | mA   |
| lout             | DC Output Current, per Pin                                                                        | ± 25                         | mA   |
| Icc              | DC Supply Current, V <sub>CC</sub> and GND Pins                                                   | ±75                          | mA   |
| PD               | Power Dissipation in Still Air, Plastic or Ceramic DIP1<br>SOIC Package1                          | 750<br>500                   | mW   |
| T <sub>stg</sub> | Storage Temperature                                                                               | -65 to +150                  | °C   |
| СЭТЕЗ            | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package)<br>(Ceramic DIP) | 260                          | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C and only beneated as studied as studied as \$2.80M and to desal SOIC Package: -7 mW/°C from 65° to 125°C and package and the studied as the studi

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

#### RECOMMENDED OPERATING CONDITIONS

| Symbol                            | Parameter                                |                         | Min  | Max   | Unit |
|-----------------------------------|------------------------------------------|-------------------------|------|-------|------|
| Vcc                               | DC Supply Voltage (Referenced to 0       | GND)                    | 2.0  | 6.0   | V    |
| V <sub>in</sub> ,V <sub>out</sub> | DC Input Voltage, Output Voltage (F      | Referenced to GND)      | 0    | Vcc   | ٧    |
| TA                                | Operating Temperature, All Package Types |                         | - 55 | + 125 | °C   |
| tr, tf                            | Input Rise and Fall Time                 | V <sub>CC</sub> = 2.0 V | 0    | 1000  | ns   |
|                                   | (Figure 1)                               | V <sub>CC</sub> = 4.5 V | 0    | 500   |      |
|                                   |                                          | V <sub>CC</sub> = 6.0 V | 0    | 400   |      |

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

|        | er s bis                                          |                                                                                                                                              | W                 | Guaranteed Limit   |                    |                    |      |
|--------|---------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|-------------------|--------------------|--------------------|--------------------|------|
| Symbol | Parameter                                         | Test Conditions                                                                                                                              | V <sub>CC</sub>   | 25°C to<br>-55°C   | ≤85°C              | ≤125°C             | Unit |
| VIH    | Minimum High-Level Input<br>Voltage               | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \le 20 \mu\text{A}$<br>(Figure 2 for $V_{out} = V_{CC} - 0.1 \text{ V}$ ) | 2.0<br>4.5<br>6.0 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V    |
| VIL    | Maximum Low-Level Input<br>Voltage                | $V_{out}$ = 0.1 V or $V_{CC}$ - 0.1 V $ I_{out}  \le 20 \mu A$ (Figure 2 for $V_{out}$ = $V_{CC}$ - 0.1 V)                                   | 2.0<br>4.5<br>6.0 | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | V    |
| VOL    | Maximum Low-Level Output<br>Voltage               | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                                                          | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | V    |
|        |                                                   | $V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$ $ I_{\text{out}}  \le 4.0 \text{ mA}$ $ I_{\text{out}}  \le 5.2 \text{ mA}$        | 4.5<br>6.0        | 0.26<br>0.26       | 0.33<br>0.33       | 0.40<br>0.40       |      |
| lin =  | Maximum Input Leakage Current                     | Vin=VCC or GND                                                                                                                               | 6.0               | ±0.1               | ±1.0               | ±1.0               | μΑ   |
| Icc    | Maximum Quiescent Supply<br>Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 µA                                                                          | 6.0               | 2                  | 20                 | 40                 | μΑ   |
| loz    | Maximum Output Leakage<br>Current                 | A = V <sub>IH</sub> or V <sub>IL</sub><br>V <sub>out</sub> = V <sub>CC</sub> or GND                                                          | 6.0               | ±0.5               | ±5.0               | ± 10.0             | μΑ   |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

<sup>\*</sup>Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

AC ELECTRICAL CHARACTERISTICS (C1 = 50 pF. Input tr = tf = 6 ns)

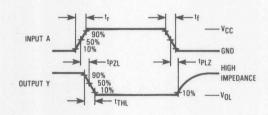
|                  |                                                                  |             | Pr                |                  |                 |                 |      |
|------------------|------------------------------------------------------------------|-------------|-------------------|------------------|-----------------|-----------------|------|
| Symbol           | Parameter                                                        |             | VCC               | 25°C to<br>-55°C | ≤85°C           | ≤125°C          | Unit |
| tPLZ,<br>tPZL    | Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2) | HC9134      | 2.0<br>4.5<br>6.0 | 115<br>23<br>20  | 145<br>29<br>25 | 175<br>35<br>30 | ns   |
|                  |                                                                  | HC9135      | 2.0<br>4.5<br>6.0 | 120<br>24<br>20  | 150<br>30<br>26 | 180<br>36<br>31 |      |
| <sup>†</sup> THL | Maximum Output Transition Time, Any Output (Figures 1 and 2)     |             |                   | 75<br>15<br>13   | 95<br>19<br>16  | 110<br>22<br>19 | ns   |
| Cin              | Maximum Input Capacitance                                        |             |                   | 10               | 10              | 10              | pF   |
| Cout             | Maximum Three-State Output Capacitance (Output in Hig State)     | h-Impedance | -                 | 10               | 10              | 10              | pF   |

#### NOTES:

- 1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- 2. Information on typical parametric values can be found in Chapter 4.

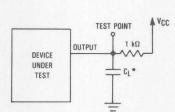
| CPD | Power Dissipation Capacitance (Per Buffer)                          | Typical @ 25°C, V <sub>CC</sub> =5.0 V |    |
|-----|---------------------------------------------------------------------|----------------------------------------|----|
|     | Used to determine the no-load dynamic power consumption:            |                                        |    |
|     | PD = CPD Vcc <sup>2</sup> f + Icc Vcc                               | 15                                     | pF |
|     | For load considerations, see Chapter 4 subject listing on page 4-2. |                                        |    |

#### **SWITCHING WAVEFORMS**



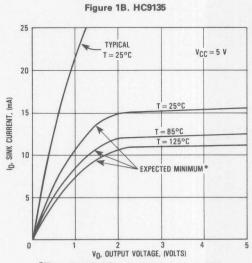
VCC INPUT A GND **←** tpZL HIGH 90% IMPEDANCE 50% OUTPUT Y -10% VOL - tTHL

Figure 1A. HC9134



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit



\*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics

|  |  |  | 25°C to<br>-55°C |  |  |  |
|--|--|--|------------------|--|--|--|
|  |  |  |                  |  |  |  |
|  |  |  |                  |  |  |  |
|  |  |  |                  |  |  |  |
|  |  |  |                  |  |  |  |
|  |  |  |                  |  |  |  |

#### 23709

- 1. For proprigation delays with hards other than 50 pF, see Chapter 4 subject feding on gone 4-2.
  - 2. Information on trained generative values can be found in Cheerter 4.

| Typical @ 28°C, Voce 5.0 V |  |
|----------------------------|--|
|                            |  |
|                            |  |
|                            |  |

#### SWEET CHING WAY EFORMS



#### Flours 1A, HC9138

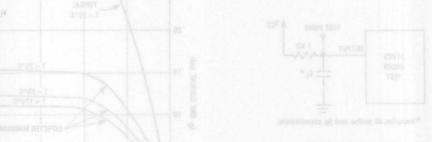


Figure 2. Test Circuit



#### MOTTOUGERFUN

The Marcola High-Speed CMOS Reliability munitar program is designed to generate an ongoing data base of reliability performance for High-Speed CMOS Logic devices. The primary purpose of the program is to identify negative treads in the date so that immediate connective action can be taken. The program size that immediate connective action is not a taken. The program size offows Matorola to develop a large data base of residently information. This information is made wellable to customers on a quarterly and yearly besis. The 1955 High-speed CMOS data base consists of results obtained from over 9500 devices from 144 lots.

#### TERT SHIP OF TARRESTON

Accelerated life testing is used to simulate long-term device operation and to gettier date for failure rate predictions. The test accordance of 125°C with test accordance bissed at 5 volts. A complete functional and do gate matric test to date sheet specifications is performed after test to date sheet specifications is performed after test to date sheet specifications is performed after save failed if parametric limits are exceeded or if functionality actions appellised in the date sheet. Forms of machinised date, the parameter actions of the parameter action of the package, are also considered to according of the package, are also considered.

A complete summary of accelerated life test data is presented in Tables 1 and 2, and Figure 1.

whereting the testing as high temperature reverse bits testing

Yable 1, 1965 Life Test Date

|  | BP<br>empots | to 6 |  |
|--|--------------|------|--|
|  |              |      |  |

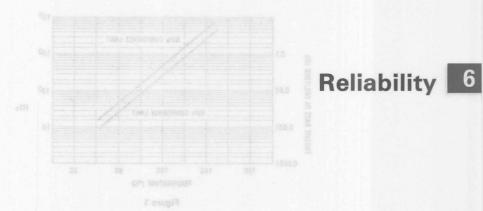
man't such that 1996 has been been been been

| Sgrips<br>Predicted<br>Fellere Race<br>Pff's |  |  |
|----------------------------------------------|--|--|
|                                              |  |  |

100 Fife # 0.019 / 1006 heart

\* See Figure 1 which doplots fature rete versus temperature.

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#### INTRODUCTION

The Motorola High-Speed CMOS Reliability monitor program is designed to generate an ongoing data base of reliability performance for High-Speed CMOS Logic devices. The primary purpose of the program is to identify negative trends in the data so that immediate corrective action can be taken. The program also allows Motorola to develop a large data base of reliability information. This information is made available to customers on a quarterly and yearly basis. The 1985 High-Speed CMOS data base consists of results obtained from over 9500 devices from 144 lots.

#### **ACCELERATED LIFE TEST**

Accelerated life testing is used to simulate long-term device operation and to gather data for failure rate predictions. The test is conducted at an ambient temperature of 125°C with devices biased at 5 volts. A complete functional and dc parametric test to data sheet specifications is performed after 48,168, and 1008 cumulative hours. A device is considered to have failed if parametric limits are exceeded or if functionality cannot be demonstrated under nominal and worst-case conditions specified in the data sheet. Forms of mechanical damage, such as cracking of the package, are also considered failures.

A complete summary of accelerated life test data is presented in Tables 1 and 2, and Figure 1.

Accelerated life testing is also referred to as high temperature operating life testing or high temperature reverse bias testing.

Table 1. 1985 Life Test Data

|         |              | 125°C       | 5 V          |               |                     |
|---------|--------------|-------------|--------------|---------------|---------------------|
| 74НСХХХ | # of<br>Lots | 48<br>Hours | 168<br>Hours | 1008<br>Hours | Total<br>% Failures |
| Plastic | 38           | 2/3763      | 0/3758       | 2/3751        | 0.10                |

Table 2. Summary of 1985 Life Test Data

| 74HCXXX | Total<br>Failures | 125°C<br>Device Hours | 85°C<br>Equivalent<br>Device Hours | 85°C*<br>Predicted<br>Failure Rate<br>FITs |
|---------|-------------------|-----------------------|------------------------------------|--------------------------------------------|
| Plastic | 4                 | 3.80×10 <sup>6</sup>  | 3.70 × 10 <sup>7</sup>             | 219**<br>141***                            |

100 FITs = 0.01% / 1000 hours

<sup>\*\*\*0.7</sup> eV; 60% Confidence Limit

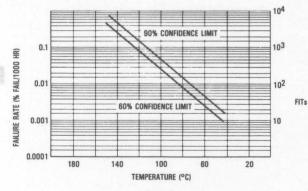


Figure 1

<sup>\*</sup>See Figure 1 which depicts failure rate versus temperature.

<sup>\*\*0.7</sup> eV; 90% Confidence Limit

#### TEMPERATURE HUMIDITY BIAS

Temperature Humidity Bias (THB) is an environmental test designed to evaluate the moisture-related performance of the package-die combination. THB is a destructive test performed under a 5 volt bias at 85°C and 85% relative humidity. Electrical performance is measured at 504 and 1008 hours to full data sheet specifications. A device is considered to have failed the temperature humidity bias test if parametric limits are exceeded or if functionality cannot be demonstrated under the conditions specified in the data sheet. Results of the 1985 temperature humidity bias testing are shown in Table 3.

Table 3. Temperature Humidity Bias

| 00 0 00 /0 H.H. 0 VOILS |              |           |            |            |  |
|-------------------------|--------------|-----------|------------|------------|--|
| 74HCXXX                 | # of<br>Lots | 504 Hours | 1008 Hours | % Failures |  |
| Plastic                 | 33           | 0/2231    | 1/2086     | 0.05       |  |

#### **AUTOCLAVE**

Autoclave, like THB, is an environmental test which measures device resistance to moisture penetration along the lead-frame-plastic interface. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig; no bias voltage is applied. Corrosion of the die is the expected failure mechanism. As with THB testing, both package integrity and actual die construction play a major role in the results. Autoclave is a highly accelerated, destructive test.

Failure criteria for autoclave testing are the same as those used for THB testing. Cosmetic package defects and degradation of lead finish and solderability are not considered as reject criteria.

Autoclave results for 1985 are found in Table 4. The single failure, detected at the 144 hour test point, failed for input leakage; no corrosion was found.

Table 4. Autoclave 121°C 100% R.H. 15 psig

|         | 121°C        | 100% H.   | H. 15 psi | 9          |
|---------|--------------|-----------|-----------|------------|
| 74HCXXX | # of<br>Lots | 144 Hours | 240 Hours | % Failures |
| Plastic | 41           | 1/1995    | 0/2084    | 0.05       |

#### TEMPERATURE CYCLE

The compatibility of materials used in the fabrication of any device is essential to its reliability. Any appreciable mismatch in physical properties, such as thermal expansion coefficients, can cause long-term device failures. Those concerns are investigated by performing temperature cycling.

During temperature cycle testing, devices are loaded into a cycling system and held at  $-65^{\circ}\text{C}$  for at least ten minutes, then brought to  $+150^{\circ}\text{C}$  for at least ten minutes. The system employs a circulating air environment to assure rapid stabilization at the specified temperatures. The dwell at each extreme, plus two transition periods of five minutes, constitute one cycle.

Devices are electrically tested after 500 and 1000 cumulative cycles. A device is defined as a failure if parametric limits are exceeded, or if functionality cannot be demonstrated per data sheet specifications. Mechanical damage, such as cracking, chipping, or breaking of the package, are also considered as failure criteria, provided such damage was not induced by fixturing or handling. Results of temperature cycle tests are found in Table 5.

Table 5. Temperature Cycle

| 74HCXXX | # of<br>Lots | 500 Cycles | 1000 Cycles | Cumulative % Failures |
|---------|--------------|------------|-------------|-----------------------|
| Plastic | 32           | 1/1803     | 0/1800      | 0.05                  |

#### CONCLUSIONS

Thorough reliability testing has been performed on an extensive cross section of the High-Speed CMOS Logic family. The evaluations included accelerated life tests and a series of environmental stresses designed to assess package integrity, moisture resistance, and thermal compatibility. Through these tests, Motorola's High-Speed CMOS has proven to be an exceptionally reliable family of devices. Reliability testing is performed on a continuous basis, and comprehensive reports are issued annually. Reports are available upon customer request.

For additional information, contact CMOS Logic Reliability Engineering at:

CMOS Logic Reliability Engineering Motorola Inc. 3501 Ed Bluestein Boulevard Austin, Texas 78721

Temperature Hamilday Bins (THB) is an environmental festestigned to evaluate the mostsum-related performance of the society of the properties. THB is a destructive test performed ander a 5 volt bias at 85°C and 85°S relative handday. Electrical ordernance is measured at 504 and 1006 hours to full date hast specifications. A device is considered to have failed the emperature humility bias real if parametric finits are encoded in the hordenality connot be demonstrated under the conditions of the foliotist in the charaster of the 1985 temperature pecified in tipe charaster are shown to Table 3.

Table 3. Temperature Hemidity Bias

#### **AUTOCLAY**

Autoclave, like THB, is an environmental test which oversures device reliatance to molecure penetration along the leadframe-plastic interfuce. Conditions employed during the cest houses 721°C, 100% relative numbridity, and 18 ptig, no blas voltage is applied. Corrector of the dis take expected fallure mechanism. As with THB testing, both peckage integrity and actual disconstruction play a major role in the results. Aupodered is a blooky accelerated, destructive test.

Failure origina for autodiave tosting are the same as those used for THB tenting. Committe package detects and degradation of load finish and solderability are not considered as reject origins.

Autoclays results for 1935 are found in Table 4. The single failure, detected or tire 144 hour test point, failed for input loskage; no connacos was found.

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|  | 17,1698 |  |
|--|---------|--|

The compatibility of materials used in the fabrication of any device is essential to its refability. Any appreciable mismatch in physical properties, such as themast expansion coefficients, see a concern and appreciate them device fabrica. Those concerns are investigated by appreciate themastates making the device fabrical and the concerns are in-

During température cycle testing, devices are loaded into a cycling system and hold at -60°C for at least ten minutes, then bequent to +150°C for at least ten minutes. The system employe a circulating air environment to essure rapid atability attents, plus the specified temperatures. The dwell at each externer, plus two transition periods of five minutes, constitute one cycle.

Devices are electrically tested after 500 and 1000 comulative cycles. A device is defined as a failure if parametric limits are exceeded, or if functionality cannot be demonstrated per data sheet specifications. Machanical demangs, such as cracking chipping, or breaking of the package, are also considered as failure criteria, provided such damage was not induced by fourting or bending. Results of temperature cycle tests are found in Table 5.

Table 5. Temperature Cycle

#### CONCLUSIONS

Thorough reliability testing has been performed on an extensive onuse section of the High-Speed CMOS Logic family.
The evaluations included accelerated tile fasts and a series of projection resistance, and thermal comparibility. Through these recisions resistance, and thermal comparibility. Through these sacts. Moreous's High-Speed CMOS has proven to be an experimentally reliable family of devices. Reliability treating is performed on a continuous basis, and comprehensive reports are issued annually. Reports are available upon customar

For additional information, contact CMOS Logic Reliability

CMOS Logic Reliability Engineerin

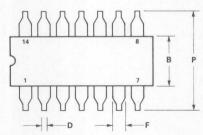
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Augula, Texas 78721

Package Dimensions 7

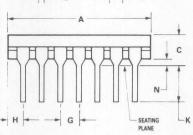
The packaging availability for each device is indicated on the individual data sheets. Dimensions for the packages are given in this section.

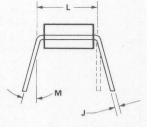
#### - 14-PIN PACKAGES -



J SUFFIX CERAMIC **CASE 632-07** 





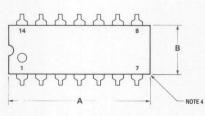


#### NOTES:

- 1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
- 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 3. DIMENSION "A" AND "B" (632-07) DO NOT INCLUDE GLASS RUN-OUT.
- LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE 4. POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

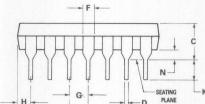
N SUFFIX PLASTIC CASE 646-06

|     | MILLIN   | IETERS | INC       | HES   |  |
|-----|----------|--------|-----------|-------|--|
| DIM | MIN      | MAX    | MIN       | MAX   |  |
| Α   | 19.05    | 19.94  | 0.750     | 0.785 |  |
| В   | 6.10     | 7.49   | 0.240     | 0.295 |  |
| C   | _        | 5.08   | _         | 0.200 |  |
| D   | 0.38     | 0.58   | 0.015     | 0.023 |  |
| F   | 1.40     | 1.77   | 0.055     | 0.070 |  |
| G   | 2.54     | BSC    | 0.100 BSC |       |  |
| Н   | 1.91     | 2.29   | 0.075     | 0.090 |  |
| J   | 0.20     | 0.38   | 0.008     | 0.015 |  |
| K   | 3.18     | 4.32   | 0.125     | 0.170 |  |
| L   | 7.62 BSC |        | 0.300     | BSC   |  |
| M   | _        | 15°    | _         | 15°   |  |
| N   | 0.51     | 1.02   | 0.020     | 0.040 |  |









#### NOTES:

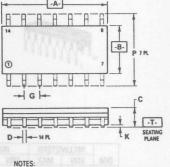
- POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE 3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  - 4. ROUNDED CORNERS OPTIONAL; AS SHOWN IN PREVIOUS ISSUE.

|     | MILLIM | IETERS   | INCHES |       |
|-----|--------|----------|--------|-------|
| DIM | MIN    | MAX      | MIN    | MAX   |
| A   | 18.16  | 19.56    | 0.715  | 0.770 |
| В   | 6.10   | 6.60     | 0.240  | 0.260 |
| С   | 3.69   | 4.69     | 0.145  | 0.185 |
| D   | 0.38   | 0.53     | 0.015  | 0.021 |
| F   | 1.02   | 1.78     | 0.040  | 0.070 |
| G   | 2.54   | 2.54 BSC |        | BSC   |
| Н   | 1.32   | 2.41     | 0.052  | 0.095 |
| J   | 0.20   | 0.38     | 0.008  | 0.015 |
| K   | 2.92   | 3.43     | 0.115  | 0.135 |
| L   | 7.62   | BSC      | 0.300  | BSC   |
| M   | 0°     | 10°      | 0°     | 10°   |
| N   | 0.39   | 1.01     | 0.015  | 0.039 |

#### 14-PIN PACKAGES -

D SUFFIX SOIC **CASE 751A-02** 

-R X 45°



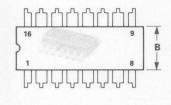


- 1. DIMENSIONS A AND B ARE DATUMS AND T IS A 4. DIMENSIONING AND TOLERANCING PER ANSI DATUM SURFACE.
- 2. POSITIONAL TOLERANCE FOR D DIMENSION
- - 3. POSITIONAL TOLERANCE FOR P DIMENSION (7 PLACES):
  - ♦ 0.25 (0.010) @ B @
- Y14.5M, 1982.
- 5. CONTROLLING DIMENSION: MILLIMETER.
- 6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- 7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

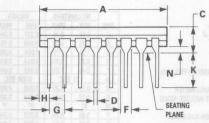
|     | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
| DIM | MIN         | MAX  | MIN       | MAX   |
| A   | 8.55        | 8.75 | 0.337     | 0.344 |
| В   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.054     | 0.068 |
| D   | 0.35        | 0.49 | 0.014     | 0.019 |
| F   | 0.40        | 1.25 | 0.016     | 0.049 |
| G   | 1.27        | BSC  | 0.050 BSC |       |
| J   | 0.19        | 0.25 | 0.008     | 0.009 |
| K   | 0.10        | 0.25 | 0.004     | 0.009 |
| M   | 0°          | 7°   | 0°        | 7°    |
| P   | 5.80        | 6.20 | 0.229     | 0.244 |
| R   | 0.25        | 0.50 | 0.010     | 0.019 |

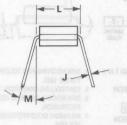
CASE 751A-02

#### J SUFFIX CERAMIC **CASE 620-08**







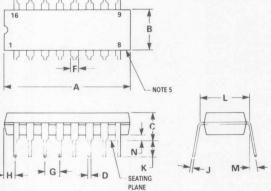


#### NOTES:

- 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE PARALLEL. POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- 2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
- 3. DIM "L" TO CENTER OF LEADS WHEN FORMED
- 4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
- 5. DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

|     | MILLIN   | ETERS | INC       | HES   |
|-----|----------|-------|-----------|-------|
| DIM | MIN      | MAX   | MIN       | MAX   |
| A   | 19.05    | 19.94 | 0.750     | 0.785 |
| В   | 6.10     | 7.49  | 0.240     | 0.295 |
| C   | NA FILL  | 5.08  | 3 _       | 0.200 |
| D   | 0.38     | 0.53  | 0.015     | 0.021 |
| F   | 1.40     | 1.78  | 0.055     | 0.070 |
| G   | 2.54     | BSC   | 0.100 BSC |       |
| Н   | 0.51     | 1.14  | 0.020     | 0.045 |
| J   | 0.20     | 0.30  | 0.008     | 0.012 |
| K   | 3.18     | 4.32  | 0.125     | 0.170 |
| L   | 7.62 BSC |       | 0.300     | BSC   |
| M   | _        | 15°   | _         | 15°   |
| N   | 0.51     | 1.02  | 0.020     | 0.040 |







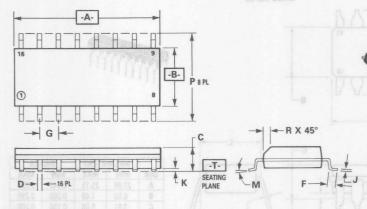
|     | MILLIN | IETERS | INCHES    |       |  |
|-----|--------|--------|-----------|-------|--|
| DIM | MIN    | MAX    | MIN       | MAX   |  |
| Α   | 18.80  | 21.34  | 0.740     | 0.840 |  |
| В   | 6.10   | 6.60   | 0.240     | 0.260 |  |
| C   | 3.69   | 4.69   | 0.145     | 0.185 |  |
| D   | 0.38   | 0.53   | 0.015     | 0.021 |  |
| F   | 1.02   | 1.78   | 0.040     | 0.070 |  |
| G   | 2.54   | BSC    | 0.100 BSC |       |  |
| Н   | 0.38   | 2.41   | 0.015     | 0.095 |  |
| J   | 0.20   | 0.38   | 0.008     | 0.015 |  |
| K   | 2.92   | 3.43   | 0.115     | 0.135 |  |
| L   | 7.62   | BSC    | 0.300     | BSC   |  |
| M   | 0°     | 10°    | 0°        | 10°   |  |
| N   | 0.39   | 1.01   | 0.015     | 0.040 |  |

#### NOTES:

- POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE 3. DIMENSION "B" DOES NOT INCLUDE MOLD
  - 4. "F" DIMENSION IS FOR FULL LEADS.
  - 5. ROUNDED CORNERS OPTIONAL.

## 16-PIN PACKAGES

D SUFFIX SOIC CASE 751B-03

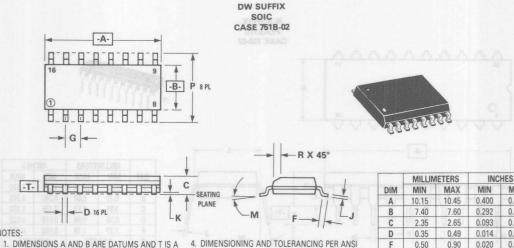


#### NOTES:

- DATUM SURFACE.
- 2. POSITIONAL TOLERANCE FOR D DIMENSION (16 PLACES):
  - ♦ 0.25 (0.010) M T B S A S
- 3. POSITIONAL TOLERANCE FOR P DIMENSION (8 PLACES):
  - ♦ 0.25 (0.010) M B M
- 1. DIMENSIONS A AND B ARE DATUMS AND T IS A 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - 5. CONTROLLING DIMENSION: MILLIMETER.
  - 6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  - 7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

|     | MILLIN | METERS | INCHES    |       |
|-----|--------|--------|-----------|-------|
| DIM | MIN    | MAX    | MIN       | MAX   |
| Α   | 9.80   | 10.00  | 0.386     | 0.393 |
| В   | 3.80   | 4.00   | 0.150     | 0.157 |
| C   | 1.35   | 1.75   | 0.054     | 0.068 |
| D   | 0.35   | 0.49   | 0.014     | 0.019 |
| F   | 0.40   | 1.25   | 0.016     | 0.049 |
| G   | 1.27   | BSC    | 0.050 BSC |       |
| J   | 0.19   | 0.25   | 0.008     | 0.009 |
| K   | 0.10   | 0.25   | 0.004     | 0.009 |
| M   | 0°     | 7°     | 0°        | 7°    |
| P   | 5.80   | 6.20   | 0.229     | 0.244 |
| R   | 0.25   | 0.50   | 0.010     | 0.019 |

CASE 751B-03



#### NOTES:

- DATUM SURFACE.
- 2. POSITIONAL TOLERANCE FOR D DIMENSION (16 PLACES):
  - ◆ 0.25 (0.010) M T B S A S
- 3. POSITIONAL TOLERANCE FOR P DIMENSION (8 PLACES):
  - ♦ 0.25 (0.010) M B M

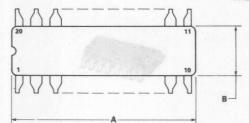
- Y14.5M, 1982.
- 5. CONTROLLING DIMENSION: MILLIMETER.
- 6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- 7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

|     | 1411# [01141 |       | HAOTIEO |       |  |
|-----|--------------|-------|---------|-------|--|
| DIM | MIN          | MAX   | MIN     | MAX   |  |
| A   | 10.15        | 10.45 | 0.400   | 0.411 |  |
| В   | 7.40         | 7.60  | 0.292   | 0.299 |  |
| C   | 2.35         | 2.65  | 0.093   | 0.104 |  |
| D   | 0.35         | 0.49  | 0.014   | 0.019 |  |
| F   | 0.50         | 0.90  | 0.020   | 0.035 |  |
| G   | 1.27         | BSC   | 0.050   | BSC   |  |
| J   | 0.25         | 0.32  | 0.010   | 0.012 |  |
| K   | 0.10         | 0.25  | 0.004   | 0.009 |  |
| M   | 0°           | 7°    | 0°      | 7°    |  |
| P   | 10.05        | 10.55 | 0.395   | 0.415 |  |
|     | 0.25         | 0.75  | 0.010   | 0.029 |  |

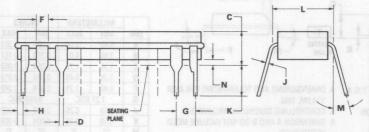
CASE 751G-01

#### 20-PIN PACKAGES =









NOTES:

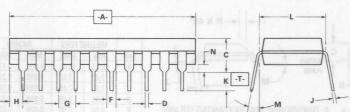
- POSITION AT SEATING PLANE, AT MAXIMUM PARALLEL. MATERIAL CONDITION.
- 1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE 2. DIM L TO CENTER OF LEADS WHEN FORMED
  - 3. DIM A AND B INCLUDES MENISCUS.

| DIM | MILLIMETERS |          | INCHES    |       |
|-----|-------------|----------|-----------|-------|
|     | MIN         | MAX      | MIN       | MAX   |
| A   | 23.88       | 25.15    | 0.940     | 0.990 |
| В   | 6.60        | 7.49     | 0.260     | 0.295 |
| C   | 3.81        | 5.08     | 0.150     | 0.200 |
| D   | 0.38        | 0.56     | 0.015     | 0.022 |
| F   | 1.40        | 1.65     | 0.055     | 0.065 |
| G   | 2.54 BSC    |          | 0.100 BSC |       |
| Н   | 0.51        | 1.27     | 0.020     | 0.050 |
| J   | 0.20        | 0.30     | 0.008     | 0.012 |
| K   | 3.18        | 4.06     | 0.125     | 0.160 |
| L   | 7.62        | 7.62 BSC |           | BSC   |
| M   | 0           | 15"      | 0°        | 15°   |
| N   | 0.25        | 1.02     | 0.010     | 0.040 |

N SUFFIX PLASTIC CASE 738-02

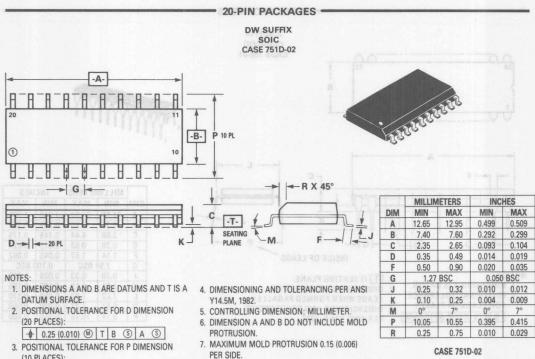






- 1. DIM -A- IS DATUM.
- 2. POSITIONAL TOL FOR LEADS:
- 3. -T- IS SEATING PLANE.
- 4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
  5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
- ♦ 0.25 (0.010) M T A M 6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

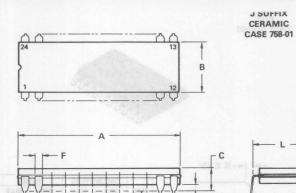
| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 25.65       | 27.18 | 1.010     | 1.070 |
| В   | 6.10        | 6.60  | 0.240     | 0.260 |
| C   | 3.94        | 4.57  | 0.155     | 0.180 |
| D   | 0.38        | 0.56  | 0.015     | 0.022 |
| F   | 1.27        | 1.78  | 0.050     | 0.070 |
| G   | 2.54 BSC    |       | 0.100 BSC |       |
| Н   | 1.65 NOM    |       | 0.065     | NOM   |
| J   | 0.20        | 0.38  | 0.008     | 0.015 |
| K   | 2.79        | 3.56  | 0.110     | 0.140 |
| L   | 7.62 BSC    |       | 0.300     | BSC   |
| M   | 0°          | 15°   | 0°        | 15°   |
| N   | 0.51        | 1.02  | 0.020     | 0.040 |



**CASE 751D-02** 

(10 PLACES):

♦ 0.25 (0.010) M B M



T-





#### NOTES:

- 1. DIMENSION A IS DATUM.
- 2. POSITIONAL TOLERANCE FOR LEADS: 24 PLACES

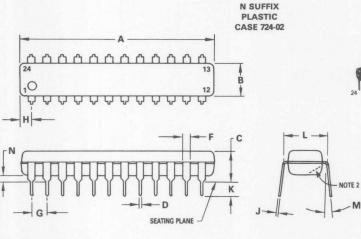
  10.25 (0.010) | T AM
- 3. T. IS SEATING PLANE.

G

- 4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

INSIDE OF LEADS

|     | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
| DIM | MIN         | MAX   | MIN       | MAX   |
| Α   | 31.50       | 32.64 | 1.240     | 1.285 |
| В   | 7.24        | 7.75  | 0.285     | 0.305 |
| C   | 3.68        | 4.44  | 0.145     | 0.175 |
| D   | 0.38        | 0.53  | 0.015     | 0.021 |
| F   | 1.14        | 1.57  | 0.045     | 0.062 |
| G   | 2.54 BSC    |       | 0.100 BSC |       |
| J   | 0.20        | 0.33  | 0.008     | 0.013 |
| K   | 2.54        | 4.19  | 0.100     | 0.165 |
| L   | 7.62        | 7.87  | 0.300     | 0.310 |
| N   | 0.51        | 1.27  | 0.020     | 0.050 |
| P   | 9.14        | 10.16 | 0.360     | 0.400 |





|     | MILLIN | IETERS | INCHES    |       |  |
|-----|--------|--------|-----------|-------|--|
| DIM | MIN    | MAX    | MIN       | MAX   |  |
| Α   | 31.24  | 32.13  | 1.230     | 1.265 |  |
| В   | 6.35   | 6.86   | 0.250     | 0.270 |  |
| C   | 4.06   | 4.57   | 0.160     | 0.180 |  |
| D   | 0.38   | 0.51   | 0.015     | 0.020 |  |
| F   | 1.02   | 1.52   | 0.040     | 0.060 |  |
| G   | 2.54   | BSC    | 0.100 BSC |       |  |
| Н   | 1.60   | 2.11   | 0.063     | 0.083 |  |
| J   | 0.18   | 0.30   | 0.007     | 0.012 |  |
| K   | 2.92   | 3.43   | 0.115     | 0.135 |  |
| L   | 7.37   | 7.87   | 0.290     | 0.310 |  |
| M   | _      | 10°    | _         | 10°   |  |
| N   | 0.51   | 1.02   | 0.020     | 0.040 |  |

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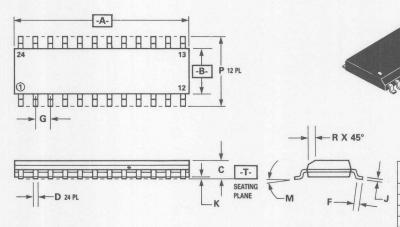
LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010)
 DIA AT SEATING PLANE AT MAXIMUM MATERIAL
 CONDITION (DIM D).

2. CHAMFERRED CONTOUR OPTIONAL.

NOTES:

#### - 24-PIN PACKAGES -

DW SUFFIX SOIC CASE 751E-01



|     | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
| DIM | MIN         | MAX   | MIN       | MAX   |
| A   | 15.25       | 15.50 | 0.601     | 0.610 |
| В   | 7.40        | 7.60  | 0.292     | 0.299 |
| C   | 2.35        | 2.65  | 0.093     | 0.104 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.50        | 0.90  | 0.020     | 0.035 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.25        | 0.32  | 0.010     | 0.012 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 10.05       | 10.55 | 0.395     | 0.415 |
| R   | 0.25        | 0.75  | 0.010     | 0.029 |

#### CASE 751E-01

#### NOTES:

- DATUM SURFACE.
- 2. POSITIONAL TOLERANCE FOR D DIMENSION (24 PLACES):
  - ♦ 0.25 (0.010) M T B S A S
- 3. POSITIONAL TOLERANCE FOR P DIMENSION (12 PLACES):
  - ♦ 0.25 (0.010) M B M
- 1. DIMENSIONS A AND B ARE DATUMS AND T IS A 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - 5. CONTROLLING DIMENSION: MILLIMETER.
  - 6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  - 7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

# PACKA (STONENSIONS

